Maintenance Manual

for

Model 2250 Digital Analyzing Voltmeter

5K5

MP MASTER
MA29400

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instrument division
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MODEL 2250

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In SECTION 1 - GENERAL INFORMATION add the following to paragraph 1-1 INTRODUCTION:

The Model 2250 has been manufactured in two different hardware configurations. These units either have the TOTAL/AVG function or they do not. Unit versions can be identified by their check sum numbers. Table 1-1A identifies model versions and check sum number data as well as the NAI manual that should accompany the unit.

Table 1-1A. F1/F1X Model Identification Chart

NAI Manual No.	Model Version	Check Sum Number
2250 MM-I-5027-1,-2 IM-I-5026A	1.0	3b1C
	1.1	dAb0
	1.2	E4A0
	1.3	3bdF
	1.4	46bF
	2.0	b767
	2.1	6767
	2.2	F9C5
	2.3	9595
	2.4	A7F4
	2.5	6044
2250 MM-I-5027A IM-I-5026B (TOTAL/AVG Configuration)	3.0	13Ab
	3.1	8Fb6
	4.0	F8C9
	5.0	52CF
	5.1	8E65
	5.2	7458
	5.3	C3A3
	5.4	54d1
	6.0	016E

Table 1-2A. F2/F2X Model Identification Chart

NAI Manual No.	Model Version	Check Sum Number
2250 MM-I-5027A IM-I-5026B (TOTAL/AVG Configuration)	1.0	dE24
	1.1	FdBe
	2.0	FB2E
	2.1	FB46

In SECTION 3 CHECKOUT, ALIGNMENT, AND CALIBRATION change the following:

1. In paragraph 3-6.e procedural step 21 change test point reference designations:

   FROM: A12TP1 and A12TP6
   TO: A12TP19 and A12TP2

2. In paragraph 3-4.f procedural step 20 add the following:

   Set A8SW2 towards rear of unit.

3. In paragraph 3-4.j change the following:

   a. Replace procedural step 11 as follows:

      11. Remove shorting jumper from DAV SIG input terminals and connect variable signal source.

   b. Add the following procedural steps:

      16. On DAV, press QUAD key.

      17. Press PHASE OFFSET 2, 7, 0 and ENTER keys in that order.

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In SECTION 3 paragraph 3-4.g change the following:

1. In procedural steps 5 and 9 change reference designations

FROM: A14R14
TO: A14R10

2. In procedural steps 7 and 11 change the reference designations

FROM: A14R10
TO: A14R14

In SECTION 1 - GENERAL INFORMATION Table 1-5. Specifications, change THD accuracy data as follows:

Item	Specification
THD accuracy (For fundamental frequency of 10 Hz to 10 kHz)	For THD readings $\geq$2%: ±0.015 x reading For THD readings <2%: $\pm[0.03 + (0.015 \times \frac{\text{VSCALE}}{\text{ERMS}})]$ where: VSCALE is the voltage scale annunciated ERMS is the signal voltage

In SECTION 6 - PARTS LIST change the following:

1. In Table 6-21. Replacement Parts List: Rear Panel Assembly A17 - 787277 change the following:

   a. Add A17B1MP2 Rubber Grommet NAI P/N 882970.
   b. Add A17T1P1 Connector (6-pin female) NAI P/N 888365 and pins NAI P/N 886039 (6 required).
   c. Add to Connector A17T1J1 the following:

      Pin (5 required) NAI P/N 880224

2. In Table 6-25. Replacement Parts List: Isolated Power Supply Assembly A17PS2, A17PS3 - 787313-1 add the following to Transformer Assembly A17PS2T1 and A17PS3T1:

   a. Connector NAI P/N 886409
   b. Pin (4 required) NAI P/N 886407

3. In Table 6-26. Replacement Parts List: Isolated Power Supply Circuit Card Assembly A17PS2A1, A17PS3A1 - 787180-1 add to W1 Cable Assembly the following:

   A17PS2P1 Connector (6-pin female) NAI P/N 886462 and cover NAI P/N 884832.

In SECTION 1 - GENERAL INFORMATION add the following note below Table 1-3. Features and Options:

NOTE

The Model 2250 chassis is supplied with mounting holes to accommodate Jonathan Interior Slides P/N 1302541B-R and 1302541B-L. Refer to Figure 1-3 for details.

In SECTION 6 PARTS LIST change the following:

1. In Table 6-26. Replacement Parts List: Isolated Power Supply CCA A17PS2A1, A17PS3A1 - 787180-1 Revision A delete capacitors C7 and C8.

2. In Figure 6-24. Isolated Power Supply A17PS2A1, A17PS3A1 (P/N 787180-1 Revision A), Parts Location Diagram delete capacitors C7 and C8.

MODEL 2250

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WARNING

Failure to ground the chassis could bring operator and maintenance personnel in contact with high voltages capable of causing personal injury or death.

WARNING

If the top cover of the Model 2250 is removed while the guard terminals are driven with a voltage, operator and maintenance personnel could come in contact with high voltages capable of causing personal injury or death.

WARNING

The front SIG and REF binding posts are connected to the corresponding rear panel connectors. If a high voltage is applied to the front input binding posts, high voltages capable of causing personal injury or death will appear at the rear input connectors. Similarly, if a high voltage is applied at the rear input connectors, a high voltage capable of causing personal injury or death will appear at the front binding posts.

MODEL 2250

SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION.

This manual provides maintenance instructions for the Digital Analyzing Voltmeter Model 2250 shown in figure 1-1, hereinafter referred to as the DAV. (A user's Instruction Manual also is available for the DAV.) Maintenance information is presented in eight sections as follows:

a. SECTION 1 - GENERAL INFORMATION.

This section describes the purpose and gives a physical description of the DAV. Several lists of interest to maintenance people are compiled in this section including lists of DAV specifications, major assemblies, and special tools and test equipment required to maintain the DAV.

b. SECTION 2 - THEORY OF OPERATION.

This section includes an overall block diagram discussion of the DAV; a system software discussion; DAV functional circuit interrelationships and circuit board descriptions based on detailed functional signal flow and schematic diagrams.

c. SECTION 3 - CHECKOUT, CALIBRATION AND ALIGNMENT.

This section begins with a schedule for performing checkout, alignment, and calibration on a periodic basis. The schedule is followed by the actual procedures in each category.

d. SECTION 4 - TROUBLESHOOTING.

This section provides troubleshooting instructions for isolating faults within the DAV. Troubleshooting is based on symptoms derived from performing the checkout procedure, error codes encountered during autocalibration, and from possible malfunctions during use of the DAV.

e. SECTION 5 - REPAIR.

This section gives removal and replacement instructions for use in repairing the DAV after fault isolation.

f. SECTION 6 - PARTS LIST.

This section contains replaceable parts lists, federal supply codes of manufacturers (FSCM), parts location diagrams, and a list of manufacturers of parts used for the DAV.

g. SECTION 7 - SCHEMATIC DIAGRAMS.

This section contains schematic diagrams for the DAV.

h. SECTION 8 - UPDATE INFORMATION.

This section contains Product Revision Sheet (PRS) data which updates the unit to the most current configuration available.

The manual reflects the current configuration of the Model 2250. For model identification purposes, on power-up the unit displays a check sum number for two seconds. Refer to tables 1-1 and 1-2 to determine versions and corresponding check sum numbers. Version numbers are assigned as follows: 1.0, 1.1, 1.2...1.X; 2.0, 2.1, 2.2...2.X; etc. The X indicates all features are applicable to that particular version.

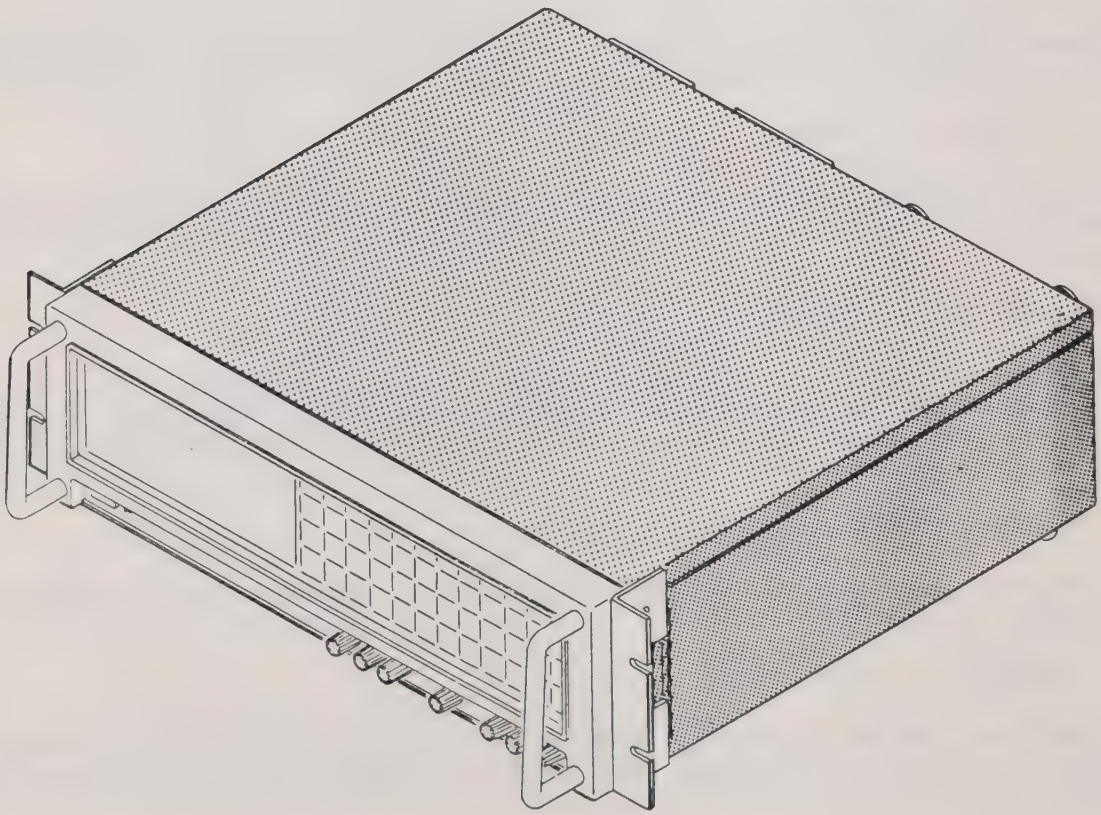


Figure 1-1. Digital Analyzing Voltmeter, Model 2250

Table 1-1. F1 Unit Version/Check Sum Numbers

MODEL VERSION	CHECK SUM NUMBER
5.0	52CF
5.1	8E65
5.2	7458
5.3	C3A3
5.4	54d1

Table 1-2. F2 Unit Version/Check Sum Numbers

MODEL VERSION	CHECK SUM NUMBER
1.1	Fd8E
1.2	C5D0
1.3	F5A0
1.4	0b26

1-2. FEATURES AND OPTIONS.

The DAV is available with various options and custom configurations. To determine features and options, a single digit number is assigned in accordance with table 1-3.

For example, a DAV with Native IEEE Interface (standard 2250) would have a feature/option number of F1.

F [1]

F1

Table 1-3. Features and Options

FEATURE		OPTION
NO,	DESCRIPTION	
F1	Interface Feature	1. Native IEEE Interface
		2. MATE-CIIL and Native IEEE Interface
		3. 225 Emulation IEEE Interface

1-3. PURPOSE.

The DAV is a multifunction voltmeter that combines a total voltmeter, a phase angle voltmeter, and a waveform signal analyzer in a single microprocessor-based instrument. As a total voltmeter the DAV can be used for the rms measurement of a total ac signal including harmonics. In addition, the DAV can make various voltage gain and attenuation measurements directly in decibels. As a phase angle voltmeter the DAV is capable of making the following multifrequency, phase-sensitive measurements on an ac signal.

a. PHASE ANGLE.

The amount of phase shift in degrees between the signal and reference voltage.

b. FUNDAMENTAL.

The RMS measurement of a fundamental signal voltage without noise and harmonics.

c. IN PHASE.

The rms measurement of the vector component of a signal voltage that is in-phase with a reference voltage.

d. QUADRATURE.

The rms measurement of the quadrature vector component of a signal voltage that is 90° out-of-phase with a reference voltage.

e. SIGNAL-TO-REFERENCE RATIO.

Used with total, fundamental, in-phase, and quadrature modes to display a signal-to-reference ratio.

As an analyzer the DAV uses a combination of waveform sampling and signal processing techniques to determine the magnitudes, phases, and harmonic parameters of a signal waveform under investigation. The DAV applies this feature for making total harmonic distortion measurement. The DAV is capable of making mathematical adjustments to facilitate signal analysis. These adjustments include phase and magnitude offsets, variable scale factors, percent deviation and dB scaling. The DAV has a dual-channel measurement system that uses identical, though isolated, signal and reference circuits. The isolation feature enables input voltages to float with respect to circuit ground.

1-4. PHYSICAL DESCRIPTION.

The DAV is packaged as shown in figure 1-1.

Details of the physical features of the DAV are presented in figure 1-2. The front panel contains several groups of controls and indicators including a power switch, a set of input terminals, a numeric keypad, a set of function keys, and a display. The

rear panel contains a group of connectors, address switches, and an input power receptacle and fuse. A complete description of the function and use of controls and indicators is covered in the separate DAV user's Instruction Manual.

With the top cover of the DAV removed, all the major assemblies are available for servicing. The major assemblies shown in figure 1-2 are listed in table 1-2. The DAV is supplied either for table top or rack mounting, as shown in the outline and dimension drawing of figure 1-3. For table top use simply place the unit horizontally on a bench or shelf so that it rests securely on the four mounting feet.

CAUTION

The DAV contains mercury-wetted relays and must be operated in a horizontal position. If the DAV is tilted more then ±30° from horizontal during operation, it will not operate properly; and may be damaged.

Rack mount ears are provided to secure the DAV to a standard 19-inch equipment rack. Slides or mounting hardware are not supplied.

1-5. MAJOR ASSEMBLIES.

Table 1-4 lists the major assemblies of the DAV that are shown in figure 1-2 and the current revision status of each assembly.

1-6. SPECIFICATIONS.

The technical features and capabilities of the DAV are compiled in specifications table 1-6.

1-7. SPECIAL TOOLS AND TEST EQUIPMENT.

Table 1-7 lists the special tools and standard test equipment required to maintain the DAV. The equipment listed or equivalent may be used.

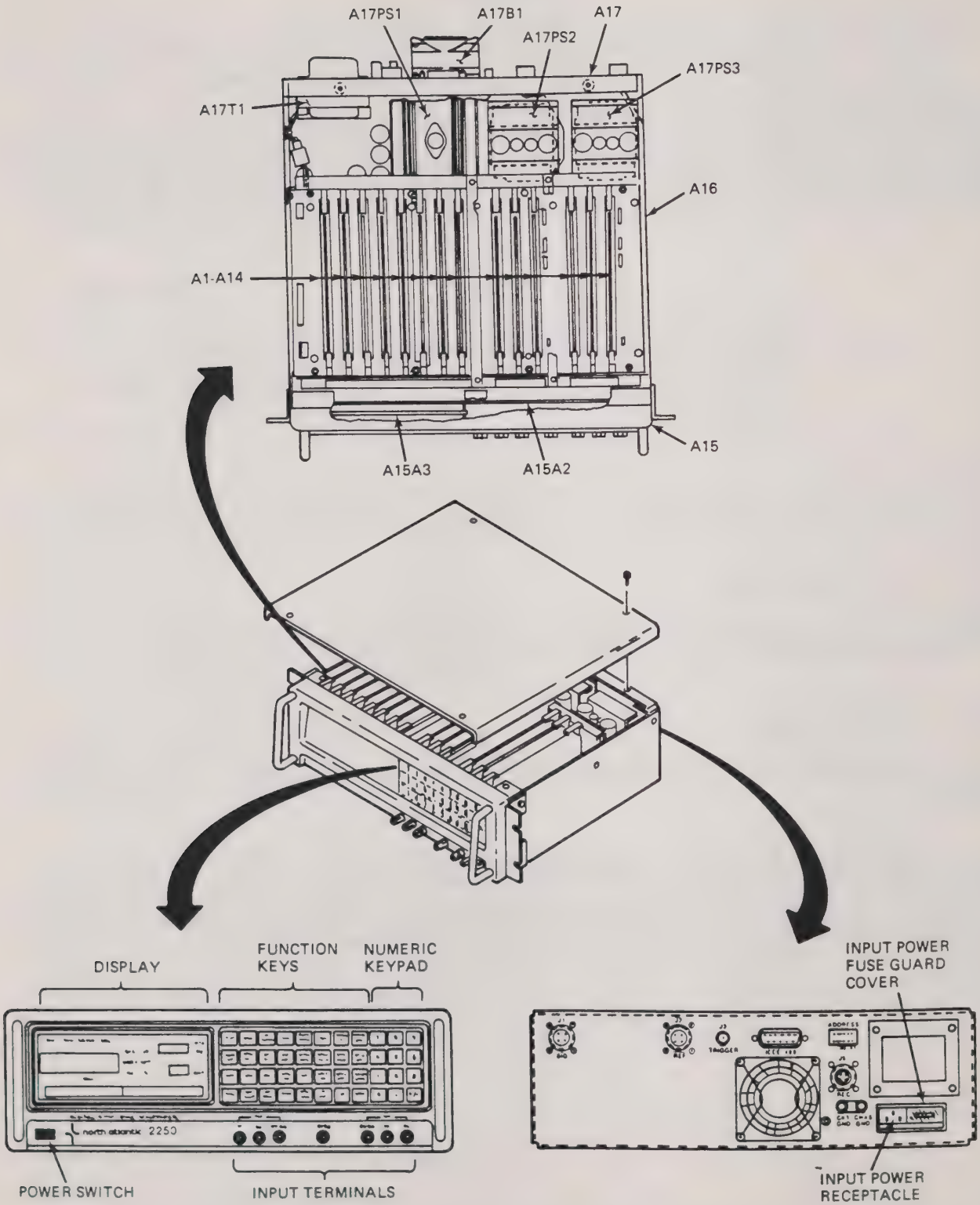


Figure 1-2. DAV Details

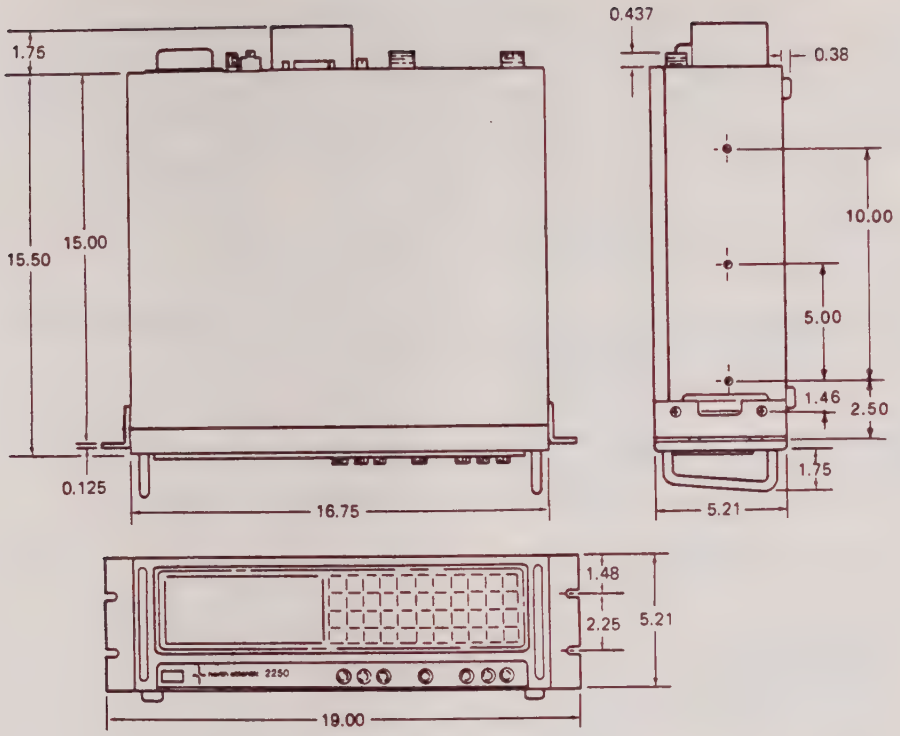


Figure 1-3. DAV 2250 Outline and Dimension Drawing Showing Mounting Details

Table 1-4. DAV, Major Assemblies

REF DES	NAME	PART NO.	SCHEMATIC NO.	CURRENT REVISION
A1	Microprocessor Circuit Card Assembly (CCA)	787170	768861	F
A2	Memory CCA	787171-3	768880-3	B
A3	I/O CCA	787172-2	768882-2	D
A4	Timing and Control CCA	787173-1	768879-1	E
A5	Phase Locked Loop CCA	787192-1	768878-1	E
A6	Signal Accumulator CCA	787193-1	768865-1	A
A7	Reference Accumulator CCA	787193-1	768865-1	A
A8	AutoCal CCA	787274-2	768877-2	A

Table 1-4. DAV, Major Assemblies (Continued)

REF DES	NAME	PART NO.	SCHEMATIC NO.	CURRENT REVISION
A9	Reference A/D Converter CCA	787664	768987	D
A10	Reference Filter CCA	787176-1	-	B
A11	Reference Front End CCA	787505-1	768930-1	E
A12	Signal A/D Converter CCA	787664	768987	D
A13	Signal Filter CCA	787176-1	-	B
A14	Signal Front End CCA	787505-1	768930-1	E
A15	Front Bezel Assembly	787198	*	G
A15A1	Keyboard	298051-3	298051-3	A
A15A2	Display Driver CCA	787179	768862	D
A15A3	Display CCA	787178	768864	D
A15A4	Signal Isolation Assembly	787448-1	768910	D
A15A5	Reference Isolation Assembly	787448-2	768910	D
A16	Chassis Assembly	787197	*	D
A16A1	Motherboard	787177	768866	J
A17	Rear Panel Assembly	787277	*	D
A17A1	Recorder Filter Assembly	787667	768983	A
A17PS1	Main Power Supply Assembly	787181	768863	H
A17PS2	Reference Isolated PS Assembly	787313-1	768876-1	A
A17PS3	Signal Isolated PS Assembly	787313-1	768876-1	A
A17T1	Main Transformer Assembly	787314	*	D

*Electrical interconnections between major assemblies of the DAV chassis are detailed in Interconnection Diagram 768928.

Table 1-5. Specifications

ITEM	SPECIFICATIONS
Voltage range	20 mV to 500 V* rms full scale in six ranges.
Maximum signal input	500 V rms ±400 V dc, total of 700 V peak maximum.
Reference voltage range	2 mV to 500 V* rms, autoranging (no adjustment necessary); ±400 V dc, total of 700 V peak maximum.
Signal autoranging	Upranges at approximately 109% of range. Downranges at approximately 10% of range.
Ratio autoranging	Upranges at 160% of range. Downranges at 10% of range.
Display	0.56-inch LED main display.
Voltage	4-1/2 digits, 0.005% full range resolution.
Phase	+0.00° to +359.99° phase lead, 0.01° resolution or 0.00° ±180° 0.01° resolution.
Frequency range, all modes	10 Hz to 100 kHz.
Warmup time	30 minutes, for rated accuracy. (Depress "CAL" switch after warmup period.)
Voltage and ratio accuracy**	Specified at 23° ±5°C ambient temperature.

NOTE

Calibration for ten operating frequencies and the TOTAL (AVG) mode may be stored in nonvolatile memory. Refer to Model 2250 Instruction Manual.

*500 V range is actually a 2000 V range with maximum signal limitations of 500 V. Use "2000 V full scale" figure to calculate accuracy specification. DO NOT apply voltages in excess of 500 V.

**Phase sensitive measurements are also affected by phase angle specifications. TOTAL (Sum) mode voltage and ratio specifications apply within autorange limits only. 35 uV TOTAL mode noise specification alters TOTAL mode voltage and ratio accuracy limits on signals of less than 20 mV.

Table 1-5. Specifications (Continued)

ITEM	SPECIFICATIONS	
TOTAL (Sum), FUND, and PHASE sensitive modes	200V Range and 500V Range (% Full Scale + % Reading)	All Other Ranges (% Full Scale + % Reading)
10 Hz to 30 Hz	±0.1% FSC + 0.1% rdng	±0.1% FSC + 0.05% rdng
>30 Hz to 1.5 kHz	±0.05% FSC + 0.1% rdng	±0.05% FSC + 0.05% rdng
>1.5 kHz to 5 kHz	±0.06% FSC + 0.12% rdng	±0.06% FSC + 0.06% rdng
>5 kHz to 20 kHz	±0.06% FSC + 0.21% rdng	±0.06% FSC + 0.12% rdng
>20 kHz to 32 kHz	±0.12% FSC + 0.34% rdng	±0.12% FSC + 0.19% rdng
>32 kHz to 54 kHz	±0.12% FSC + 0.8% rdng	±0.12% FSC + 0.50% rdng
>54 kHz to 100 kHz	±0.12% FSC + 1.2% rdng	±0.12% FSC + 0.75% rdng

Total (AVG) Mode

TOTAL (Avg)	0 to 1/2 Scale	1/2 Scale to FSC
10 Hz to 26 Hz	0.25% FSC	0.5% reading
26 Hz to 10 kHz	0.125% FSC	0.25% reading
10 kHz to 30 kHz	0.25% FSC	0.5% reading
30 kHz to 100 kHz	0.50% FSC	1.0% reading

Ratio modes

Reference input voltage:
2 mV rms to 500 V rms continuous.

Ratio Range	Full Scale Ratio	Autorange Uprange Point	Maximum Display
.01 R	10.000 x 10^{-3}	16.000	99.999 x 10^{-3}
.1 R	100.00 x 10^{-3}	160.000	999.99 x 10^{-3}
1 R	1.0000	1.6000	9.9999
10 R	10.000	16.000	99.999
100 R	100.00	160.000	999.99
1000 R	1000.0		9999.99

NOTE

Display indicates "SCALE" to indicate excessive ratio when not in autoranging mode. Signal and reference voltage ranges always autorange when in ratio mode.

Table 1-5. Specifications (Continued)

ITEM	SPECIFICATIONS
Ratio accuracy	@23° ±5°C ambient temperature where: V ref = The actual voltage applied to the REF input. (This may be displayed by going out of Ratio mode and into TOTAL and READ REF.) V rng = The reference voltage range (in volts) being used. (This range is annunciated when the reference voltage is read as described above.) R rng = ratio range R = ratio tolerance

TOTAL (Sum), FUND, IN PHASE and QUAD	200 V Range and 500 V Range	All Other Ranges
10 Hz to 30 Hz	$R = (0.0010\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.00010 x Reading	$R = (0.0010\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0005 x Reading
>30 Hz to 1.5 kHz	$R = (0.0005\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.00010 x Reading	$R = (0.0005\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0005 x Reading
> 1.5 kHz to 5 kHz	$R = (0.0006\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.00012 x Reading	$R = (0.0006\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0006 x Reading
> 5 kHz to 20 kHz	$R = (0.0006\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0021 x Reading	$R = (0.0006\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0012 x Reading
>20 kHz to 32 kHz	$R = (0.0012\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0034 x Reading	$R = (0.0012\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0019 x Reading
>32 kHz to 54 kHz	$R = (0.0012\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0080 x Reading	$R = (0.0012\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0050 x Reading
>54 kHz to 100 kHz	$R = (0.0012\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0120 x Reading	$R = (0.0012\ R_{rng})\ \frac{Vrng}{Vref}$ + 0.0075 x Reading

Table 1-5. Specifications (Continued)

ITEM	SPECIFICATIONS
Orthogonality	
10 Hz to 30 Hz	±0.10°
>30 Hz to 5.0 kHz	±0.05°
> 5.0 kHz to 100 kHz	$\pm\frac{f(\text{in kHz})^\circ}{100}$
0 Volt input accuracy	Equal to full scale accuracy spec.
Total mode noise, 20 mV range	35 V maximum
Nulling sensitivity	1 μV
Phase angle accuracy	Accuracy specifications apply in "Autorange" only.
10 Hz to 30 Hz	±0.10°
>30 Hz to 5 kHz	±0.05°
> 5 kHz to 100 kHz	$\pm\frac{f(\text{in kHz})^\circ}{100}$ degrees
Harmonic rejection	2nd Harmonic: -60 dB
(Fundamental and phase sensitive modes)	3rd Harmonic: -80 dB All higher order harmonics at fundamental frequency of 400 Hz: -86 dB
Total harmonic distortion (THD)	
Frequency of fundamental	Harmonics evaluated:
10 Hz to 3.16 kHz	2nd to 30th
3.16 kHz to 10.6 kHz	2nd to 10th
10.6 kHz to 28.5 kHz	2nd and 3rd
28.5 kHz to 100 kHz	None

Table 1-5. Specifications (Continued)

ITEM	SPECIFICATIONS
THD Accuracy (For fundamental frequency of 10 Hz to 10 kHz)	For readings 2%: ± 0.015 x Reading For readings <2%: ± (0.03 + 0.015 x *VSCALE / ERMS) where VSCALE is the voltage scale annunciated ERMS is the signal voltage
THD range of evaluation	0.00% to 999.99%
THD method of evaluation	The 2250 DAV evaluates THD relative to the fundamental by using the harmonics evaluated at the frequency of interest in accordance with the table above and the following formula:
THD formula	$THD = \frac{\sqrt{(Ef2)^2 + (Ef3)^2 + \ldots(Efn)^2}}{Ef1}$ where: Ef1 = true rms voltage of fundamental. Ef2 = true rms voltage of the second harmonic. Efn = true rms voltage of the highest harmonic evaluated for that particular fundamental frequency, per table above.
THD display	THD may be displayed as percent or in decibels relative to the fundamental.
Random Noise measurement in THD mode	Excluded, as it is not an element of TOTAL HARMONIC DISTORTION.

*See "Harmonics Evaluated" above. Measurements of signals containing high amplitude harmonics of higher orders than those evaluated may incur additional error.

Table 1-5. Specifications (Continued)

ITEM	SPECIFICATIONS
Harmonic phase:	
Method of measurement	The phase of the selected harmonic component is measured relative to the fundamental of that signal. In READ REF mode, phase angle of the selected harmonic component of the reference is measured relative to the fundamental component of the reference. For example: The measure of phase angle displayed is relative to the harmonic signal. That is, 60° of the third harmonic is equal to 20° relative to the fundamental. This is because 360° of the fundamental equals 3 cycles or 1080° of the third harmonic.
Accuracy	The phase accuracy (related to the phase of the fundamental) is n times the fundamental phase specification, where n equals the harmonic order.
Harmonic amplitude	Harmonic amplitude accuracy is equal to the fundamental accuracy specification times n, where n equals the harmonic order.
Filters	The signal and reference channel precision filters allow signals rich in harmonics (including square waves) to be evaluated for fundamental frequency phase-sensitive parameters.
Filters switched in	Filters are automatically switched in when in "FUND", "IN-PHASE", "QUAD", and "PHASE ANGLE" modes.
Filters switched out	Filters are automatically switched out when in "TOTAL" or "THD" modes and during all harmonic measurements.
Frequency readout accuracy:	
10 Hz to 100 Hz 100 Hz to 100 kHz	±2% ±0.5%
SIG input impedance REF input impedance	2 Megohms shunted by 180 pf (typical). 2 Megohms shunted by 180 pf (typical).

Table 1-5. Specifications (Continued)

ITEM	SPECIFICATIONS
Common mode rejection (20 mV range, zero source impedance)	
10 Hz to 999 Hz	126 dB minimum
1 kHz to 5 kHz	110 dB minimum
>5 kHz to 32 kHz	100 dB minimum
>32 kHz to 54 kHz	91 dB minimum
Trigger input	TTL compatible input, negative edge triggered. Minimum pulse width is 30 nS.
Recorder output (16 BIT)	Separate inphase and quadrature outputs are provided.
Range	Full scale equals ±2.00 V dc. (8.75 V optional, see Instruction Manual.)
Accuracy	±.05% of full scale added to specification for mode, range, and frequency.
Resolution	1 mV nominal.
Power requirements	115/230 V rms ±15%, 47 to 67 Hz, 30 VA
Fuse	2 A for 115 V operation. 1 A for 230 V operation
Connectors on DAV	Type
Front SIG input	5 way binding posts
Front REF input	5 way binding posts
Rear SIG input	MS3102A14S-2P
Rear REF input	MS3102A14S-2P
Trigger input	BNC female
Recorder output	MS3102A14S-2S
Remote Interface	IEEE-488 standard connector
Power input	IEC standard 115/230 V connector
Operating Position	Horizontal
Maximum tilt angle	±30°
Dimensions	5-1/4"H x 16-3/4"W x 19"D
Weight	35 pounds (15.9 kg)

Table 1-6. Special Tools and Test Equipment

EQUIPMENT	MANUFACTURER	MODEL NO.
Thermal RMS Digital Multimeter with Ohms Converter (DMM, ac Voltmeter)	Fluke	8506A with option 02A
Oscillator (Variable Signal Source)	Krohn-Hite	4000A
Amplifier	Krohn-Hite	7500
Oscilloscope	Tektronix	465
Distortion Analyzer	Krohn-Hite	6900A
Ratio Box (Low Frequency Ratio Box)	Ailtech/Gertsch	RT-20R
Hypot	Associated Research	412
Megohmmeter	Freed Transformer	1620
Extender Card	NAI	787731
High Frequency Ratio Transformer (High Frequency Ratio Box)	Dytronics	RT501
2 MHz Variable Phase Synthesizer (Phase Generator)	Wavetek	650
IEEE Controller including ROM Drawer including I/O ROM Advanced Program (PRGM) HP-IB Interface (Controller)	Hewlett-Packard	HP-85B 82936A 00085-15003 00085-15005 82937A
Stop Watch		Commercial
AC Voltage Standard	Electronic Development Corp.	4600
High Resolution Timer Counter (Frequency Counter)	Philips	PM6670
AC Voltage Calibrator (Alternate Variable Signal Source)	Fluke	5200

SECTION 2

THEORY OF OPERATION

2-1. INTRODUCTION.

This section contains a description of DAV operating principles which are discussed at two levels. The first level presents an overall description of DAV operation and is supported by an overall block diagram. The second level, a more detailed description of DAV circuit interrelationships, is referenced to functional block diagrams. Detailed functional signal flow diagrams are provided for each circuit board.

2-2. SIGNAL CONVENTION AND SYMBOLOGY.

Signal names appearing on the diagrams within this section are represented, for the most part, by mnemonics that describe the respective signal functions. Although each signal is described the first time it appears, all signal mnemonics and other abbreviations that are mentioned also appear in Appendix A of this volume for easy reference.

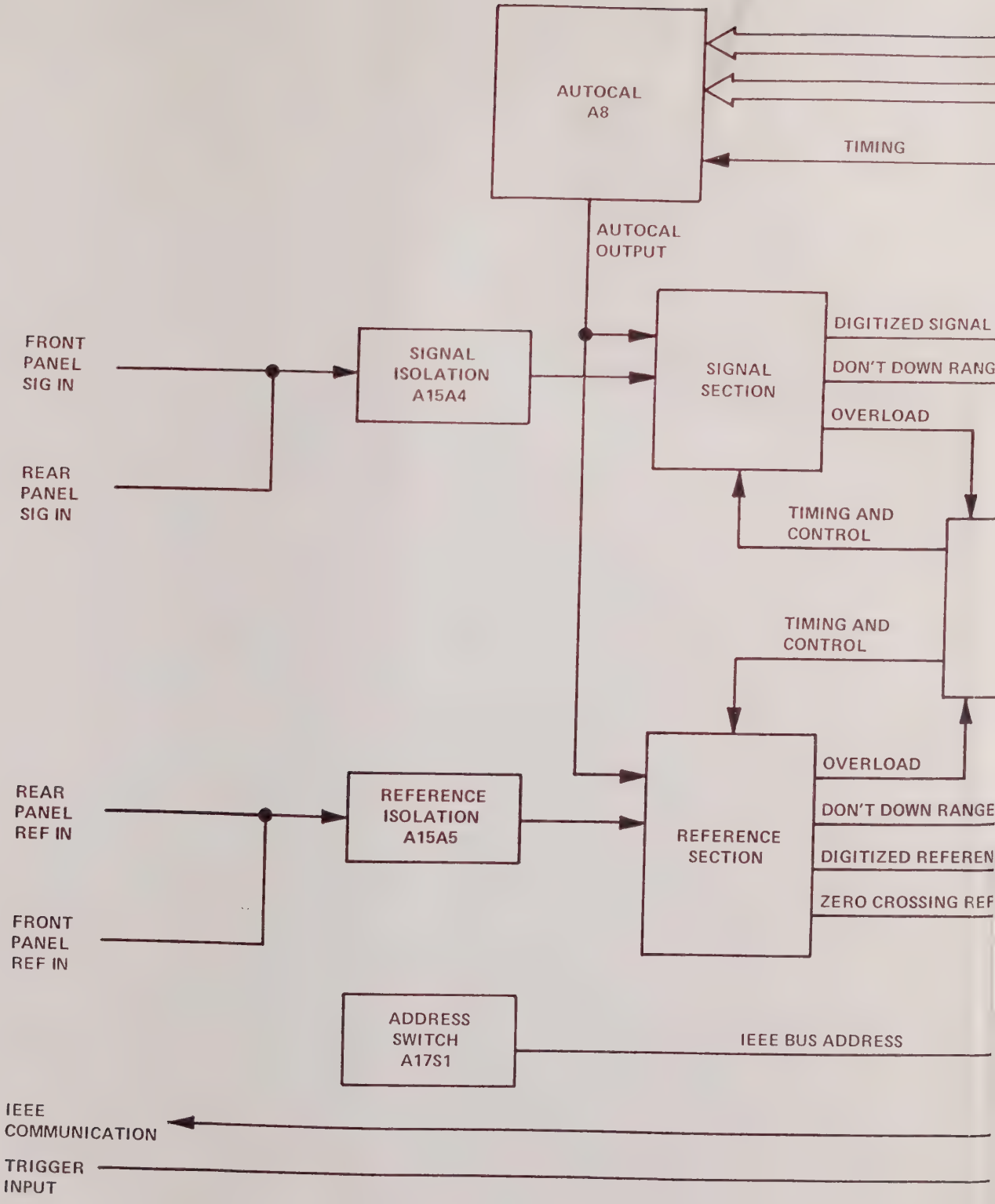
2-3. OVERALL BLOCK DIAGRAM DESCRIPTION. (See figure 2-1.)

The DAV is a microprocessor (uproc) - based multifunction instrument that performs phase sensitive voltage measurements, ratio measurements, and signal analysis over the frequency range of 10 Hz to 100 kHz. The DAV implements these functions by using data sampling techniques to extract the desired information from the input signal under control of operator-initiated commands from the front panel keyboard. This information is processed using a discrete Fourier transform (DFT) calculation to yield magnitude, phase, and harmonic data. In addition, by means of a hardware multiplier/accumulator, the raw sampled data is continuously averaged, thereby enhancing measurement resolution and accuracy.

As a laboratory instrument, the DAV provides the user with a means of measuring and analyzing an input signal. These functions are achieved by a microprocessor which controls signal processing and interfaces with the user front panel keyboard and displays. Changes to the DAV operating mode are initiated by pressing a keyboard key to select the type of signal analysis desired, such as voltage measurements in the TOTAL, FUNDamental, IN PHASE, or QUADrature modes; voltage gain/loss measurements in dB; phase shift (PHASE ANGLE) measurements; total harmonic distortion (THD) measurements; etc.

Keyboard input information is read by the microprocessor which uses this information to modify signal analysis computations accordingly. After the microprocessor performs the necessary DFT and analysis calculations based on user inputs, the resultant signal data is then transferred to the display for user monitoring purposes.

When the DAV is used as a remote instrument in an automated test system serviced by an IEEE-488 interface, the DAV bus address is physically set by the DIP switch on the rear panel, and commands and data transfers between the DAV and external IEEE-488 data bus are remotely selected and controlled.


AUTOCAL
A8
TIMING
AUTOCAL
OUTPUT
FRONT
PANEL
SIG IN
REAR
PANEL
SIG IN
SIGNAL
ISOLATION
A15A4
SIGNAL
SECTION
DIGITIZED SIGNAL
DON'T DOWN RANG
OVERLOAD
TIMING AND
CONTROL
TIMING AND
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REAR
PANEL
REF IN
FRONT
PANEL
REF IN
REFERENCE
ISOLATION
A15A5
REFERENCE
SECTION
OVERLOAD
DON'T DOWN RANGE
DIGITIZED REFEREN
ZERO CROSSING REF
ADDRESS
SWITCH
A17S1
IEEE BUS ADDRESS
IEEE
COMMUNICATION
TRIGGER
INPUT

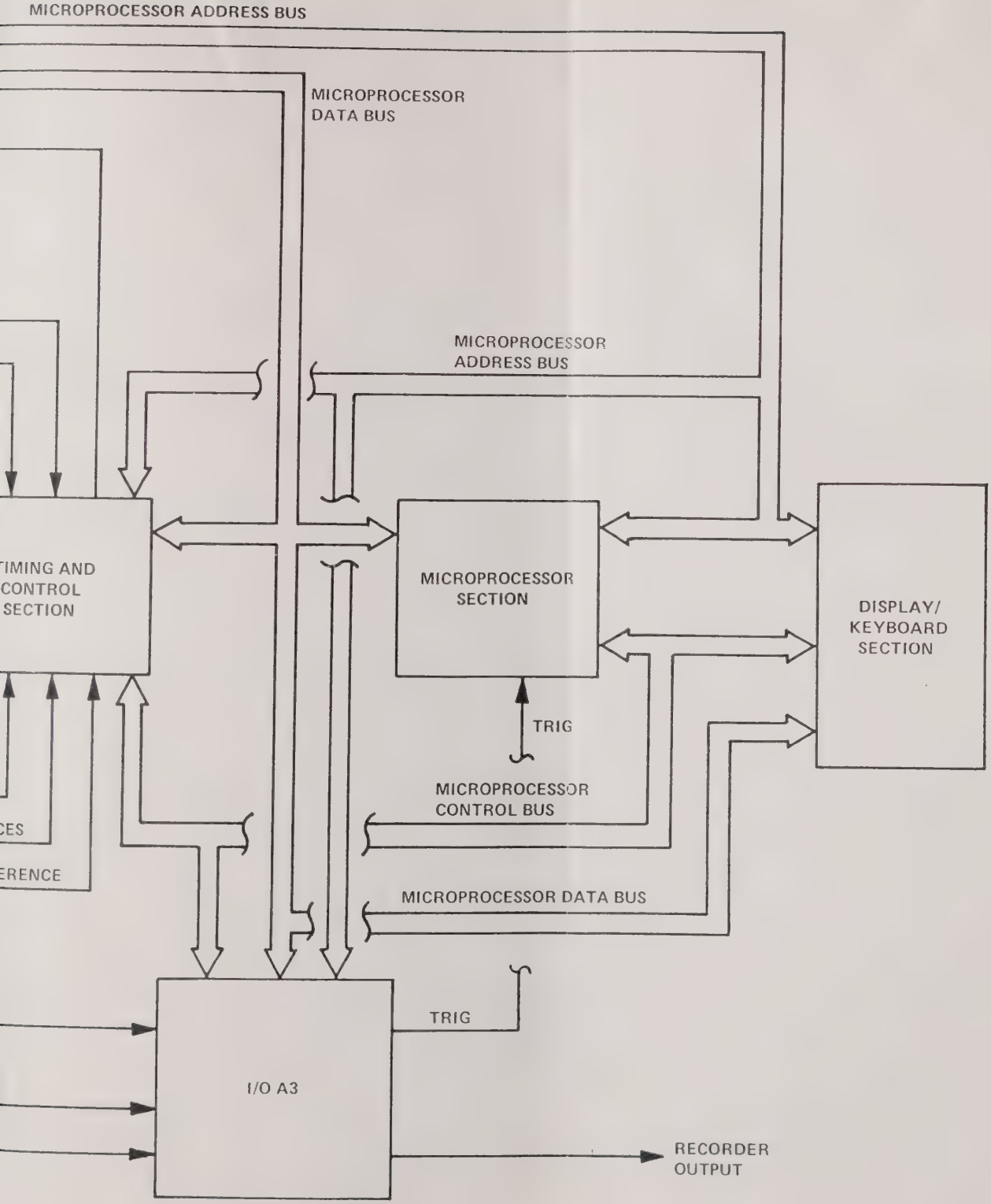


Figure 2-1. DAV, Overall Block Diagram

As shown in figure 2-1, the DAV is organized into functional sections that provide signal and reference input conditioning; timing and control; microprocessor-controlled data acquisition and storage, internal data communication, and DFT and analysis calculations; input/output (I/O) interface control for communication between an external IEEE-488 bus and the microprocessor; a display function for converting processed data to the required display formats; an autocalibration function that permits detection and characterization of errors in the signal and reference sections to produce phase/amplitude correction data for subsequent signal measurement calculations; and a keyboard function that permits operator interface with, and selection and control of, signal measurement modes and parameters.

a. MICROPROCESSOR SECTION.

The microprocessor section consists of microprocessor board and memory board. The microprocessor board itself contains a 16-bit microprocessor operating at 8 MHz and the required external logic for interrupt, address bus, data bus, and data transfer control. All required memory is contained on memory board A2, which includes 64 kilobytes of programmable read-only-memory (PROM) and 32 kilobytes of random access memory (RAM). Although responsible for data acquisition, keyboard, display, and I/O functions, the microprocessor controls these asynchronous tasks by passing data to independently operating hardware. The autocalibration function is accomplished by controlling the Autocal board A8 as an output port. The majority of processing time is occupied by calculating DFTs and display data in response to operator mode/control inputs from the keyboard. Program elements are stored in the PROM of memory board.

b. SIGNAL AND REFERENCE SECTIONS.

The signal and reference sections of the DAV are identical, with each consisting of a front end board, filter board, and analog-to-digital (A/D) converter board. The signal to be measured and/or analyzed can be supplied to the respective SIG or REF HI-LO-GUARD binding posts on the front panel, or to the SIG or REF connector J1 or J2 on the rear panel. In either case, the signal and reference inputs are supplied to the desired signal or reference sections of the DAV via respective isolation modules A15A4 and A15A5 when the measurement mode is active, and autocalibration mode has not been selected by the operator.

In the signal section, the input level or waveform is amplified, filtered, sampled by means of a track/hold amplifier, and then digitized by a high-speed A/D converter. This process also occurs simultaneously in the reference section and results in data samples that represent the amplitude of the incoming waveforms at discrete points in time. Sixty-four (64) samples-per-cycle are obtained when the incoming signal frequency is 3.16 kHz or less; at higher frequencies, the number of samples-per-cycle is reduced and the number of cycles over which data is examined is increased, so that the DFT is always performed on 64 data samples.

Operation of both the signal and reference sections is managed by timing and control signals which are isolated from other internal logic using optical isolation.

The signal and reference filter boards, which function within the signal path of the front end board, receive respective signal outputs from the front end board, and are active when in the FUND, QUAD, IN PHASE, and PHASE ANGLE modes. When this is the case, the filter board is programmed to a frequency appropriate to the signal being measured or to the frequency preset by user input.

The front end boards also monitor the magnitude of the amplified input signals for two specific conditions: overload, and ok-to-downrange. When an overload condition is present, due to excessive high positive or negative voltages, an overload is generated and communicated to the microprocessor through the timing and control section. Similarly, when the incoming signal magnitude is too great for the next lower measurement range, a don't-down-range signal is produced and communicated to the microprocessor through the timing and control section to prevent automatic selection of a lower measurement range.

The amplified signal from the front end board is supplied to the A/D converter board where it is attenuated, sampled by a track/hold amplifier and applied to an A/D converter. When operating in TOTAL (AVG) mode the signal is routed through the TOTAL (AVG) rectifier where it is converted to a dc voltage proportional to the rms amplitude of a sine wave. The A/D converter performs a 12-bit successive approximation conversion process on the analog signal that is held at the output of the track/hold amplifier. The result, which is applied to the timing and control section, is a serial data representation of the analog signal. A secondary output from the reference front end board is also supplied to the A/D converter board to produce a zero-crossing timing reference which is supplied to the timing and control section.

c. TIMING AND CONTROL SECTION.

The timing and control section consists of the timing and control board, signal and reference accumulator boards, and the phase locked loop (PLL) board. The timing and control board, in conjunction with the two accumulator boards, functions to control data acquisition, average the data, and make this data available to the microprocessor data bus. The PLL board receives the zero crossing reference signal from the A/D converter in the reference section, and provides selection of this signal (or the autocalibration signal, during autocalibration mode) to provide synchronization for the data acquisition and sampling process. Once locked to the frequency under consideration, a lock indication bit is produced and transferred to the data bus for program use. The PLL board also provides an output frequency multiplied by a factor of 64 or 16. This output is applied to the timing and control board where it is used to generate the sample clock for synchronization of the entire data acquisition process. On the timing and control board a division process occurs to the output from the PLL board which determines the proper number of samples per input cycle. Data at frequencies below 3.16 kHz are sampled over a one-cycle period, and those above 3.16 kHz are sampled over multiple cycles to yield a total of 64 data samples in all cases.

The timing and control board contains address decoding and data latches for system control ports. Most hardware functions of the DAV are controlled through these ports. The timing and control board contains a state machine circuit which controls the data acquisition process. It generates the necessary timing and control commands to hold data at the track/hold amplifier, start conversion at the A/D converter, and circulate data through the hardware multiplier/accumulator. In addition, the timing and control board generates accumulator RAM addresses to put each of the 64 data samples in their proper accumulator RAM locations.

During the data acquisition process, the serial data from the signal and reference A/D converters is applied to the accumulators. For the first set of measurements in a data acquisition sequence, the first 64 data samples are loaded into RAM locations set aside for these samples. All subsequent samples are accumulated by dividing the

incoming sample by 16 and adding the result to 15/16th of the value of the previous sample. This accumulated result is carried out to 16 bits and replaces the corresponding previous sample in RAM. When the data acquisition and processing for each sample is finished, the microprocessor is permitted to read data from the accumulator dual ported RAM. It is this data upon which the microprocessor performs the required calculations for magnitude and phase angle using DFT algorithms.

Each accumulator board also contains an overload detector port which receives signal and reference overload and don't-down-range signals, performs logic functions on these signals, and makes them available to the microprocessor.

d. DISPLAY/KEYBOARD FUNCTION.

The display function consists of the display driver board, keyboard, and the display board. The display driver board contains the driver logic for the alphanumeric and discrete LED displays on the display board and the keyboard. The display driver board is a synchronous peripheral device which decodes addresses and performs a handshake interface with the microprocessor.

The keyboard is a 4 x 11 switch matrix with associated LEDs. Whenever a keyboard key is pressed, the peripheral interface adapter (PIA) logic generates an interrupt, provided the PIA is enabled and this interrupt is sent to the microprocessor function. A keyboard interrupt service routine will determine which key is pressed and alter DAV operation accordingly.

e. I/O FUNCTION.

The I/O function is contained on the I/O board A3 which provides communication between the microprocessor data bus and an external IEEE standard 488 interface bus. Information is exchanged by means of an IEEE 488 general purpose interface bus (GPIB) controller. This controller is also considered a synchronous peripheral device by the microprocessor and, as such, communicates with the microprocessor using handshake signals similar to those for the timing and control section and the display function.

Data and control lines for the IEEE 488 interface are connected to IEEE 488 connector J4 on the rear panel of the DAV. Similarly, dip switch A17S1 (ADDRESS) on the rear panel provides a means of selecting the DAV address for IEEE 488 communication. In addition, the rear panel contains TRIGGER BNC connector J3 for application of an external trigger to the DAV for purposes of generating an IEEE bus service request (SRQ) and for track/hold mode display update.

The I/O board also contains two 16-bit multiplying digital-to-analog D/A converters (DAC) that receives data from the microprocessor which is equivalent to that used for the DAV front panel in-phase and quadrature readouts and converts these to dc voltages. The in-phase and quadrature analog (dc) outputs are supplied to the recorder (REC) connector J5 on the rear panel.

f. AUTOCALIBRATION FUNCTION.

The autocalibration function is controlled by the microprocessor and uses the autocal board A8 which may be set to the frequency currently being measured, or to the frequency preset by the FREQ pushbutton on the front panel keyboard. Calibration is initiated by pressing the keyboard CAL pushbutton. When this occurs, the

measurement signal and reference inputs to the front end board are disconnected by the input isolation relays which, in turn, connect the signal input paths to the output from the autocalibration board. During autocalibration sequence, the autocalibration board generates an output sinewave signal in the frequency range from 10 Hz to 100 kHz, and an auxiliary squarewave output, synchronized with the sinewave. Control of the autocalibration function is achieved by three timing signals from the timing and control section, and by frequency and amplitude information communicated through the data bus.

2-4. DAV PROGRAM SOFTWARE. (See figure 2-2.)

Figure 2-2 illustrates the initialization and main program loops executed by the microprocessor in the logical management of DAV operational functions. Upon initial turn-on, the microprocessor calculates and displays the checksum, thereby testing the internal PROMs. The microprocessor reads all of the data in the PROMs and calculates the sum of this data to come up with a number. This number is displayed on the front panel as the checksum and tells what revision of software is in the unit.

Next the hardware is initialized. This consists of writing to the registers in the peripheral interface (PIA) adapter on display driver board A15A2, writing to the registers on I/O board A3, and writing to the timer registers on timing and control board A4 that are used to measure frequency. This sets all of these registers to their initial conditions. A check is then performed to see if the front panel key strokes from the last time the DAV was powered up are in memory. This is accomplished by looking at a specific location in memory to see if data normally stored there is present. If the data is not present (the no path on figure 2-2), the software assumes that all previous front panel memory is no longer present, and sets the unit to built-in default values. If the data is present (the yes path on figure 2-2), the software proceeds to initialize the displays by setting all keyboard indicators and annunciators to initial conditions based on the previous setup.

The above initialize sequence is only performed once, upon cold start at power turn-on. After this sequence, the DAV software enters the "main loop" sequence. The first thing that occurs is a check to determine if the dip switches that enable a self-check are active. If yes, the DAV performs a self-test sequence. If no, the frequency counter is started. Following this, a major subroutine, data acquisition, makes sure that the phase-locked loop circuits have acquired phase lock and that the analog-to-digital converter does a conversion, gets data from the analog-to-digital converter by way of the hardware averaging accumulator, and stores the data in memory.

Following the data acquisition routine, data calculation subroutines are performed. These calculate the actual numbers from the raw data stored in memory, using the DFT, to be read out to the display. The software then checks to see if the frequency counter is done. If the frequency counter is not done, the program branches back to the beginning of the main loop and another data acquisition sequence is performed. If the frequency counter is done, a check is performed to see if the unit is able to measure the frequency. If the frequency cannot be measured, a no-lock indication is forced and the software branches back to the start of the acquisition section of the main loop. If the frequency can be measured, it is displayed on the front panel. The frequency measurement that was just made is compared with the band that was selected for the phase-locked loop to determine if the phase-locked loop is set to the proper band. If not, a no-lock indication is forced again and the software branches to the

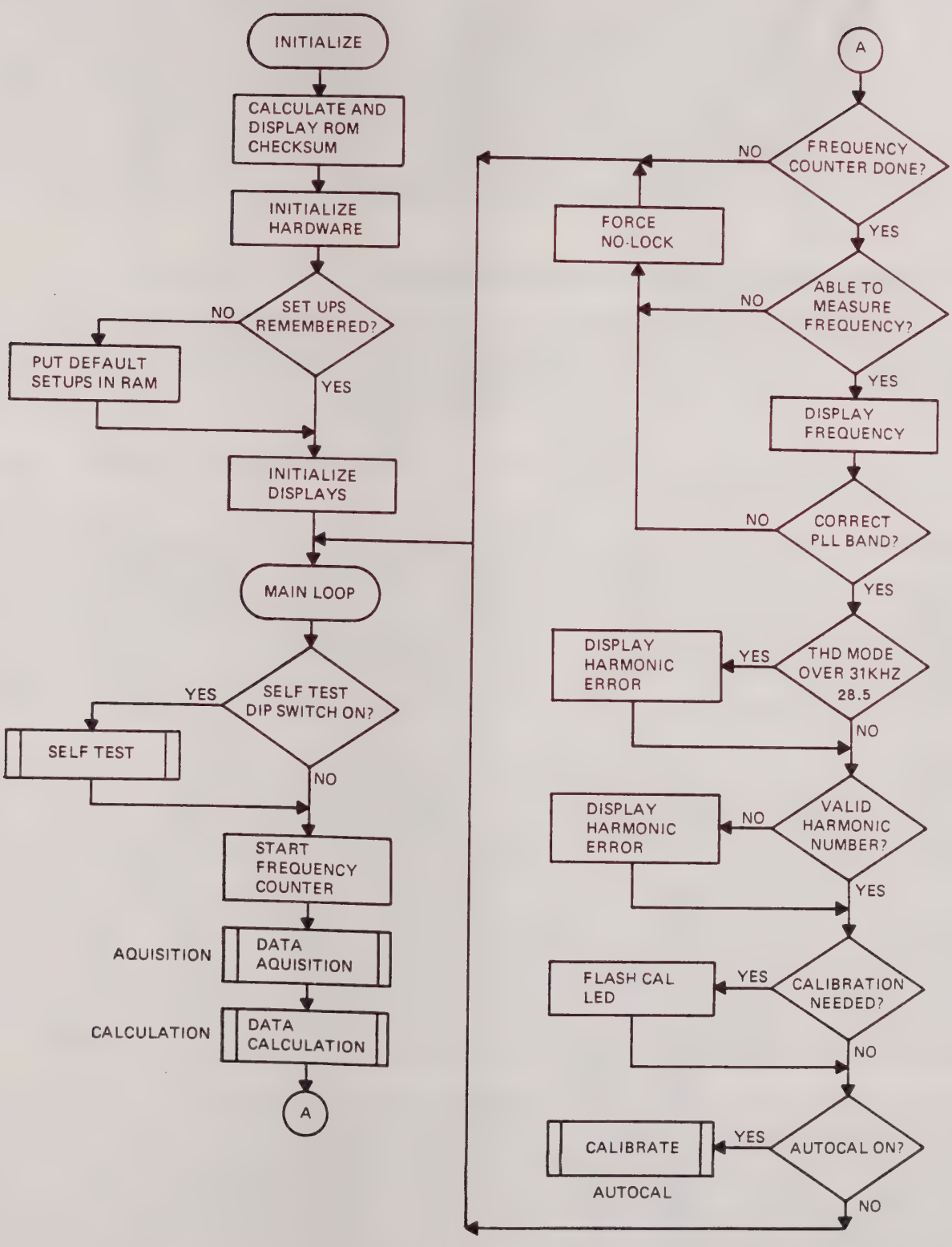


Figure 2-2. DAV Program Flow Chart

start of the acquisition section of the main loop. At this point, a group of error and mode checks are performed. Since THD is not allowed above 28.5 kHz, an error display is obtained if THD mode is set above that value. If THD mode is set below 28.5 kHz, the THD value is displayed. When the DAV is analyzing a harmonic and a valid harmonic number is not obtained, an error is displayed. If the harmonic number is valid, the unit determines if calibration is needed. If calibration is needed, the front panel CAL indicator flashes. The unit checks to see if autocal is on. If autocal is on and the frequency has changed by more than 5 percent from the calibration factors stored in the memory, the calibration sequence is initiated. If autocal is not on, or if not required, the software then goes back and repeats the main loop sequence.

2-5. MICROPROCESSOR SECTION FUNCTIONAL DESCRIPTION. (See figure 2-3.)

The microprocessor function consists of microprocessor board A1 and memory board A2. Its purpose is to control overall DAV operation by means of a software program that interrogates and monitors DAV operational status conditions; initiates data acquisition; performs DFT calculations; and enables display of the resultant information to the user.

a. MICROPROCESSOR BOARD A1. (See figure 2-4 for details of functional signal flow on Microprocessor board A1.)

Microprocessor board A1 contains a 68000 microprocessor having asynchronous 16-bit data and 24-bit address buses. As shown on figure 2-3, the address bus output consists of bits AB1-23; the 24th bit, AB0, is determined by which data byte -upper or lower- of a 16-bit word is to be written to, or read from. For the upper data byte, internal address bit AB0 is zero (0), and the upper data strobe ($\overline{UDS}$) is issued; for the lower data byte, internal address bit AB0 is a one (1), and the lower data strobe ($\overline{LDS}$) is issued. Thus, only even addresses are word (16-bit) locations and all addresses may be used to access individual byte (8-bit) locations.

I/O board A3, autocal board A8, display driver board A15A2, and part of the timing and control board A4 operate as external synchronous peripheral devices. To provide synchronous data transfer operation, the 68000 microprocessor operates in a mode identical to a 6800 type microprocessor using three signals; namely, enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). This latter signal is generated internally by decoding the microprocessor status, address strobe ($\overline{AS}$), and a signal called $\overline{6800}$ which is returned by the synchronous peripheral when addressed. The memory board A2, accumulators A6/A7, and timing and control board A4 operate as asynchronous 68000 peripherals using the read/write (R/$\overline{W}$), address strobe ($\overline{AS}$), and data transfer acknowledge ($\overline{DTACK}$) signals. A read or write cycle is initiated when the microprocessor places an address on the address bus, asserts the address strobe ($\overline{AS}$) and asserts the read/write enable (R/$\overline{W}$). The data transfer is completed when the addressed device asserts data transfer acknowledged ($\overline{DTACK}$).

When an interrupt is received, the microprocessor determines the interrupt level, and compares it to the internal interrupt mask. If the interrupt level is greater than the interrupt mask, the microprocessor places the interrupt level on address bus lines AB1-3, and sets the internal function code to interrupt request acknowledge ($\overline{IRQACK}$). The address strobe ($\overline{AS}$) is then asserted, followed by the upper and lower data strobes ($\overline{UDS}$, $\overline{LDS}$), which are used only for memory board A2. The interrupt request acknowledge status is decoded to assert the $\overline{VPA}$ input to the microprocessor, thus enabling the microprocessor to fetch an interrupt vector for

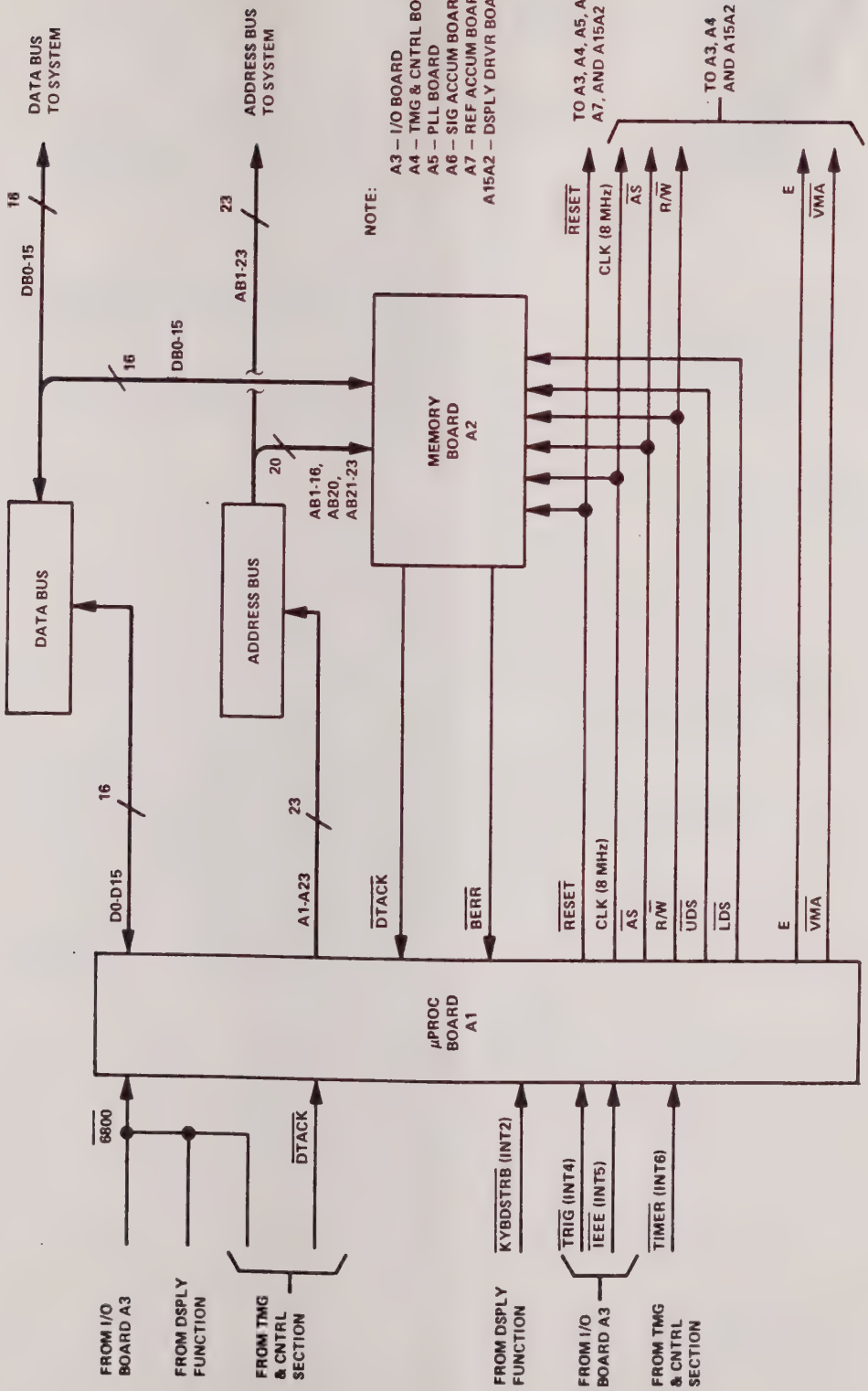
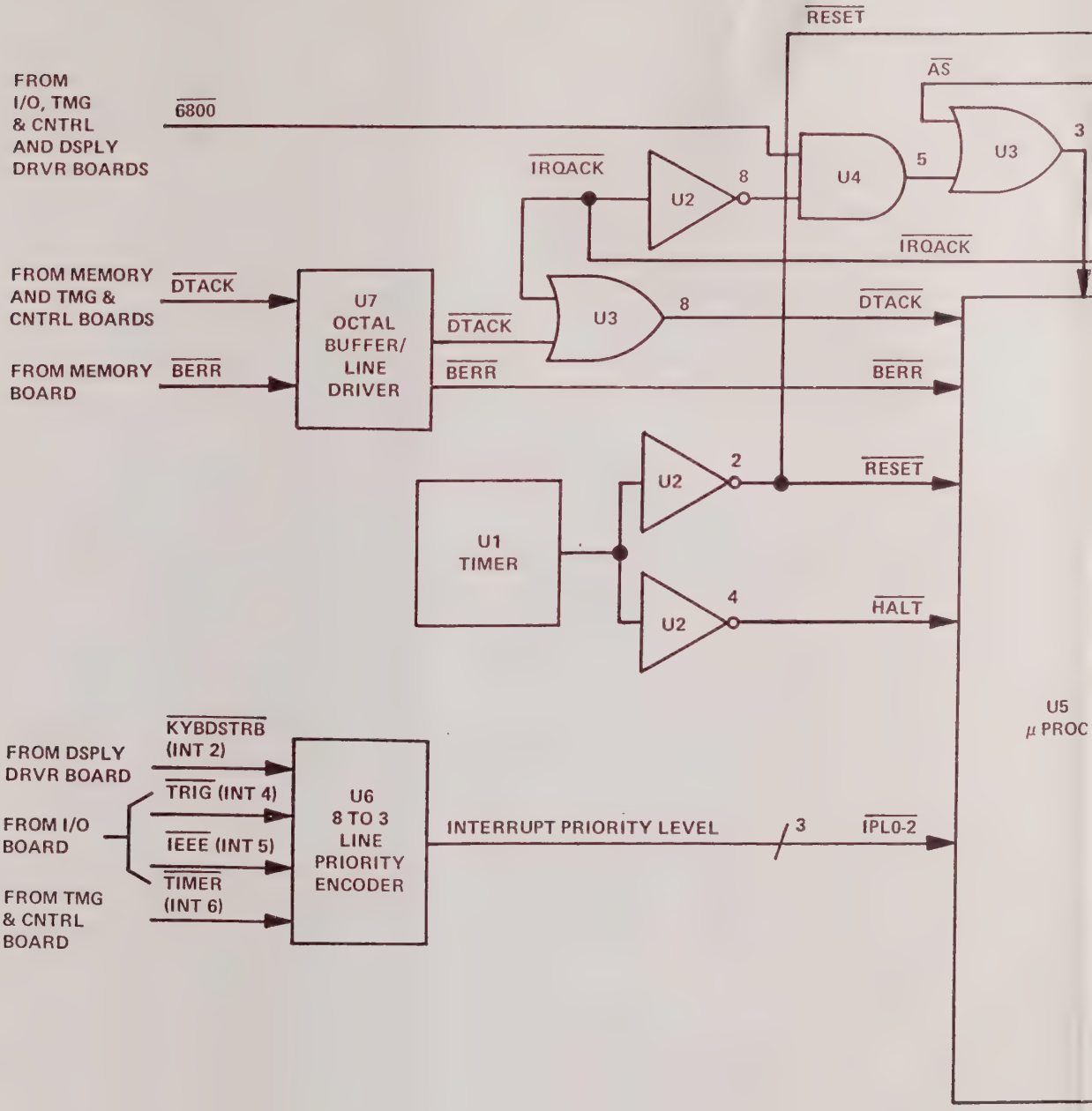


Figure 2-3. Microprocessor Section, Functional Block Diagram


RESET
AS
FROM I/O, TMG & CNTRL AND DSPLY DRVR BOARDS
6800
IRQACK
U2
8
U4
5
U3
3
IRQACK
FROM MEMORY AND TMG & CNTRL BOARDS
DTACK
FROM MEMORY BOARD
BERR
U7 OCTAL BUFFER/ LINE DRIVER
DTACK
BERR
U3
8
DTACK
BERR
U2
2
RESET
U1 TIMER
U2
4
HALT
U5 μ PROC
FROM DSPLY DRVR BOARD
KYBDSTRB (INT 2)
FROM I/O BOARD
TRIG (INT 4)
IEEE (INT 5)
FROM TMG & CNTRL BOARD
TIMER (INT 6)
U6 8 TO 3 LINE PRIORITY ENCODER
INTERRUPT PRIORITY LEVEL
3
IPL0-2

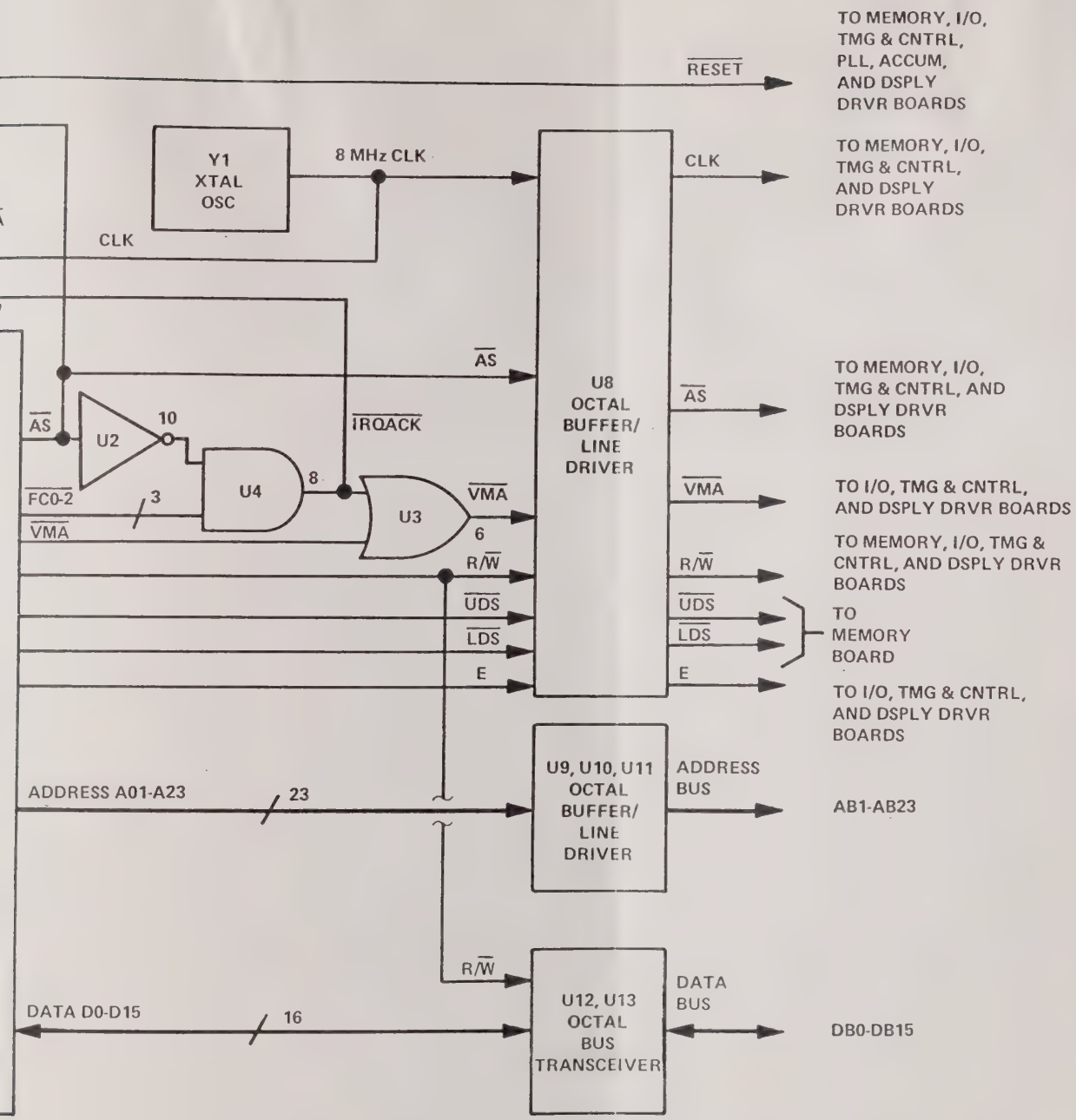


Figure 2-4. Microprocessor Board A1, Functional Signal Flow Diagram

the interrupt level received. The program will then branch to the interrupt service routines pointed to by the interrupt vector.

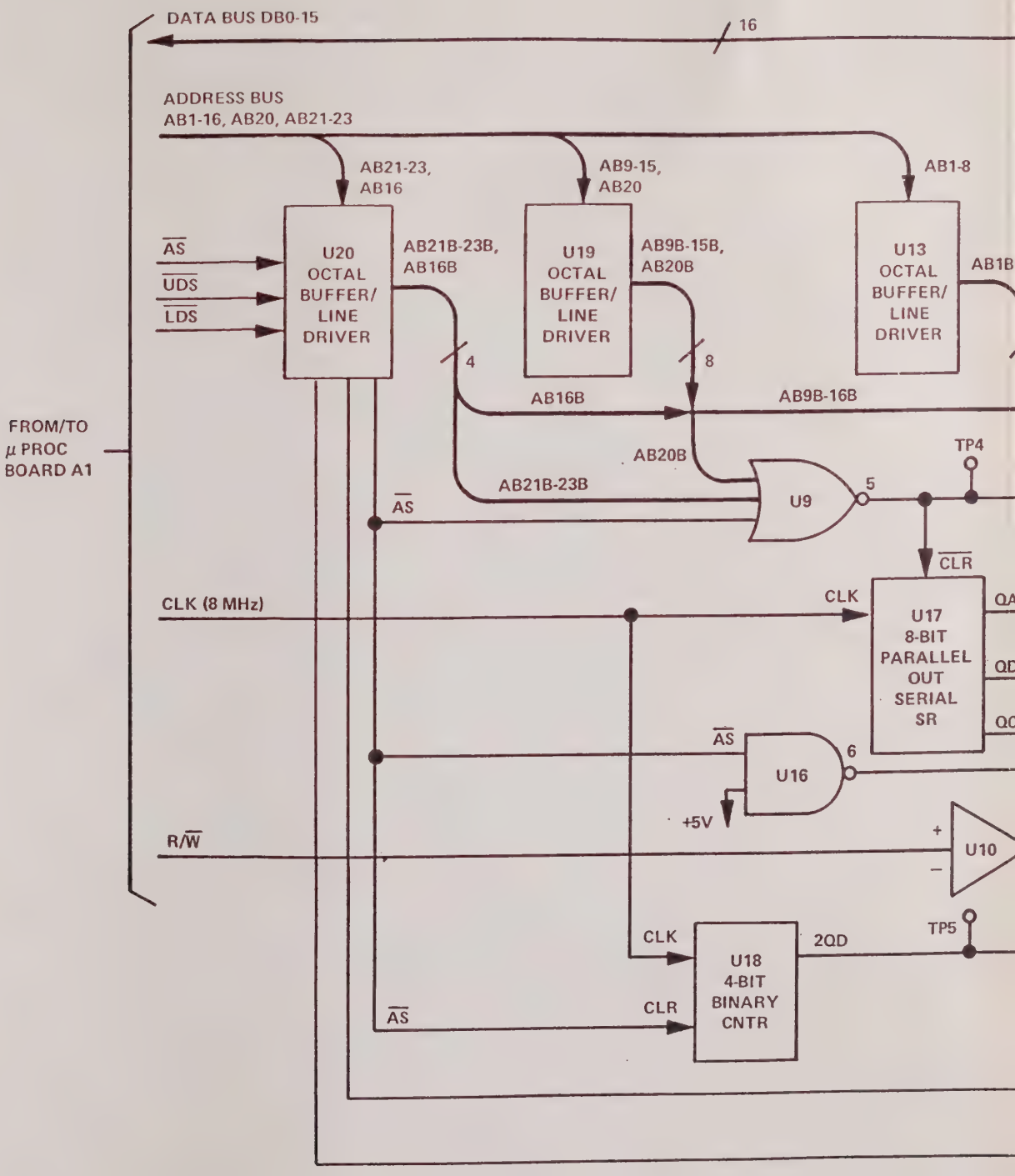
In general, at least once every signal sampling process, the microprocessor reads sampled and averaged data present on the accumulator RAM data bus. This data, when both accumulators are considered, consists of two sets of 64 samples for the input signals under consideration - input signal and reference signal. The microprocessor uses both sets of data to perform mathematical calculations to extract values for various parameters of the input signals as specified by user keyboard inputs. The mathematical calculations are based on a DFT algorithm residing in microprocessor program memory. When the DFT algorithm is applied to the two sets of 64 data samples, the result is magnitude and phase angle data for each set, related to an arbitrary reference point. If specific harmonics are to be evaluated, as determined from the keyboard inputs, additional DFT calculations are performed until amplitude and phase data are obtained for each harmonic of interest. This harmonic amplitude data can then be used to calculate total harmonic distortion (THD).

For sets of data samples that represent input frequencies greater than 3.16 kHz, the 64 data samples equal more than one cycle (the fundamental) of the input signal. The DFT program is designed to interpret either the 3rd, 7th, or 9th harmonic as the fundamental in these cases. The microprocessor also calculates ratio measurements. In ratio mode, the microprocessor divides the signal section data by the reference section data to calculate the numeric ratio. When the operator keys in a requirement for a ratio reading in dB, the microprocessor calculates the dB value relative to the reference section data. For gain or loss measurements in dB, the microprocessor can perform calculations using either a presently displayed voltage or an operator-entered value as a reference voltage. The calculation of percent deviation is handled by the microprocessor in a manner similar to gain and loss measurements in dB, except that the result is expressed as a percent change from the reference voltage instead of dB relative to the reference voltage. The values calculated by the microprocessor are communicated via the data bus to the display function for display on the front panel, and to the I/O function for communicating to equipment external to the DAV, via the IEEE 488 data bus.

b. MEMORY BOARD A2. (See figure 2-5 for details of functional signal flow on Memory board A2.)

Memory board A2 contains four 16K by 8-bit ultraviolet erasable programmable read-only-memory (UVEPROM) storage devices - a total memory capacity of 64K data bytes -, and four 8K by 8-bit random access memory (RAM) devices - a total working storage capacity of 32K data bytes. Within UVEPROM storage resides the stored DAV program, while RAM provides temporary storage for system variables (initiated from the front panel keyboard), and the results of calculations performed by microprocessor A1. Memory board A2 uses the microprocessor clock to generate control signals. Data bus transfers are performed asynchronously using the address bus (AB1-16, AB20, AB21-23), address strobe ($\overline{AS}$), upper and lower data strobes ($\overline{UDS}$, $\overline{LDS}$), the read/write enable (R/$\overline{W}$) and data transfer acknowledge ($\overline{DTACK}$). Two UVEPROMs and two RAMS each are assigned to upper and lower data bytes DB8B-15B and DB0B-7B, respectively.

Data is both written to and read from RAM, while data is only read from UVEPROM. A read cycle is initiated when the microprocessor sets the R/$\overline{W}$ line to read (high), places a function code (processor status) on the internal FC0-2 lines, places memory board A2 address on lines AB1-16, AB20, and AB21-23, and asserts the address strobe


DATA BUS DB0-15
16
ADDRESS BUS
AB1-16, AB20, AB21-23
AB21-23, AB16
AB9-15, AB20
AB1-8
AS
UDS
LDS
U20 OCTAL BUFFER/ LINE DRIVER
AB21B-23B, AB16B
U19 OCTAL BUFFER/ LINE DRIVER
AB9B-15B, AB20B
U13 OCTAL BUFFER/ LINE DRIVER
AB1B
4
8
AB16B
AB9B-16B
FROM/TO μ PROC BOARD A1
AB20B
AB21B-23B
U9
5
TP4
AS
CLR
CLK (8 MHz)
CLK
U17 8-BIT PARALLEL OUT SERIAL SR
QA
QD
QC
AS
U16
6
+5V
R/W
U10
TP5
CLK
U18 4-BIT BINARY CNTR
2QD
CLR
AS

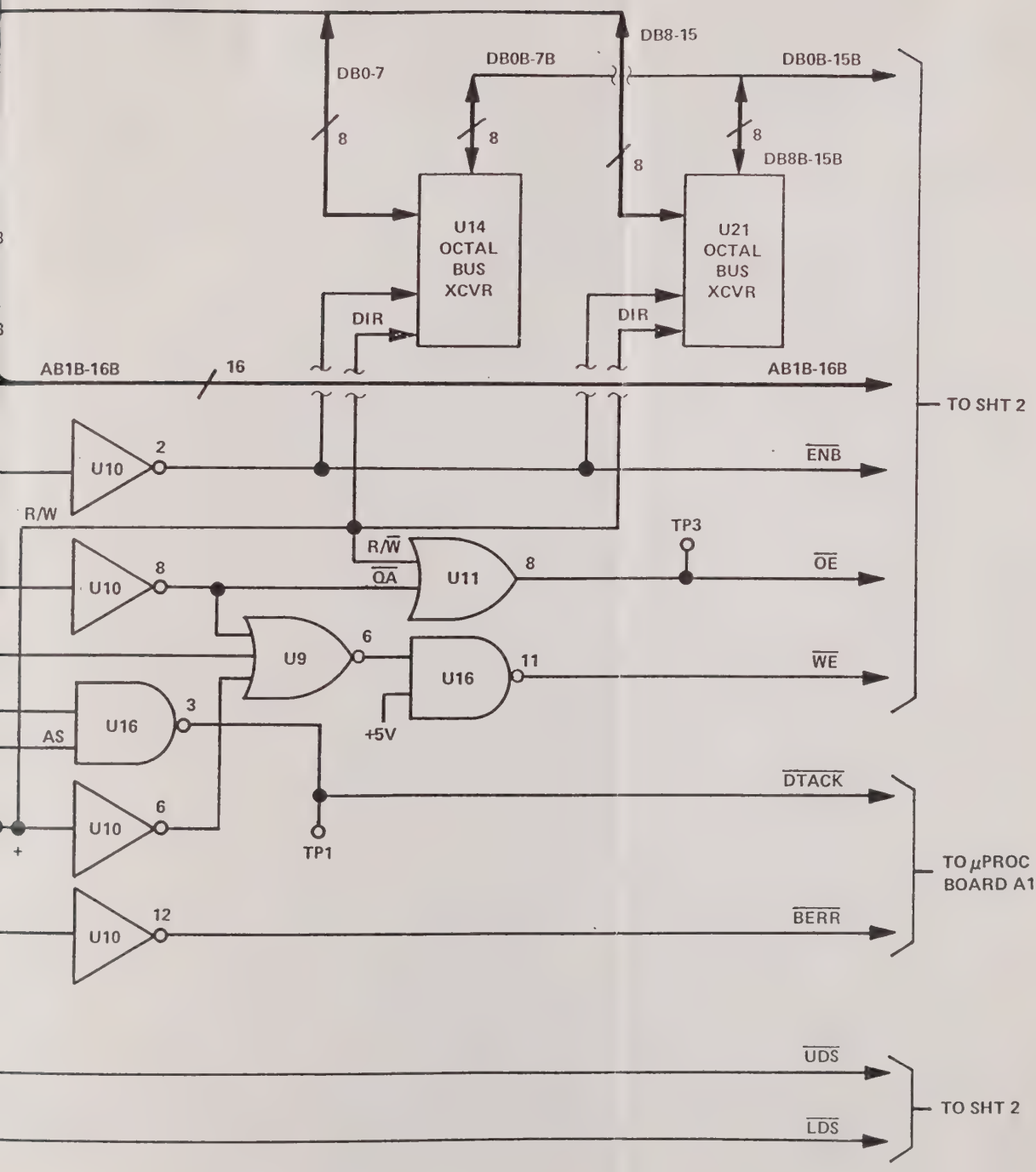
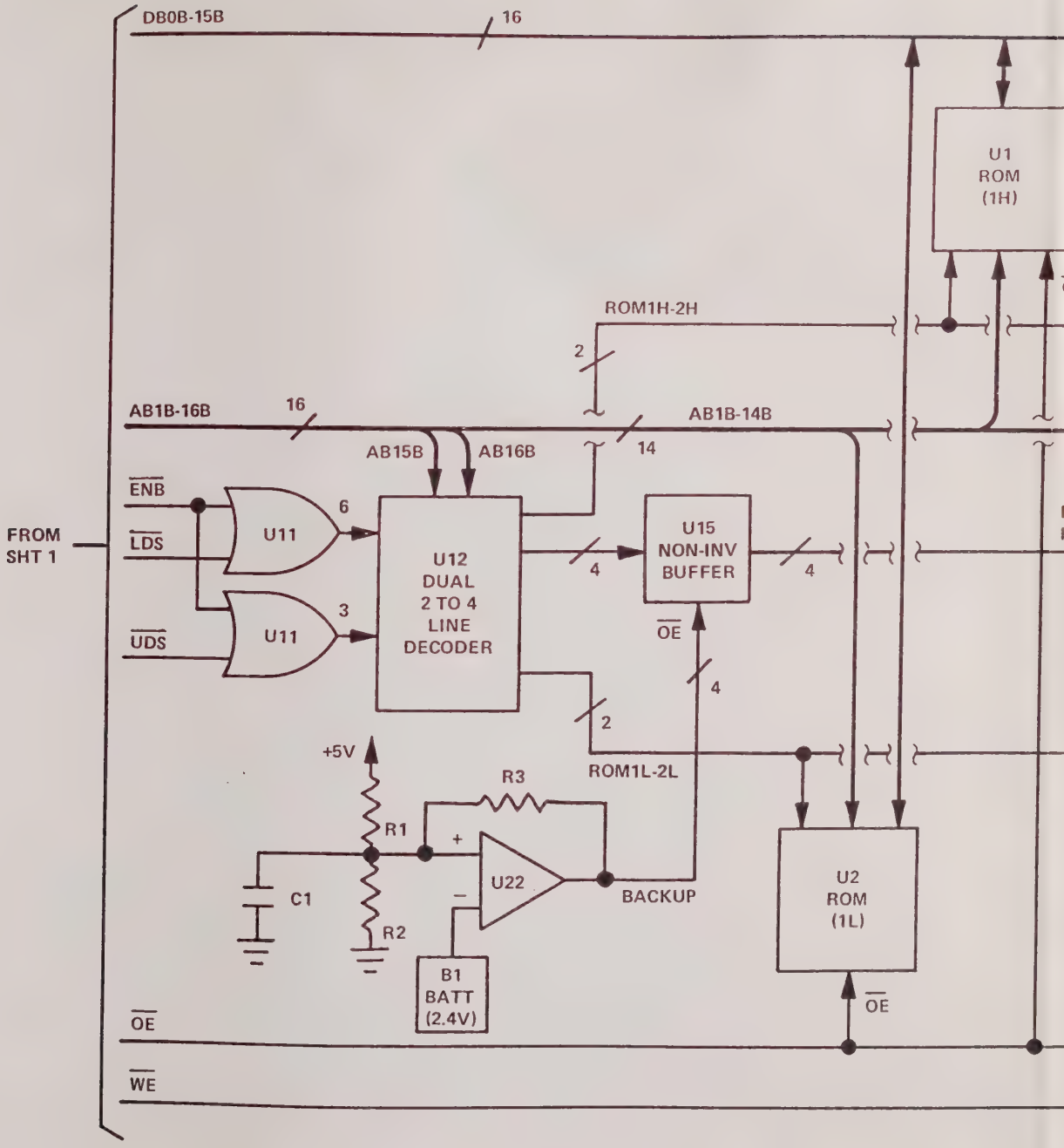


Figure 2-5. Memory Board A2, Functional Signal Flow Diagram (Sheet 1 of 2)


DB0B-15B
16
U1
ROM
(1H)
ROM1H-2H
2
AB1B-16B
16
AB1B-14B
AB15B
AB16B
14
ENB
LDS
UDS
FROM
SHT 1
U11
6
U11
3
U12
DUAL
2 TO 4
LINE
DECODER
4
U15
NON-INV
BUFFER
4
OE
4
2
ROM1L-2L
+5V
R3
R1
+
U22
–
C1
R2
BACKUP
B1
BATT
(2.4V)
U2
ROM
(1L)
OE
OE
WE

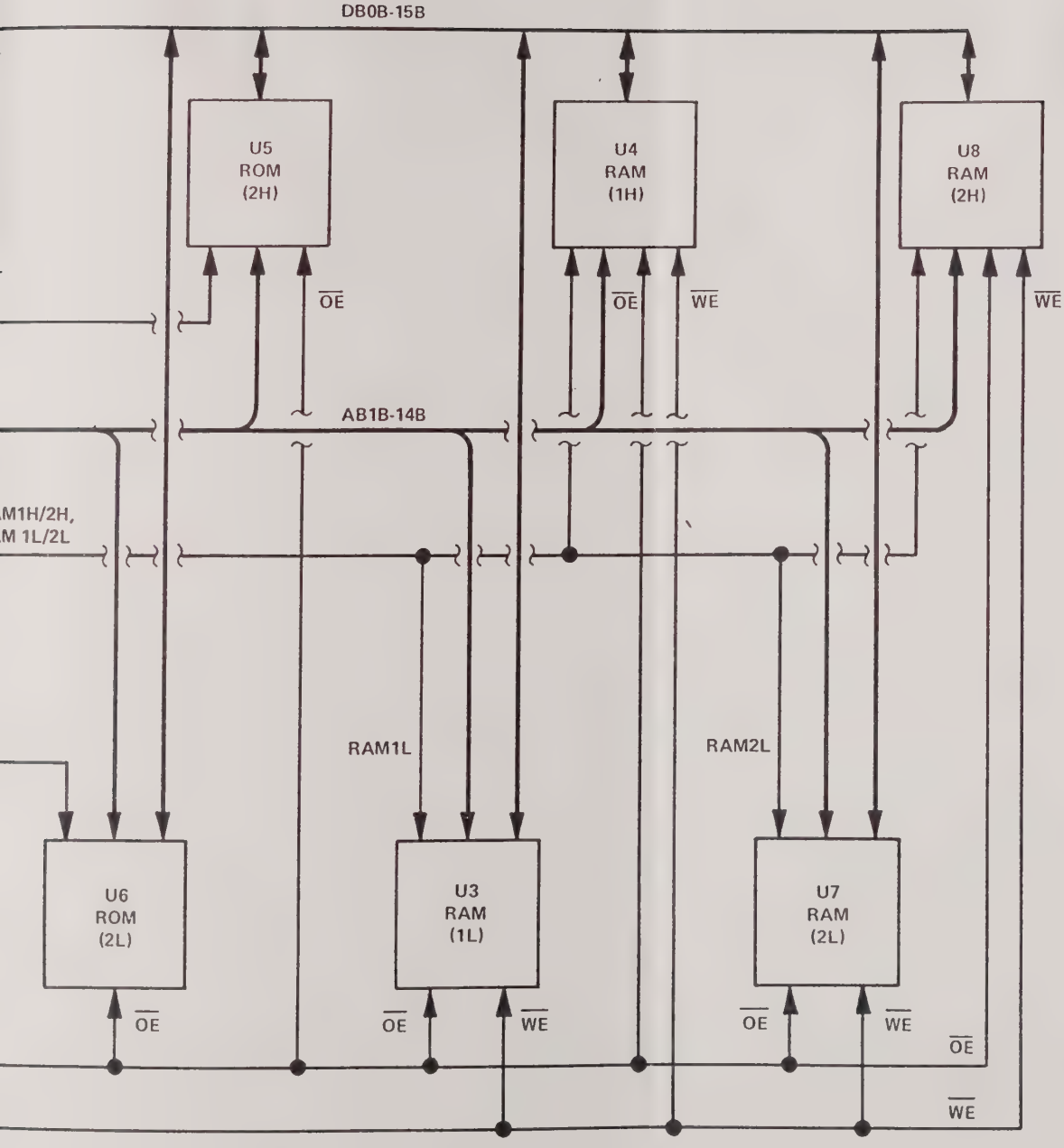


Figure 2-5. Memory Board A2,
Functional Signal Flow Diagram
(Sheet 2 of 2)

($\overline{AS}$). Following this, the $\overline{UDS}$ and $\overline{LDS}$ signals are asserted (address bit AB0 equals 0 for $\overline{UDS}$ and 1 for $\overline{LDS}$). Upon receipt of the address, an address decoder enable is produced, conditioned by the address strobe. With the R/$\overline{W}$ control high, an output enable is produced for the upper and/or lower byte UVEPROM and RAM devices and a pair of bus transceivers are enabled to read data from the UVEPROM/RAM data bus to the microprocessor data bus. A shift register, clocked by the 8 MHz clock, acts as a state machine to produce output enable and signals at the proper times. After data is transferred to the data bus, the data transfer acknowledge ($\overline{DTACK}$) to the microprocessor is asserted by the last state output of the shift register. When the microprocessor latches the data, the $\overline{UDS}$, $\overline{LDS}$, and $\overline{AS}$ lines are negated and data is removed from the DB0-15 lines. When $\overline{AS}$ is negated, $\overline{DTACK}$ is also negated.

Write cycle timing is similar, except the R/$\overline{W}$ input is asserted (low) after the memory board address is placed on the bus and the address strobe ($\overline{AS}$) is asserted. In this case, the bus transceivers are enabled in the reverse direction to transfer upper and/or lower bytes of data from the microprocessor bus to the UVEPROM/RAM data bus. Although an output enable is still generated, the state of address bits AB15 and 16 cause the UVEPROM enable (chip select) to be deselected, and only the RAM select is generated for a write data transfer. Write enable to RAM is also produced by the state output of the shift register. After data is written to RAM the data transfer acknowledge ($\overline{DTACK}$) is asserted. The microprocessor then negates $\overline{UDS}$, $\overline{LDS}$, and $\overline{AS}$, removes data from the bus lines and sets R/$\overline{W}$ to read (high). When $\overline{AS}$ is negated, $\overline{DTACK}$ is also negated to terminate the bus write cycle.

If no data transfer acknowledge ($\overline{DTACK}$) is produced, the microprocessor produces wait states with address strobe ($\overline{AS}$) still asserted. If $\overline{DTACK}$ is not produced prior to eight microprocessor clock times, a bus error ($\overline{BERR}$) signal is produced by a watchdog counter and sent to the microprocessor; this causes a microprocessor halt state which terminates the bus cycle and maintains the data and address buses in a high-impedance state, until $\overline{BERR}$ is negated.

The random access memory chip select buffer on memory board A2 is furnished with a backup battery input voltage in case RAM power fails. This voltage inhibits the RAM chip select (enable) signals, thereby preventing extraneous data from being written to RAM as system power decays. Thus, the data already stored in RAM is preserved.

2-6. SIGNAL AND REFERENCE SECTIONS FUNCTIONAL DESCRIPTION. (See figure 2-6.)

The Signal and Reference sections each consist of a front end board A14/A11, an A/D converter board A12/A9 and a programmable filter board A13/A10 with associated shielding. Each isolated channel (signal or reference) receives an input of the signal under evaluation through either the front panel SIG or REF binding posts, or through respective rear panel connectors J1 or J2. In the case of the rear panel connectors, the signal and reference inputs are passed through a length of triaxial cable to the associated signal and reference isolation boards A15A4 and A5; the front panel binding posts make a direct mechanical connection to the associated isolation board.

When the autocalibration mode is not active, control signal MSR/$\overline{AC}$ from the associated accumulator board A6/A7 is high (negated) and the isolation boards each maintain high-voltage, low capacitance isolation from each other and from other DAV circuits during normal measurement (MSR) operation. When MSR/$\overline{AC}$ is asserted, this control signal is optically coupled to a set of relay drivers, thereby causing the measurement input signal(s) under test to be disconnected.

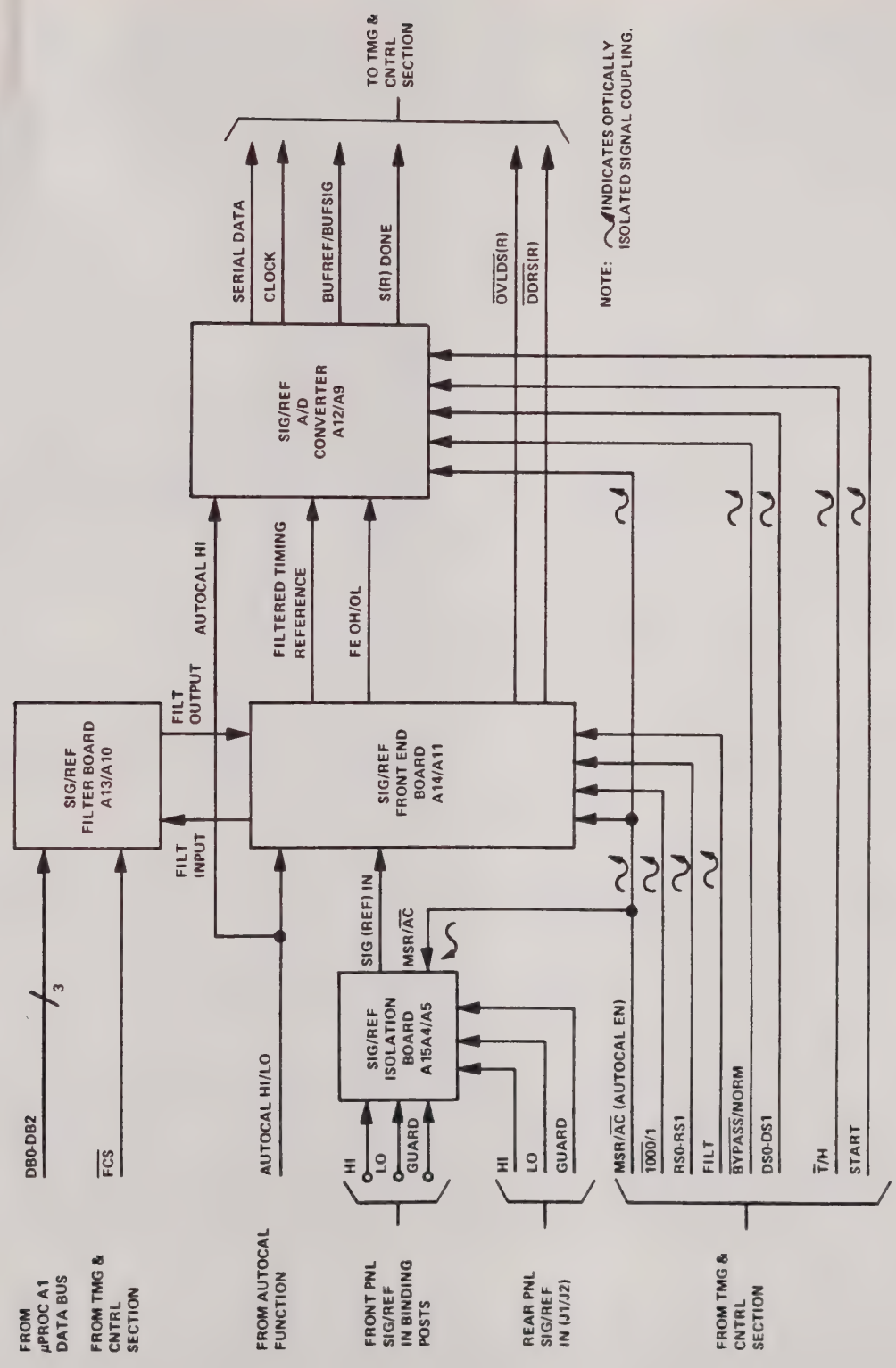


Figure 2-6. Signal/Reference Sections, Functional Block Diagram

a. SIGNAL AND REFERENCE FRONT END BOARDS A14/A11. (See figure 2-7 for details of functional signal flow on Front End boards A14/A11.)

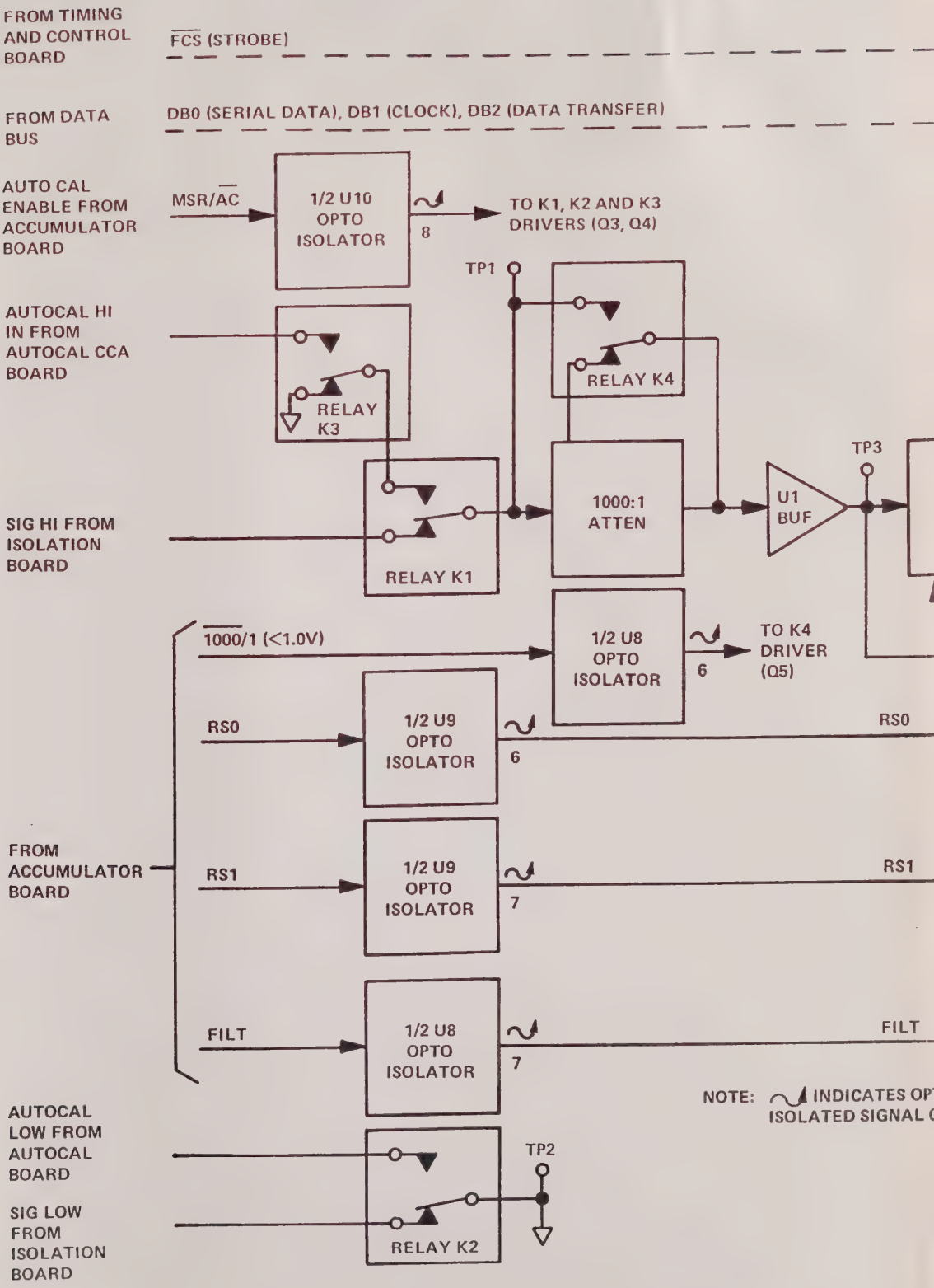
The output of the isolation board is applied to front end board A14/A11 in the associated channel through a length of triaxial cable that terminates on motherboard A16A1. The input signal to front end board A14/A11 is capacitively coupled and routed through isolation relays to a selectable 1:1 or 1000:1 attenuator, through an overload-protected buffer amplifier, and then to a three-step decade attenuator. The combination of the 1000:1 attenuator and the decade attenuator provide for selection of 1 of 6 ranges. The attenuator output is applied to a fixed gain amplifier (gain of 17.3205) whose output, in turn, is applied to precision filter board A13/A10; to a high frequency noise filter with a cutoff of about 350 kHz; and to the overload/range comparator logic. The MSR/$\overline{AC}$, $\overline{1000}$/1, RS0/RS1, and FILT control input signals from the front end control output port on associated accumulator board A6/A7 are all optically coupled at front end board A14/A11, thereby providing maximum isolation for improved common mode rejection. These control inputs are derived from output ports (latches) on the respective accumulator A6/A7, and are strobed into accumulator board A6/A7 by a signal/reference front end control signal ($\overline{SFECTL}$/$\overline{RFECTL}$) from the timing and control board A4. The amplified signal passes through the selectable, programmable low pass filter (activated by the FILT control input) and is further amplified with an additional gain of 17.3205 to yield a total signal gain of 300. This analog output signal (FE OH/OL) is supplied to the input of A/D converter board A12/A9. An additional gain of 17.3205 amplifier always receives the output of the programmable filter and provides an input to the zero crossing comparator circuit on the A/D converter board A12/A9.

b. SIGNAL AND REFERENCE FILTER BOARDS A13/A10. (See figure 2-8 for details of functional signal flow to and from Filter boards A13/A10.)

Precision signal and reference filter boards A13/A10 are programmable 4-pole low pass filters that receive the amplified signal from a point between the gain stages of front end board A14/A11. The filter is switched into the main signal path when in the FUND, QUAD, IN-PHASE, and PHASE ANGLE modes. The cutoff frequency of the filter is programmed in serial form in an 11-bit word placed on the DB0 line of the data bus. The most significant bit (MSB) of this word specifies frequency range; the remaining 10 bits specify a frequency within the range. Data bus line DB1 contains the serial clock input, while the DB2 line initiates data transfer from the filter register to the filter. These data transfers to the filter occur when the filter is selected as an output port with strobe $\overline{FCS}$.

c. SIGNAL AND REFERENCE A/D CONVERTER BOARDS A12/A9. (See figure 2-9 for details of functional signal flow on A/D Converter boards A12/A9.)

The amplified signal (RFE OH/OL) from signal/reference front end boards A14/A11 is supplied to the input of respective signal/reference A/D converter board A12/A9. Within the A/D converter, the signal passes through contacts of a calibration isolation relay (MSR/$\overline{AC}$ negated), and through a four-step binary attenuator and gain of 4 amplifier. When TOTAL (AVG) mode is selected the signal passes through the TOTAL (AVG) rectifier circuit and then to the track/hold amplifier. The binary attenuator, which provides for selection of one of 4 inter-ranges, is controlled by the DS0-DS1 output of the front end control output port on the associated accumulator. This port is strobed by the respective signal front end control ($\overline{SFECTL}$) and reference front end control ($\overline{RFECTL}$) signals generated by the timing and control board A4.


FROM TIMING AND CONTROL BOARD
FCS (STROBE)
FROM DATA BUS
DB0 (SERIAL DATA), DB1 (CLOCK), DB2 (DATA TRANSFER)
AUTO CAL ENABLE FROM ACCUMULATOR BOARD
MSR/AC
1/2 U10 OPTO ISOLATOR
8
TO K1, K2 AND K3 DRIVERS (Q3, Q4)
TP1
AUTOCAL HI IN FROM AUTOCAL CCA BOARD
RELAY K3
RELAY K4
TP3
SIG HI FROM ISOLATION BOARD
RELAY K1
1000:1 ATTEN
U1 BUF
1000/1 (<1.0V)
1/2 U8 OPTO ISOLATOR
6
TO K4 DRIVER (Q5)
RS0
1/2 U9 OPTO ISOLATOR
6
RS0
FROM ACCUMULATOR BOARD
RS1
1/2 U9 OPTO ISOLATOR
7
RS1
FILT
1/2 U8 OPTO ISOLATOR
7
FILT
NOTE: INDICATES OP
ISOLATED SIGNAL
AUTOCAL LOW FROM AUTOCAL BOARD
SIG LOW FROM ISOLATION BOARD
TP2
RELAY K2

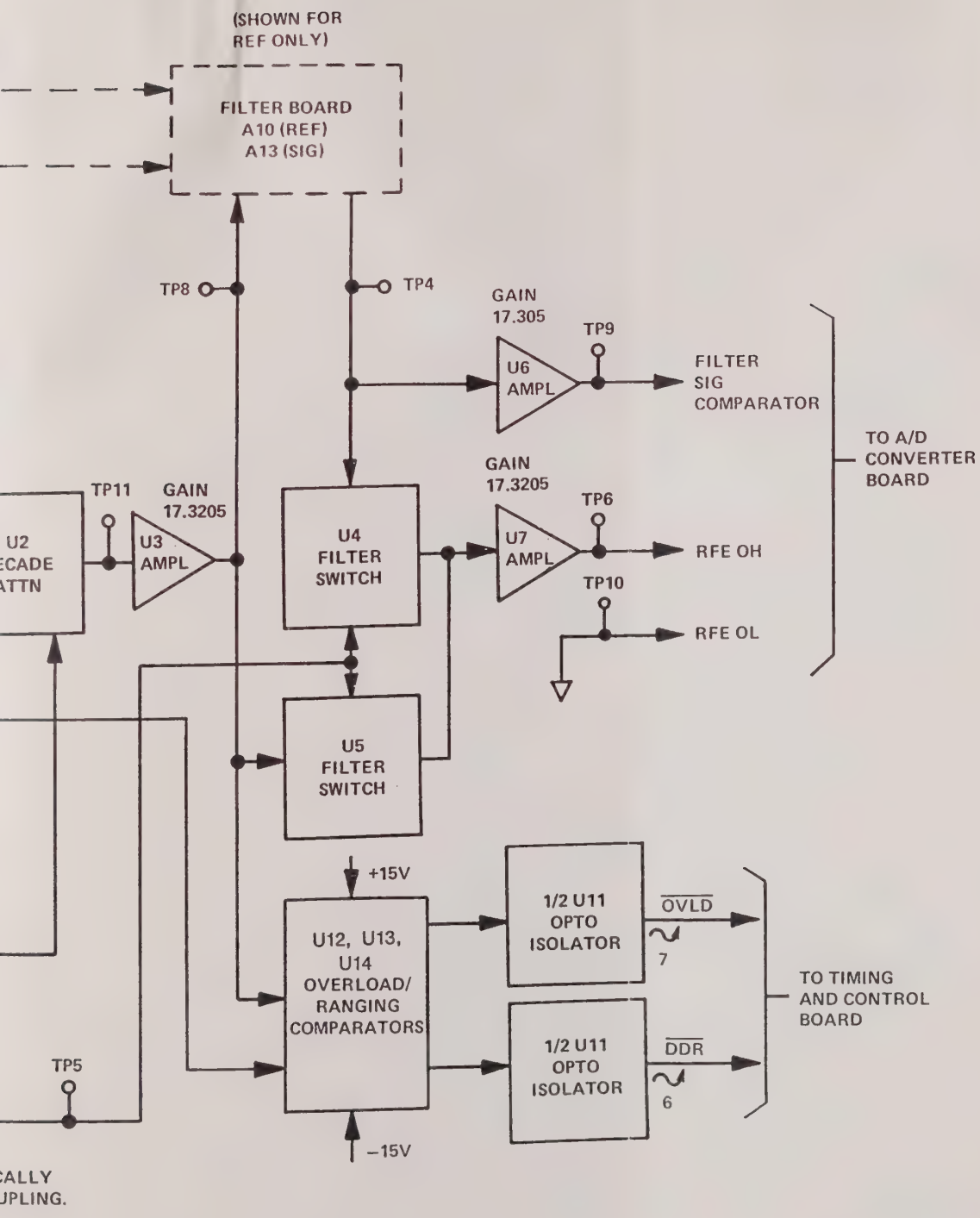


Figure 2-7. Front End Boards A11/A14, Functional Signal Flow Diagram

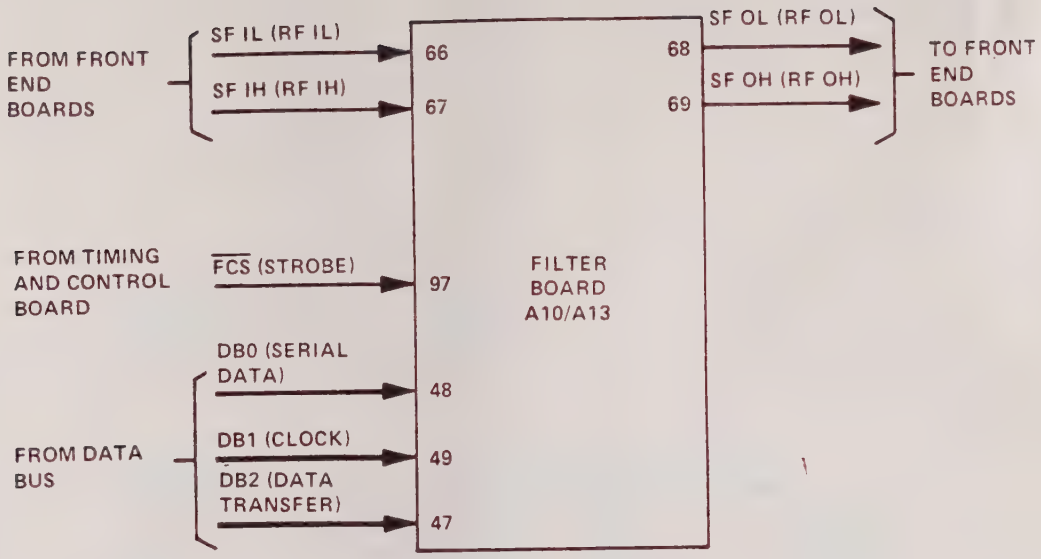


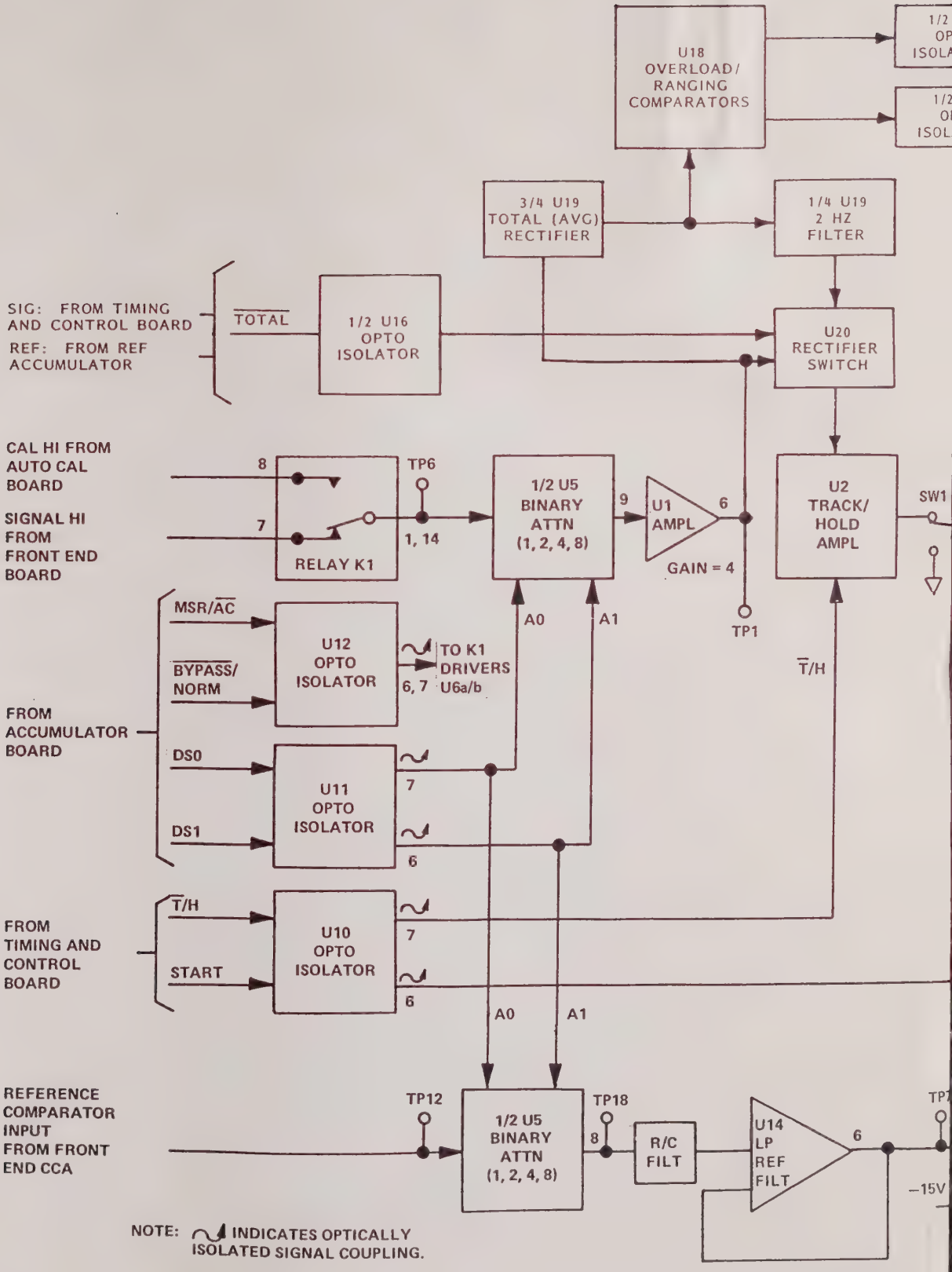
Figure 2-8. Filter Board A10/A13, Signal Interconnection Diagram

During the data acquisition and processing cycle, timing and control board A4 sequences the events that take place. One of the first events to occur is the holding of a data sample at the output of the track/hold amplifier so that the A/D converter can obtain an accurate digital approximation of a discreet point on a time-varying analog signal. Following this, the START input is asserted, thereby enabling the A/D converter to digitize the analog signal sample. The A/D converter thus provides a 12-bit serial data output accompanied by a serial data clock signal, to associated accumulator board A6/A7. When conversion is complete, the A/D converter status output line goes low and this signal is sent to timing and control board A4 as the DONE enable. The serial data, clock, DONE (SDONE/RDONE), and BUFREF outputs are all passed to the output by extremely high-speed (10 MHz) optical isolators. The timing and control board A4 state machine enters a wait state during the data acquisition process until both the SDONE and RDONE outputs are received from respective signal and reference A/D converter boards A12/A9.

The BUFREF signal generated by A/D converter board A12/A9 is derived from the filtered timing reference signal input from associated front end board A14/A11. This signal is coupled through a binary attenuator (also controlled by the DS0-DS1 inputs) 3 pole low pass filter and to a zero-crossing detector (comparator). The resultant output, a TTL compatible square wave, is optically coupled to PLL board A5, where it is used for sample synchronization and frequency measurement.

d. SHIELDING.

Each measurement channel (signal and reference) is electrostatically and electromagnetically isolated from each other as well as from the rest of the measurement system. There are no common grounds. This is accomplished by using highly isolated power supplies A17PS2 and A17PS3, and by effectively shielding sensitive analog circuits by enclosing each of the three boards in each channel in an electrostatic shield which is connected to the respective front panel GUARD binding post. On front end boards A14/A11, this shield is made of magnetic material to reduce pickup of power frequency signals. As mentioned previously, input signals are routed to front


U18
OVERLOAD/
RANGING
COMPARATORS
3/4 U19
TOTAL (AVG)
RECTIFIER
1/4 U19
2 HZ
FILTER
SIG: FROM TIMING
AND CONTROL BOARD
REF: FROM REF
ACCUMULATOR
TOTAL
1/2 U16
OPTO
ISOLATOR
U20
RECTIFIER
SWITCH
CAL HI FROM
AUTO CAL
BOARD
SIGNAL HI
FROM
FRONT END
BOARD
8
7
RELAY K1
TP6
1, 14
1/2 U5
BINARY
ATTN
(1, 2, 4, 8)
9
U1
AMPL
6
GAIN = 4
U2
TRACK/
HOLD
AMPL
SW1
TP1
MSR/AC
BYPASS/
NORM
U12
OPTO
ISOLATOR
TO K1
DRIVERS
6, 7 U6a/b
A0
A1
T/H
FROM
ACCUMULATOR
BOARD
DS0
DS1
U11
OPTO
ISOLATOR
7
6
T/H
START
FROM
TIMING AND
CONTROL
BOARD
U10
OPTO
ISOLATOR
7
6
A0
A1
REFERENCE
COMPARATOR
INPUT
FROM FRONT
END CCA
TP12
1/2 U5
BINARY
ATTN
(1, 2, 4, 8)
TP18
8
R/C
FILT
U14
LP
REF
FILT
6
−15V
NOTE: INDICATES OPTICALLY
ISOLATED SIGNAL COUPLING.

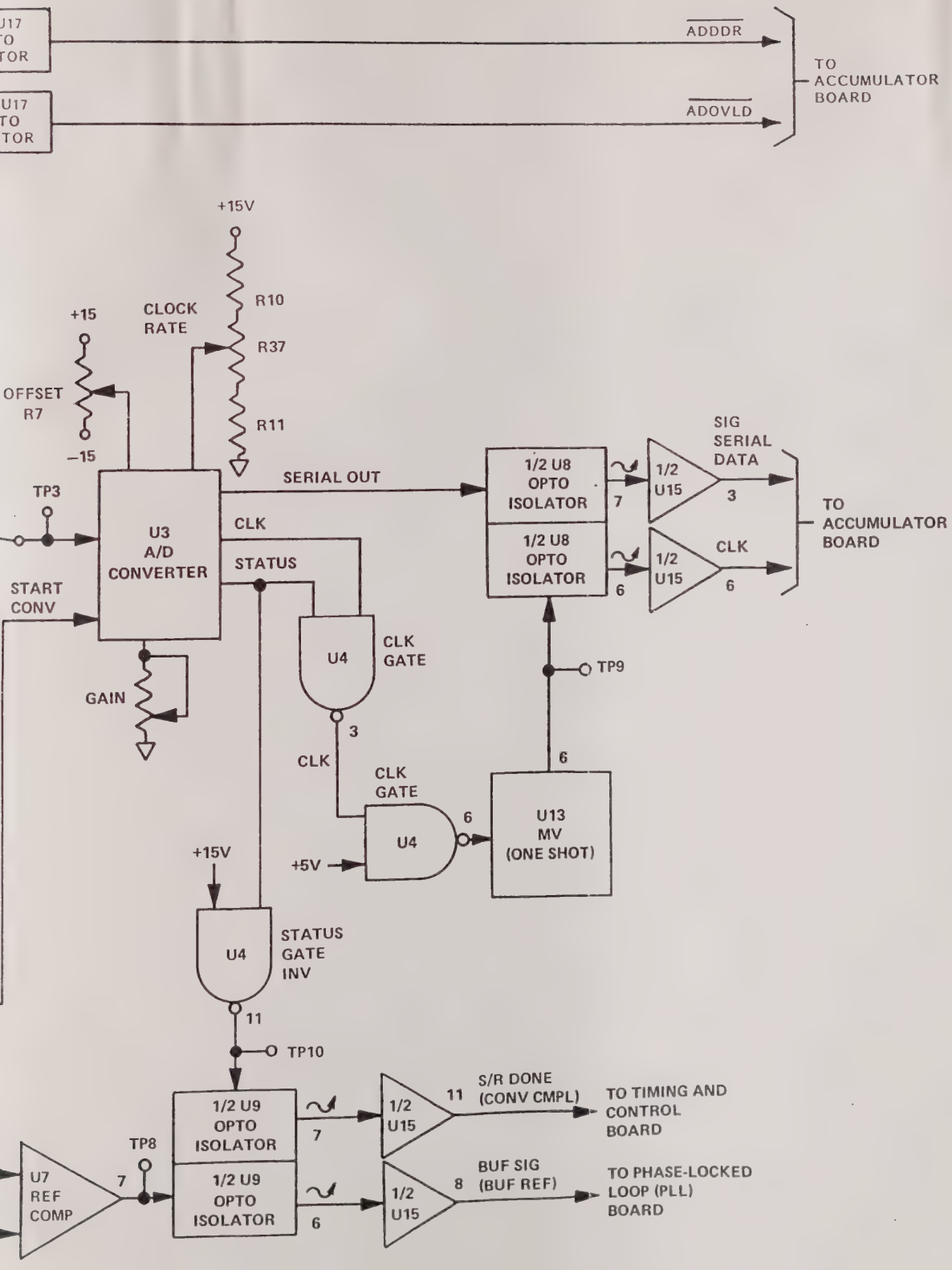


Figure 2-9. A/D Converters A9/A12, Functional Signal Flow Diagram

end boards A14/A11 using triaxial cable. The center conductor and inner shield are the input high and low, respectively; the second shield is connected to the front panel GUARD binding post. For high impedance null and bridging measurements, this guard may be driven by a low impedance potential equal to the input signal low, thereby unloading the capacitance between the signal and the rest of the measurement system. For less critical measurements, this guard is simply strapped to the low side of the input.

2-7. TIMING AND CONTROL SECTION FUNCTIONAL DESCRIPTION. (See figure 2-10.)

The timing and control section consists of four boards that operate as an integral function to control, acquire, and process digitized data representing the input and reference signals; these boards include timing and control A4, phase locked loop (PLL) A5, and signal and reference accumulators A6/A7.

a. TIMING AND CONTROL BOARD A4. (See figure 2-11 for details of functional signal flow on Timing and Control board A4.)

Timing and control board A4 performs 3 distinct functions. First, it provides I/O ports for communication with other DAV hardware. Second, it controls the data acquisition and sample averaging process. Lastly, it provides frequency measurement and timing functions.

(1) I/O Port Control. A 1 of 8 decoder and a 1 of 16 decoder on timing and control board A4 are used to provide address decoding for microprocessor access to DAV internal I/O ports. The address represented by bits AB16-23 are decoded to provide an enable for each of the ports represented by the 16 outputs from this decoder. The 16 (Hexadecimal numbers 0 through F) outputs are as follows:

0. Autocalibration status ($\overline{\text{ACLSTAT}}$) to autocal board A8.

1. Filter control strobe ($\overline{\text{FCS}}$) to the signal and reference front end filter boards A13 and A10.

2. Signal front end control ($\overline{\text{SFECTL}}$) to signal accumulator A6.

3. Reference front end control ($\overline{\text{RFECTL}}$) to reference accumulator A7.

4. Autocalibration control ($\overline{\text{ACLCTL}}$) to autocal board A8.

5. Autocalibration frequency ($\overline{\text{ACLFRQ}}$) to autocal board A8.

6. Lock indication control ($\overline{\text{LINCTL}}$) to PLL board A5.

7. Status (STATUS) to PLL board A5.

8. Start generator ($\overline{\text{STRTGN}}$) enable for generation of three coded binary bits (DIV0-3), based on the frequency being measured, for division of the CLKIN frequency from phase-locked loop board A5.

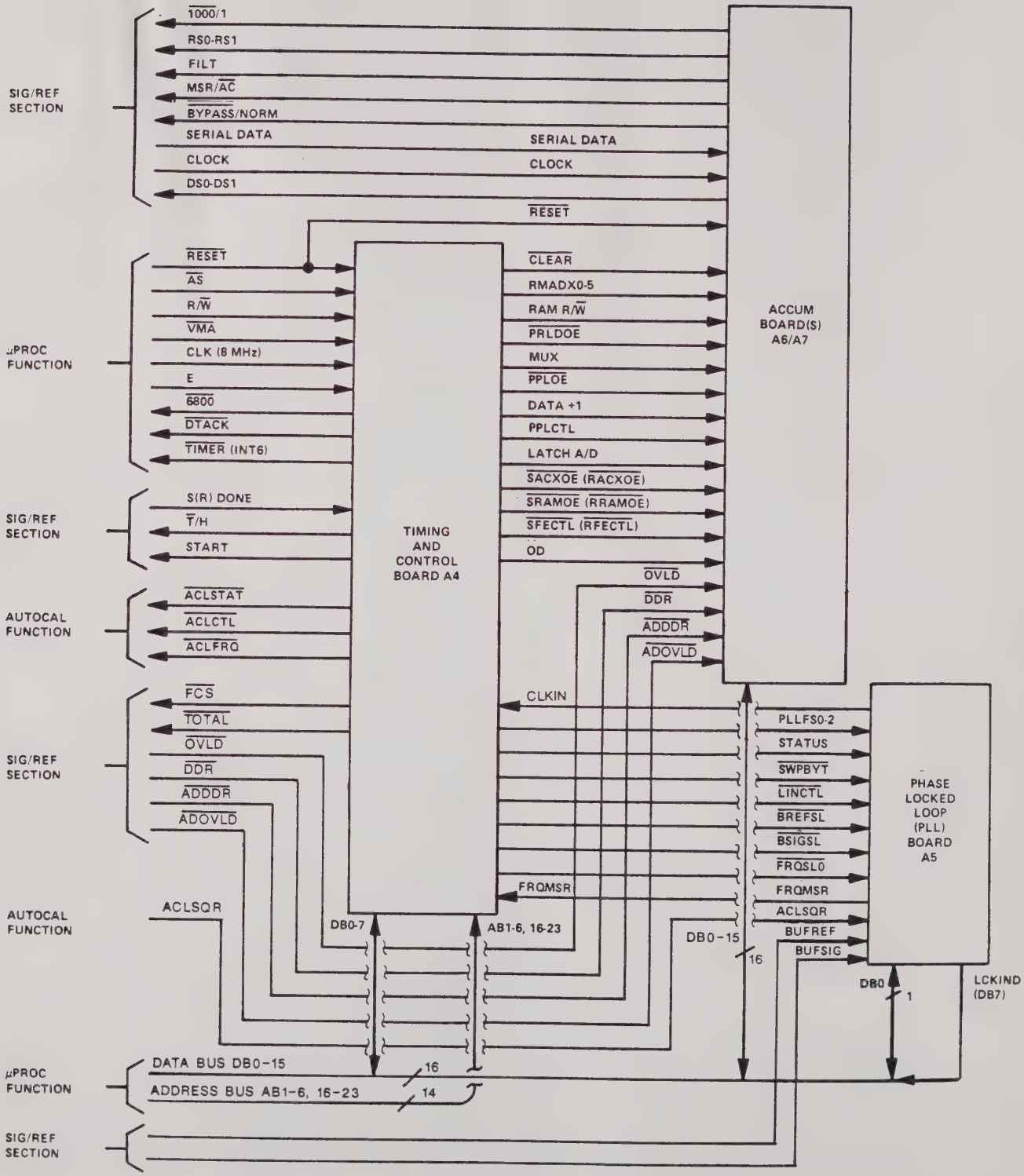
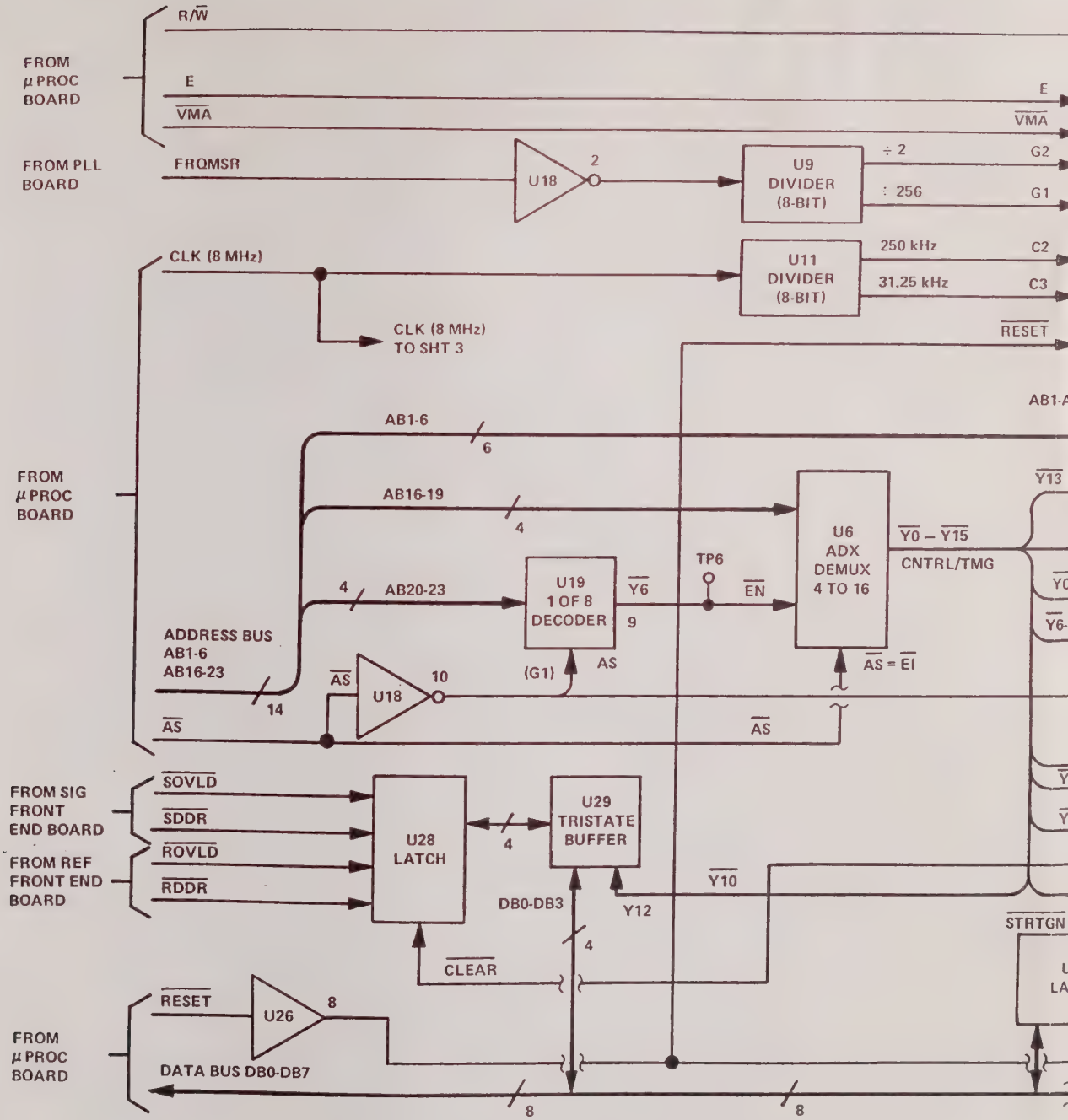


Figure 2-10. Timing and Control Section, Functional Block Diagram


FROM
µPROC
BOARD
R/W
E
VMA
FROM PLL
BOARD
FROMSR
U18
2
U9
DIVIDER
(8-BIT)
÷ 2
G2
÷ 256
G1
CLK (8 MHz)
U11
DIVIDER
(8-BIT)
250 kHz
C2
31.25 kHz
C3
CLK (8 MHz)
TO SHT 3
RESET
AB1-6
6
AB16-19
4
4
AB20-23
U19
1 OF 8
DECODER
Y6
9
(G1)
AS
TP6
EN
U6
ADX
DEMUX
4 TO 16
Y0 – Y15
CNTRL/TMG
AS = EI
Y13
ADDRESS BUS
AB1-6
AB16-23
14
AS
U18
10
AS
AS
FROM SIG
FRONT
END BOARD
FROM REF
FRONT END
BOARD
SOVLD
SDDR
ROVLD
RDDR
U28
LATCH
4
U29
TRISTATE
BUFFER
DB0-DB3
4
Y12
Y10
CLEAR
STRTGN
RESET
U26
8
FROM
µPROC
BOARD
DATA BUS DB0-DB7
8
8

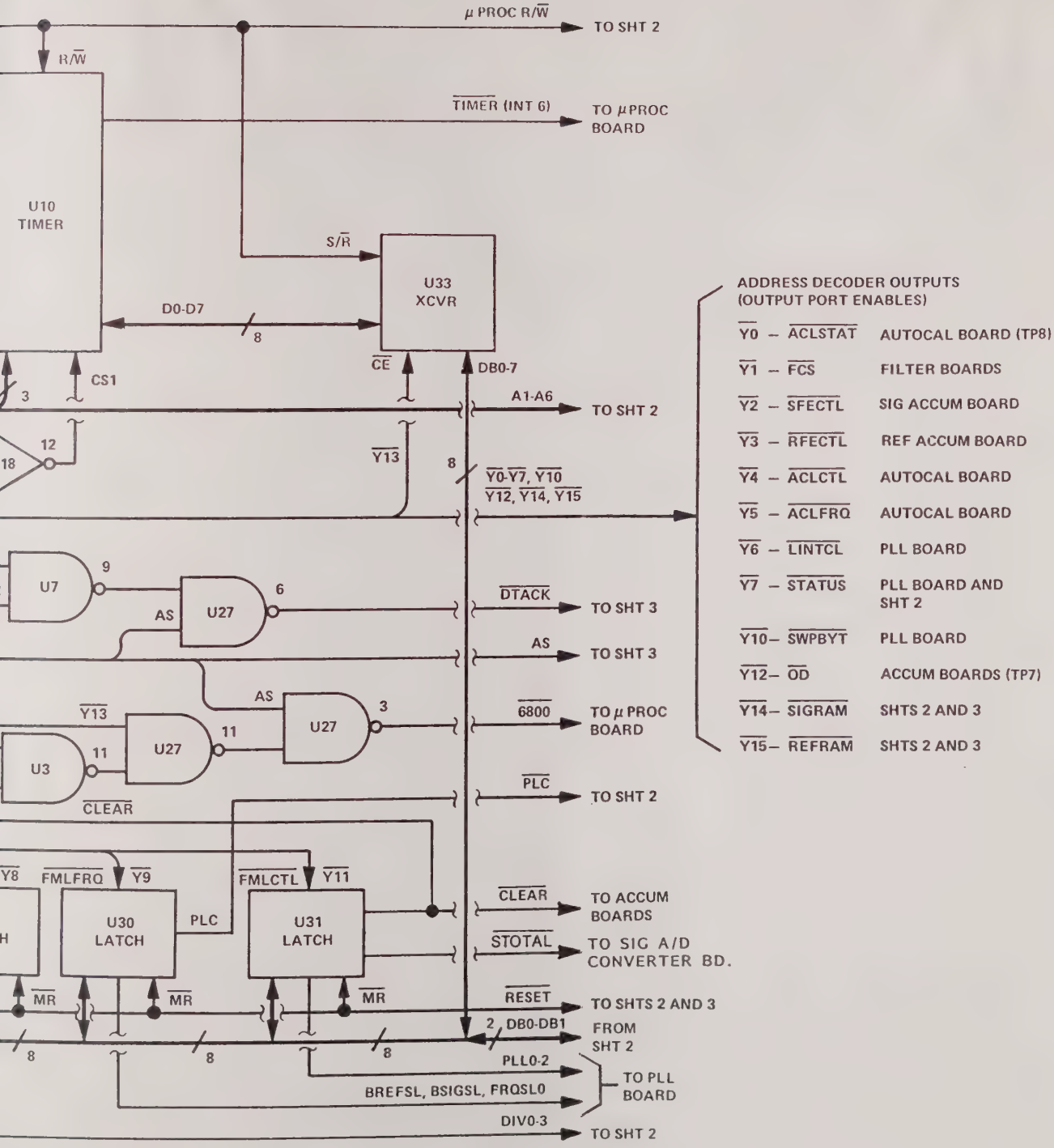
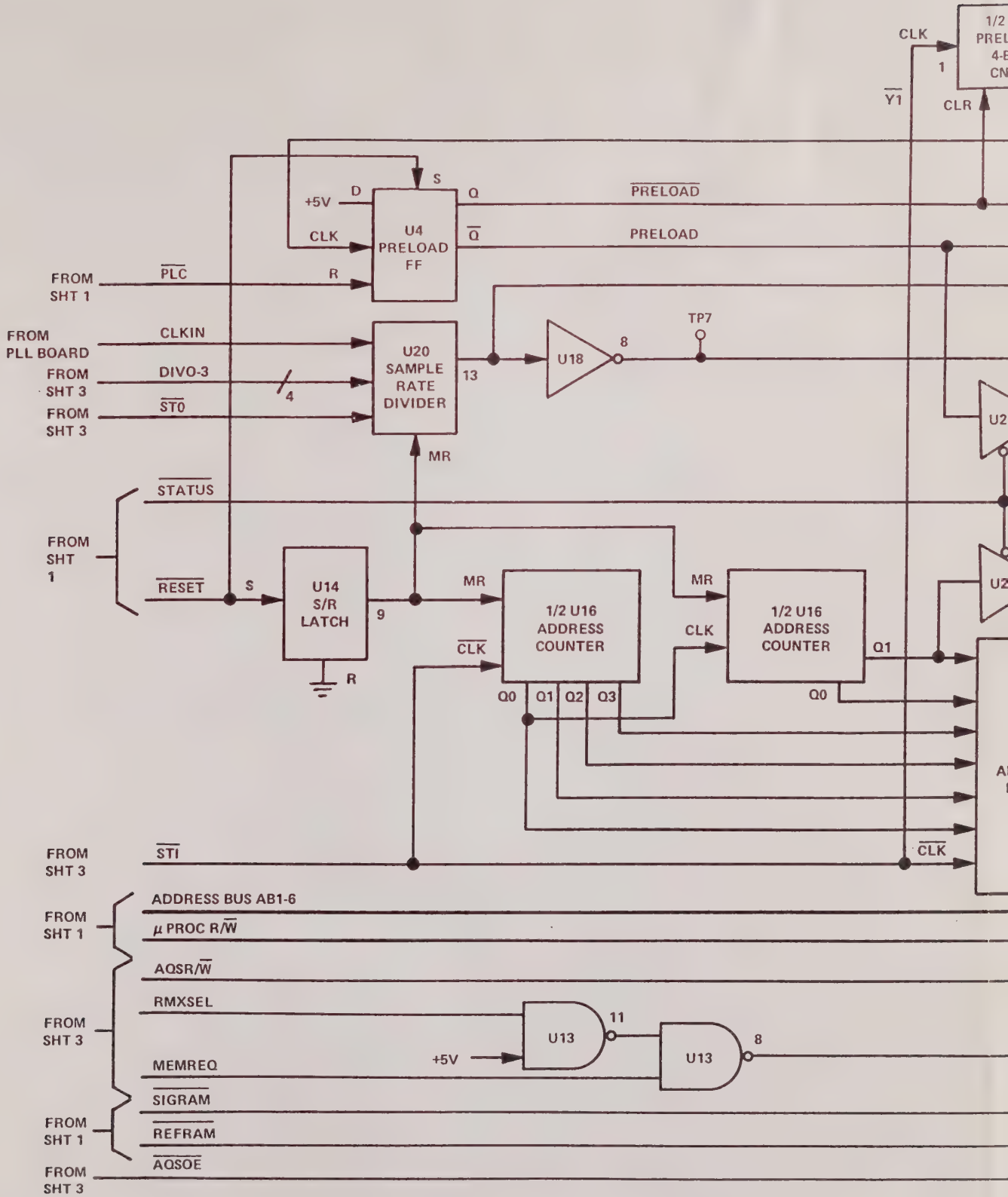


Figure 2-11. Timing and Control Board A4, Functional Signal Flow Diagram (Sheet 1 of 3)


CLK
1
$\overline{Y1}$
CLR
+5V
D
S
Q
$\overline{PRELOAD}$
CLK
U4
PRELOAD
FF
$\overline{Q}$
PRELOAD
FROM
SHT 1
$\overline{PLC}$
R
FROM
PLL BOARD
CLKIN
FROM
SHT 3
DIVO-3
4
FROM
SHT 3
$\overline{ST0}$
U20
SAMPLE
RATE
DIVIDER
13
U18
8
TP7
MR
$\overline{STATUS}$
FROM
SHT
1
$\overline{RESET}$
S
U14
S/R
LATCH
9
R
MR
1/2 U16
ADDRESS
COUNTER
$\overline{CLK}$
Q0
Q1
Q2
Q3
MR
CLK
1/2 U16
ADDRESS
COUNTER
Q1
Q0
FROM
SHT 3
$\overline{STI}$
$\overline{CLK}$
ADDRESS BUS AB1-6
FROM
SHT 1
μ PROC R/$\overline{W}$
AQSR/$\overline{W}$
RMXSEL
FROM
SHT 3
MEMREQ
+5V
U13
11
U13
8
$\overline{SIGRAM}$
FROM
SHT 1
$\overline{REFRAM}$
$\overline{AQSOE}$
FROM
SHT 3

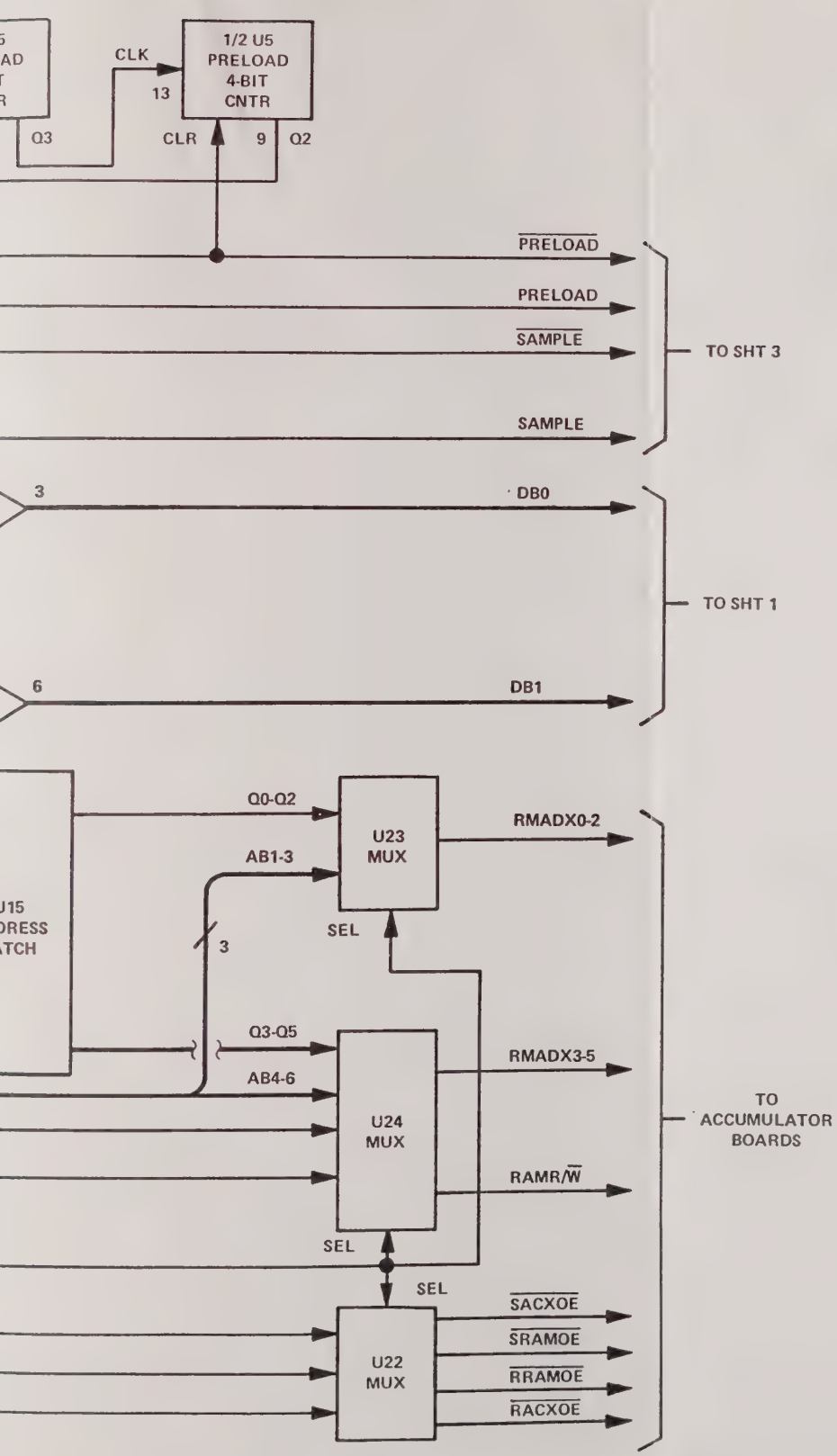
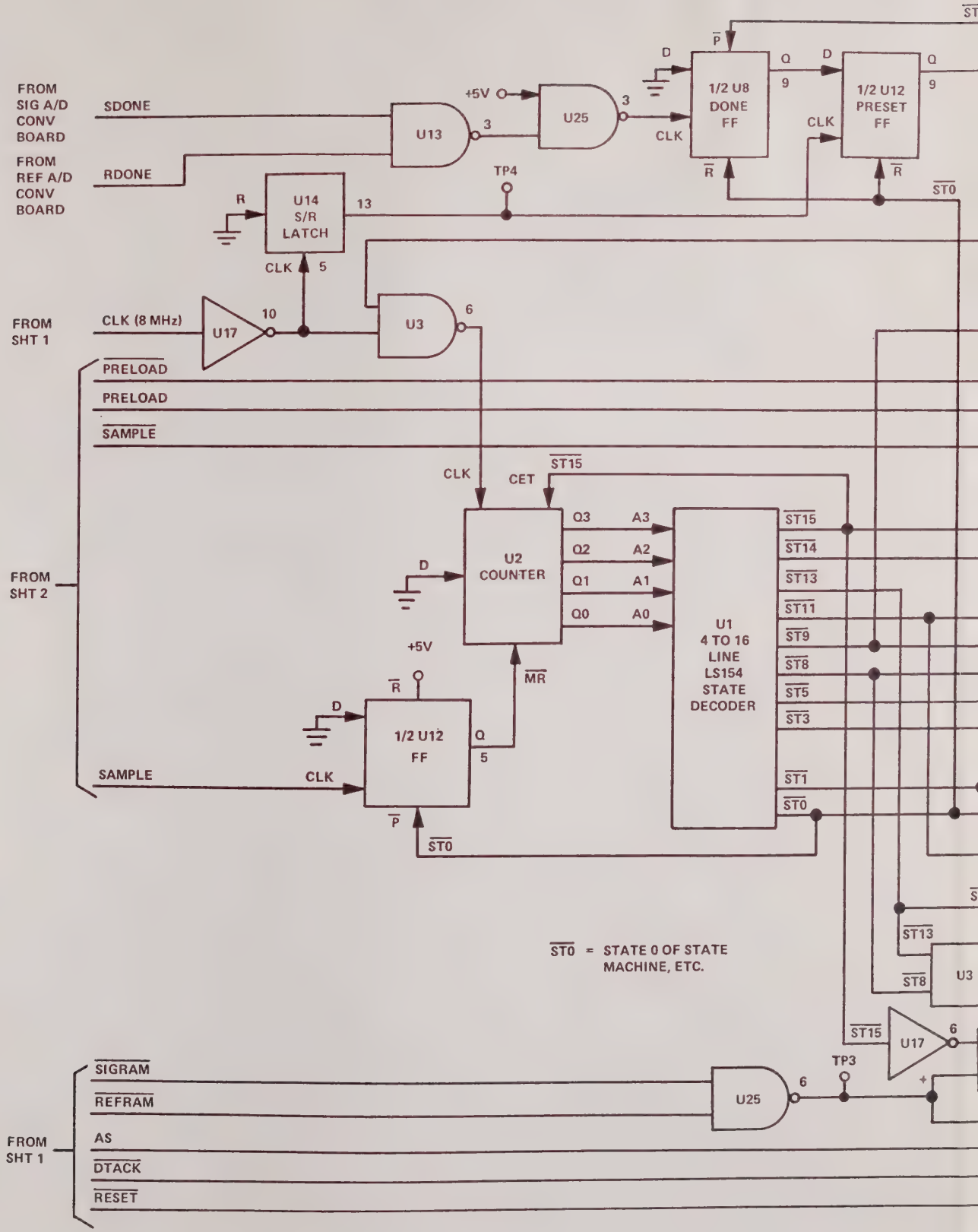


Figure 2-11. Timing and Control Board A4, Functional Signal Flow Diagram (Sheet 2 of 3)


FROM SIG A/D CONV BOARD
SDONE
FROM REF A/D CONV BOARD
RDONE
U13
+5V
U25
1/2 U8 DONE FF
1/2 U12 PRESET FF
CLK
TP4
U14 S/R LATCH
FROM SHT 1
CLK (8 MHz)
U17
U3
PRELOAD
PRELOAD
SAMPLE
FROM SHT 2
CET
ST15
U2 COUNTER
Q3
Q2
Q1
Q0
A3
A2
A1
A0
U1 4 TO 16 LINE LS154 STATE DECODER
ST15
ST14
ST13
ST11
ST9
ST8
ST5
ST3
ST1
ST0
MR
1/2 U12 FF
SAMPLE
CLK
ST0 = STATE 0 OF STATE MACHINE, ETC.
ST13
ST8
U3
ST15
U17
TP3
SIGRAM
REFRAM
U25
FROM SHT 1
AS
DTACK
RESET

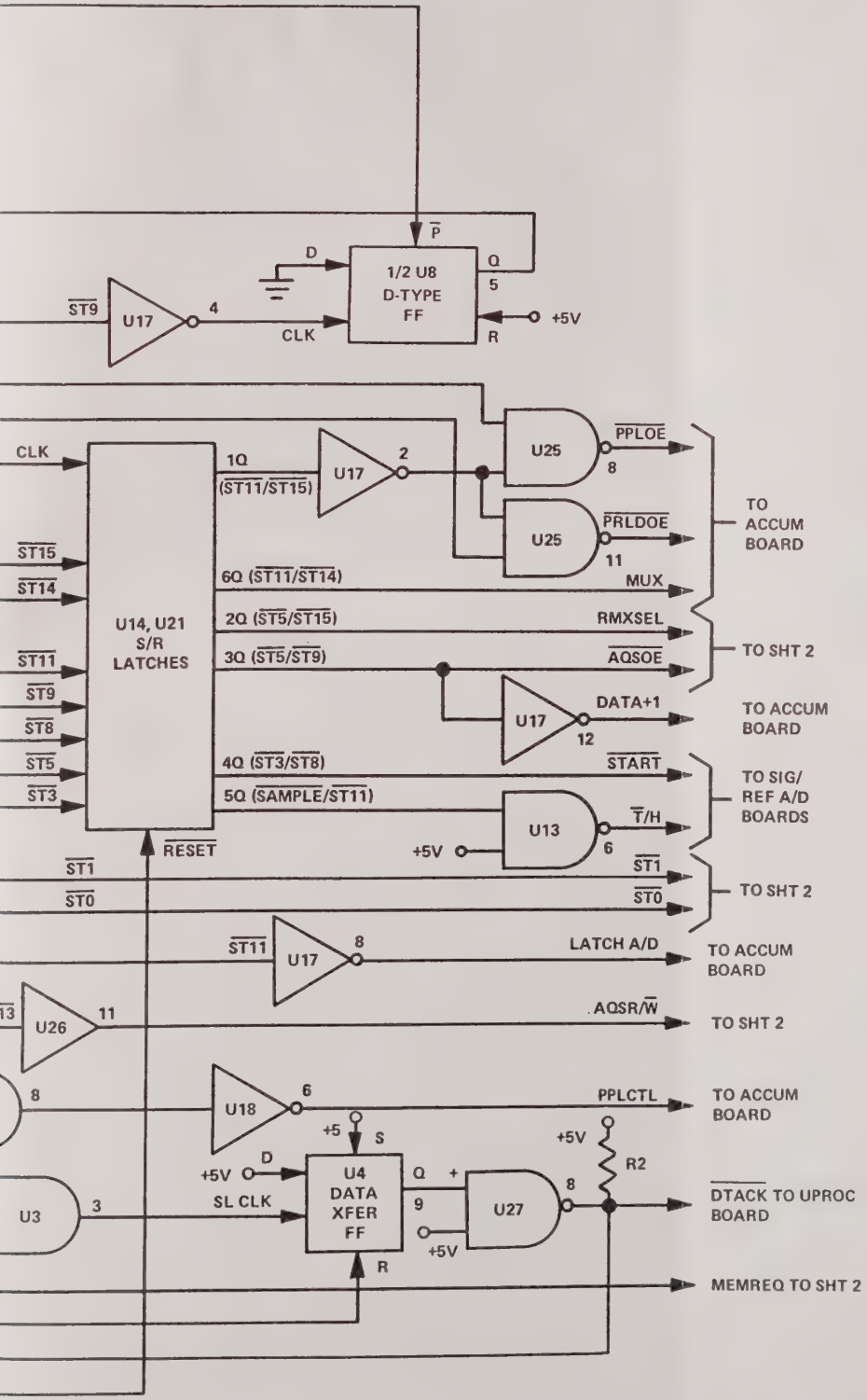


Figure 2-11. Timing and Control Board A4, Functional Signal Flow Diagram (Sheet 3 of 3)

9. Frequency multiplier frequency ($\overline{\text{FMLFRQ}}$) enable for generation of three bits representing buffer reference select (BREFSL), buffer signal select (BSIGSL), and frequency select (FRQSL0) for determination of the measurement frequency (FRQMSR) on PLL board A5.

A. Sweep byte ($\overline{\text{SWPBYT}}$) enable to PLL board A5 for selection of initial PLL frequency input range (2 kHz).

B. Frequency multiplier control ($\overline{\text{FMLCTL}}$) enable for generation of three coded binary bits - PLLFS0-2 - representing PLL frequency range to PLL board A5.

C. An overload detect ($\overline{\text{OD}}$) enable to strobe the signal/reference overload signals to the data bus, and into the overload detector on the signal/reference accumulators.

D. A chip select enable for the programmable timer, and a bus transceiver for data transfer in either direction between the programmable timer and the data bus.

E. A signal RAM ($\overline{\text{SIGRAM}}$) enable for generation of signal accumulator transmit and RAM output enables to signal accumulator A6.

F. A reference RAM ($\overline{\text{REFRAM}}$) enable for generation of reference accumulator transmit and RAM output enables to reference accumulator A7.

(2) Frequency Measurement and Blink Timing. Timing and control board A4 contains a timer IC which has 3 internal timers. Two of these timers are used for frequency measurement. A third is used to provide timing for front panel display blinking functions. An output from PLL A5, FRQMSR, is supplied to timing and control board A4 as the frequency to be measured. The state of $\overline{\text{FRQSL0}}$ determines whether or not FRQMSR represents the input reference signal frequency, or a PLL loop feedback frequency. This PLL loop signal is frequency and phase-locked to the fundamental of the incoming frequency under test. The timer uses the frequency measure signal (FRQMSR) to gate the 8 MHz clock into the timer. When the timer underflows, an interrupt is produced.

When the microprocessor receives the $\overline{\text{TIMER}}$ interrupt, it places an interrupt level on address bus lines AB1-3 and asserts the internal interrupt request acknowledge ($\overline{\text{IRQACK}}$) based on the function code; this interrupt request acknowledge is decoded to produce a valid peripheral address ($\overline{\text{VPA}}$) input. The microprocessor then asserts the address strobe ($\overline{\text{AS}}$) to timing and control board A4. The microprocessor then branches to the default interrupt vector for that interrupt level. The interrupt service routine polls the timer to determine which of the 3 timers has produced the interrupt.

During certain DAV measurement modes and conditions, a blinking indication (annunciator or LED) is provided to alert the user. For example, the CAL key LED flashes, if no previous calibration sequence has occurred at that frequency. The blinking indication under these conditions is generated by the $\overline{\text{TIMER}}$ interrupt (INT 6) to the microprocessor from timing and control board A4. The microprocessor handles this interrupt in the same manner as the frequency counter interrupt.

(3) Data Acquisition and Timing. CLKIN, a signal generated by PLL board A5 which is either 16 or 64 times the DAV input frequency, when received by timing and control board A4, is frequency divided by a factor depending on the frequency being measured as determined by the program logic.

As a result, sample pulses are produced which are used to synchronize the start of a state machine which consists of a counter, a 1 of 16 decoder, and other logic. Once started, this state machine generates 16 event state outputs, synchronous to the microprocessor 8 MHz clock, to provide the required control timing signals for data acquisition and processing. These signals include the following:

(a) $\overline{\text{Track}}$/hold ($\overline{\text{T}}$/H) goes low to hold data at the output of the track/hold amplifier in the signal/reference A/D converters A12/A9.

(b) A preload output enable ($\overline{\text{PRLDOE}}$) is generated to load parallel A/D data from the A/D data bus to the RAM data bus in the accumulators A6/A7.

(c) A RAM address select is generated to enable selection of RAM addresses RMADX0-5 for accumulator RAM, based on bus address AB1-6 from the microprocessor.

(d) An acquisition output enable is produced and used to generate accumulator RAM output enables ($\overline{\text{SRAMOE}}$ and $\overline{\text{RRAMOE}}$).

(e) The DATA +1 signal is generated for the calculation of 15/16 of the current value of the data sample in accumulator RAM.

(f) A START command is generated and sent to A/D converter boards A12/A9 to initiate the signal digitizing process.

(g) A partial product latch control (PPLCTL) is sent to accumulators A6/A7 to latch 15/16th of the previous conversion in the partial product latches.

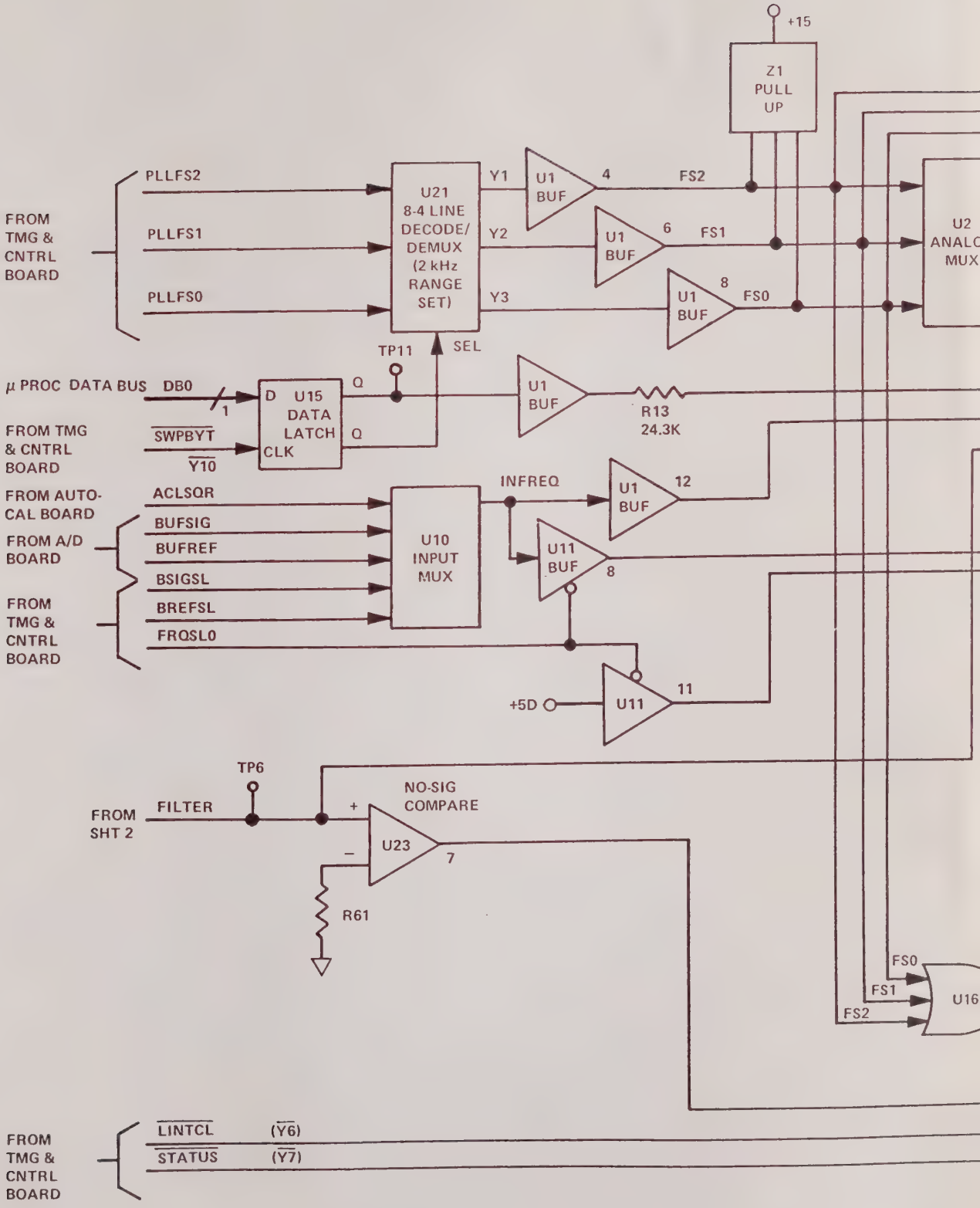
(h) A latch A/D (LATCH A/D) signal is produced to latch the incoming serial data from A/D converters A12/A9 into the parallel input latches in accumulators A6/A7.

(i) The partial product latch output enable ($\overline{\text{PPLOE}}$) is asserted to place 15/16th of the previous data on the accumulator RAM data bus.

(j) A MUX signal is generated to transfer A/D bus data to the output of the accumulator multiplexers (1/16th of the value of the A/D converter data).

b. PHASE-LOCKED LOOP BOARD A5. (See figure 2-12 for details of functional signal flow on Phase-Locked Loop board A5.)

PLL board A5 provides frequency/phase synchronization for the data sampling process by generating both a frequency measurement signal output and a sample clock which is 64 or 16 times the input signal frequency. Synchronization of the output signals to the incoming signal is accomplished by comparison of the input signal frequency (BUFREF, BUFSIG, or ACLSQR) to the frequency established in a phase lock servo loop.


+15
Z1
PULL
UP
FROM
TMG &
CNTRL
BOARD
PLLFS2
PLLFS1
PLLFS0
U21
8-4 LINE
DECODE/
DEMUX
(2 kHz
RANGE
SET)
Y1
Y2
Y3
U1
BUF
4
6
8
FS2
FS1
FS0
U2
ANALO
MUX
TP11
SEL
μ PROC DATA BUS
DB0
1
D
U15
DATA
LATCH
CLK
Q
FROM TMG
& CNTRL
BOARD
SWPBYT
Y10
R13
24.3K
FROM AUTO-
CAL BOARD
FROM A/D
BOARD
FROM
TMG &
CNTRL
BOARD
ACLSQR
BUFSIG
BUFREF
BSIGSL
BREFSL
FRQSL0
U10
INPUT
MUX
INFREQ
U11
BUF
12
8
+5D
U11
11
TP6
FROM
SHT 2
FILTER
NO-SIG
COMPARE
+
–
U23
7
R61
FS0
FS1
FS2
U16
FROM
TMG &
CNTRL
BOARD
LINTCL
STATUS
(Y6)
(Y7)

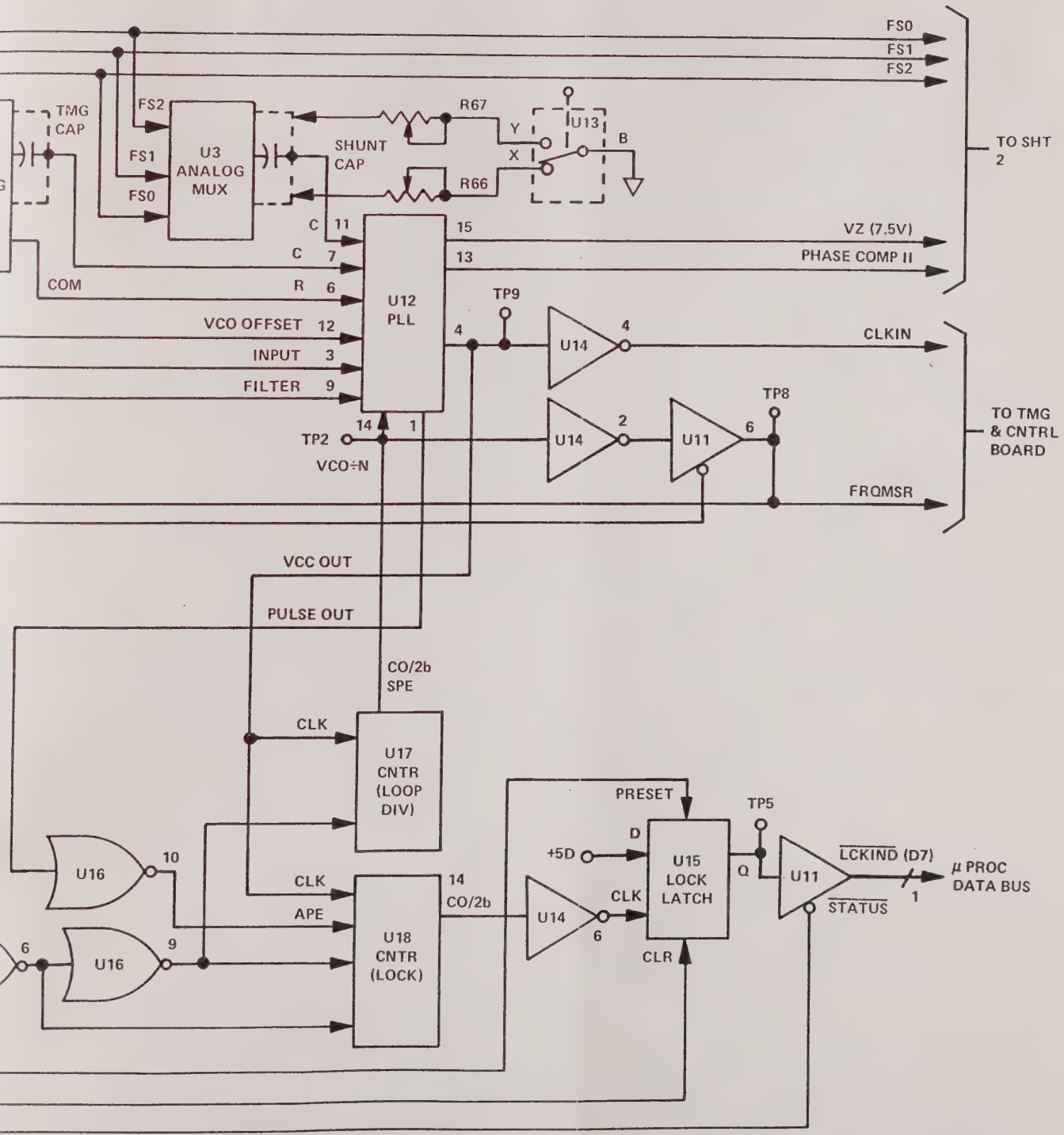
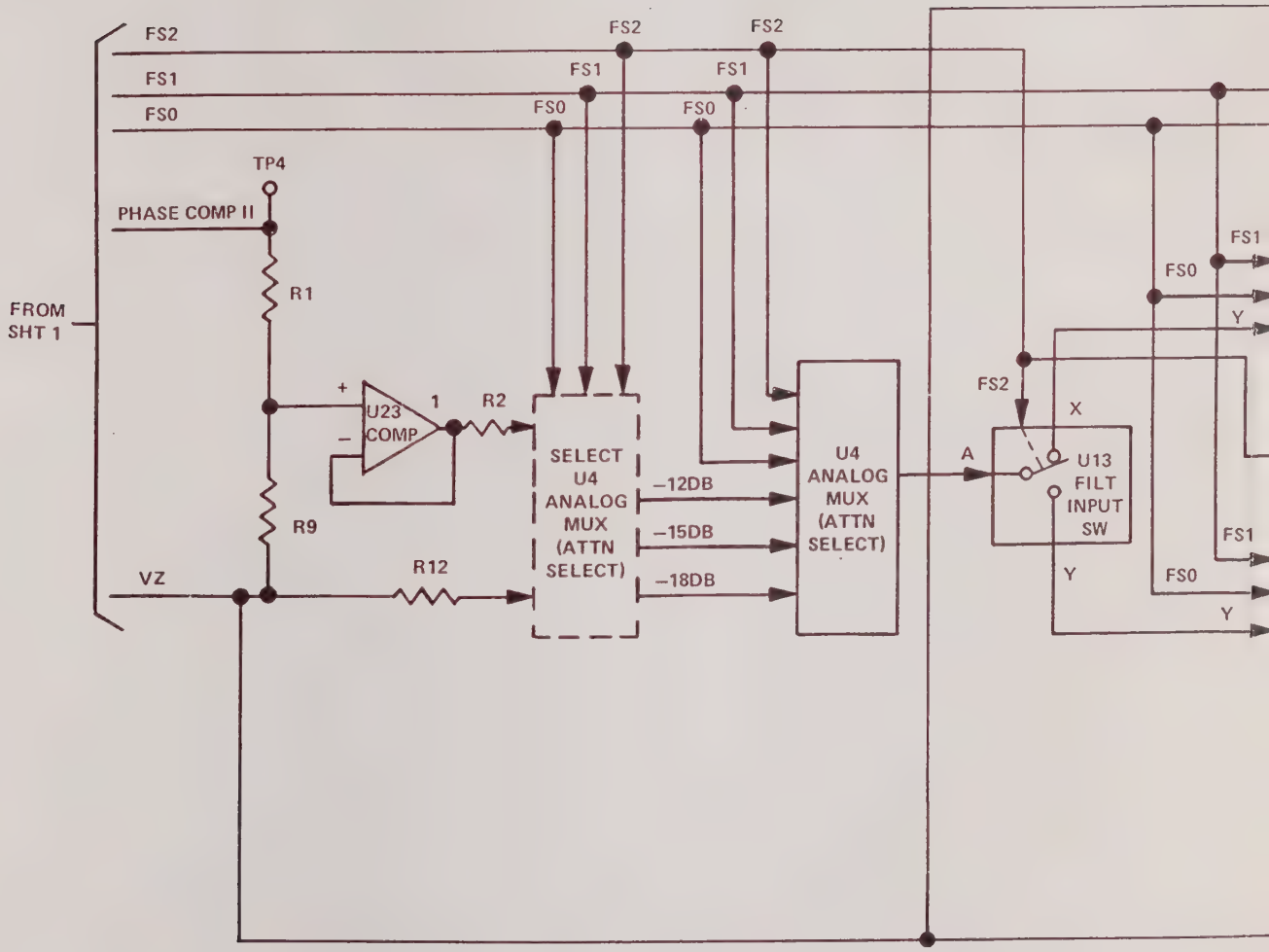


Figure 2-12. Phase-Locked Loop Board A5, Functional Signal Flow Diagram (Sheet 1 of 2)


FS2
FS1
FS0
TP4
PHASE COMP II
FROM SHT 1
R1
R9
VZ
R12
U23 COMP
R2
SELECT U4 ANALOG MUX (ATTN SELECT)
-12DB
-15DB
-18DB
U4 ANALOG MUX (ATTN SELECT)
A
U13 FILT INPUT SW
X
Y

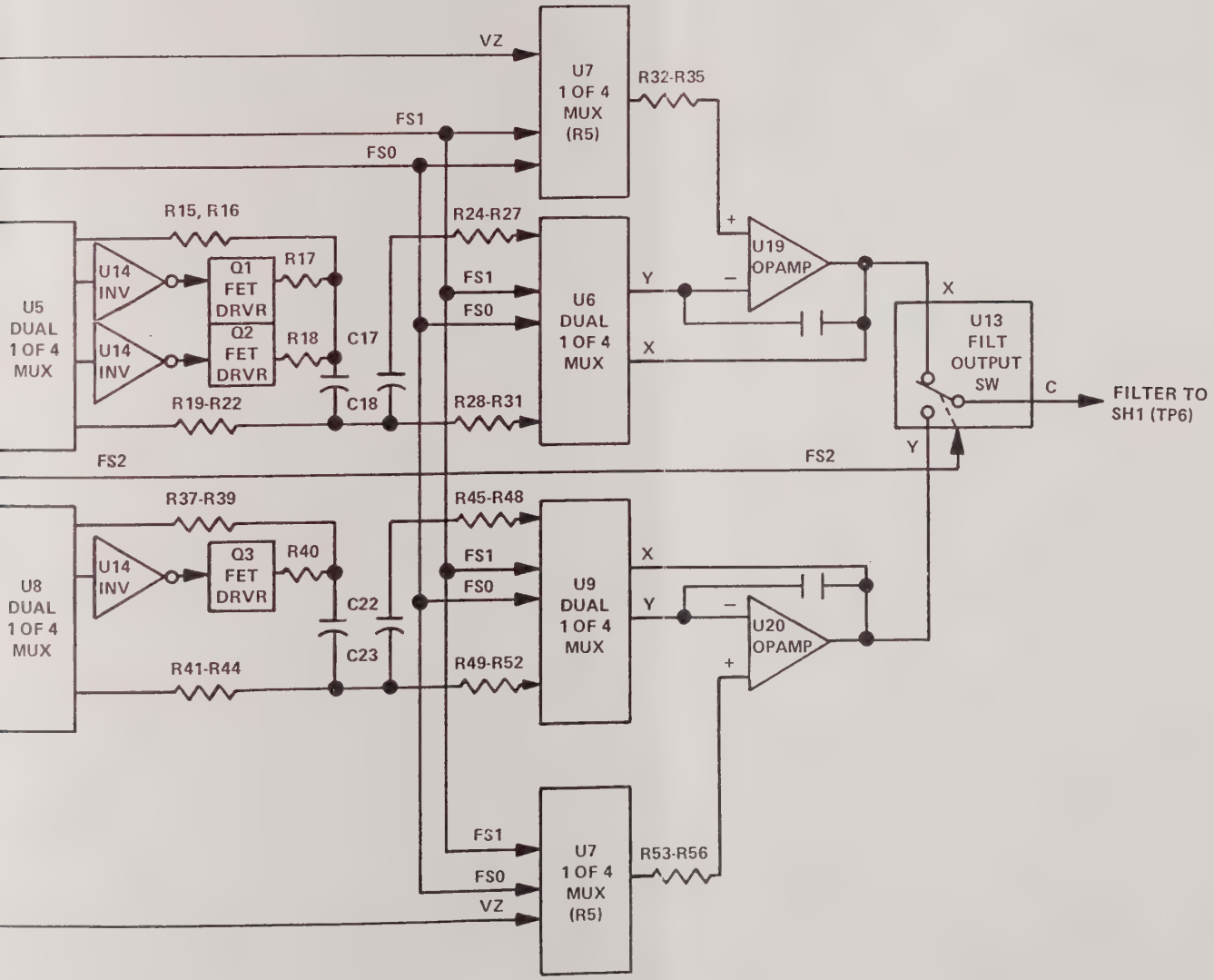


Figure 2-12. Phase-Locked Loop Board A5, Functional Signal Flow diagram (Sheet 2 of 2)

When input frequency is below 28.5 kHz, the feedback loop provides a multiplication factor of 64, while a factor of 16 is provided for frequencies above 28.5 kHz. The reference zero crossing square wave signal and the autocalibration squarewave signal are applied to an input multiplexer which provides selection of either of these inputs depending on the state of the BREFSL and BSIGSL select bits from timing and control board A4.

The resulting input frequency signal (INFRQ) provides the input to the precision phase-locked loop circuit which consists of a phase detector/VCO chip, digital loop dividers, lock detection logic, and eight selectable loop filters. One loop filter is selected for each of the following eight frequency bands:

PLL BAND	FREQUENCY
0	28.5 kHz - 100 kHz
1	10.6 kHz - 28.5 kHz
2	3.16 kHz - 10.6 kHz
3	1 kHz - 3.16 kHz
4	316 Hz - 1 kHz
5	100 Hz - 316 Hz
6	32 Hz - 100 Hz
7	10 Hz - 32 Hz

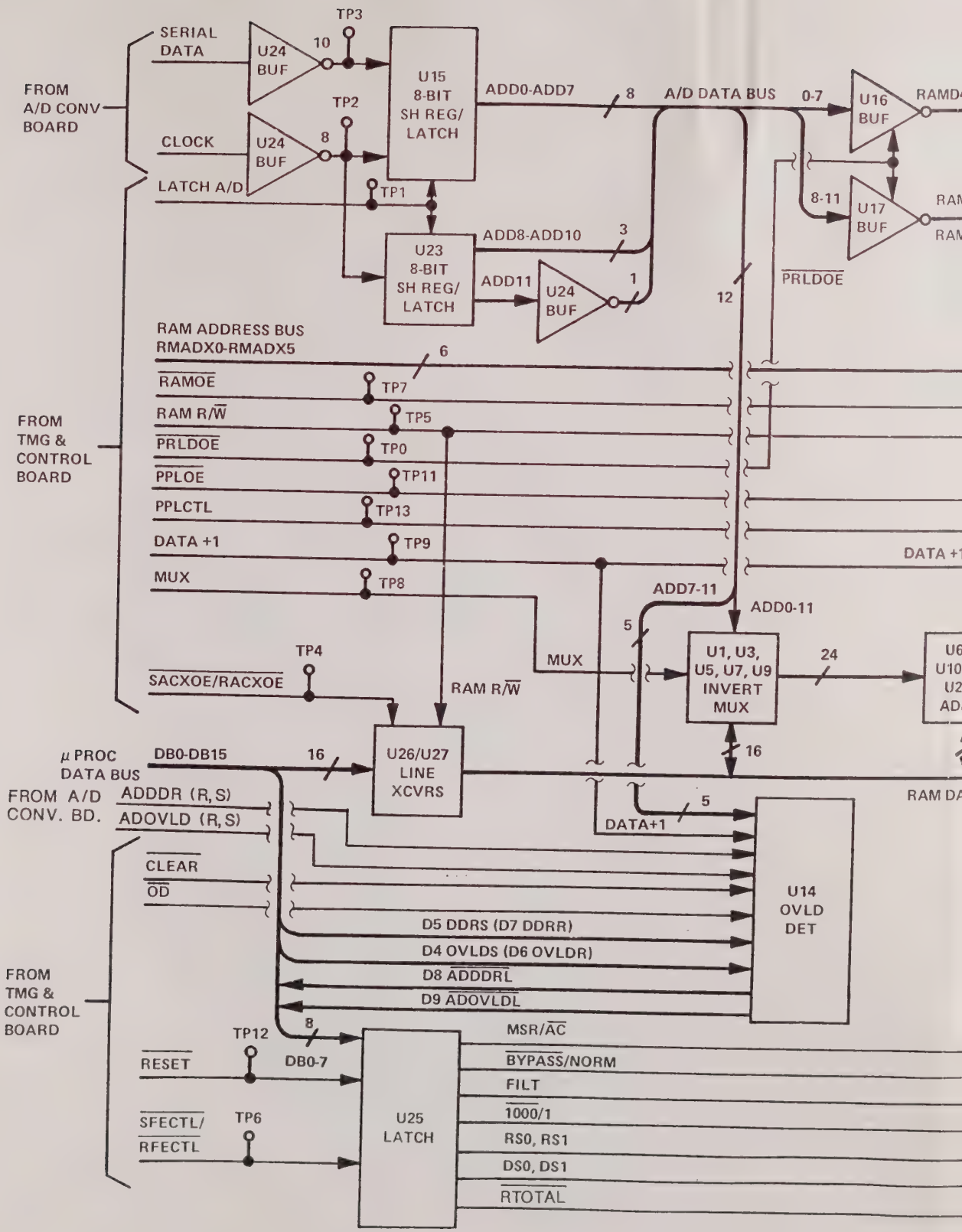
When the PLL has locked, the output frequency, CLKIN, is synchronized to the incoming signal under test. Since a digital divider is included in the loop, the loop output signal, CLKIN, is frequency multiplied by the loop division factor, which is always 64 or 16. Another signal, FRQMSR, which is used for frequency measurement, is not divided and has the same frequency as the input. The FRQMSR and CLKIN signals are supplied to timing and control board A4.

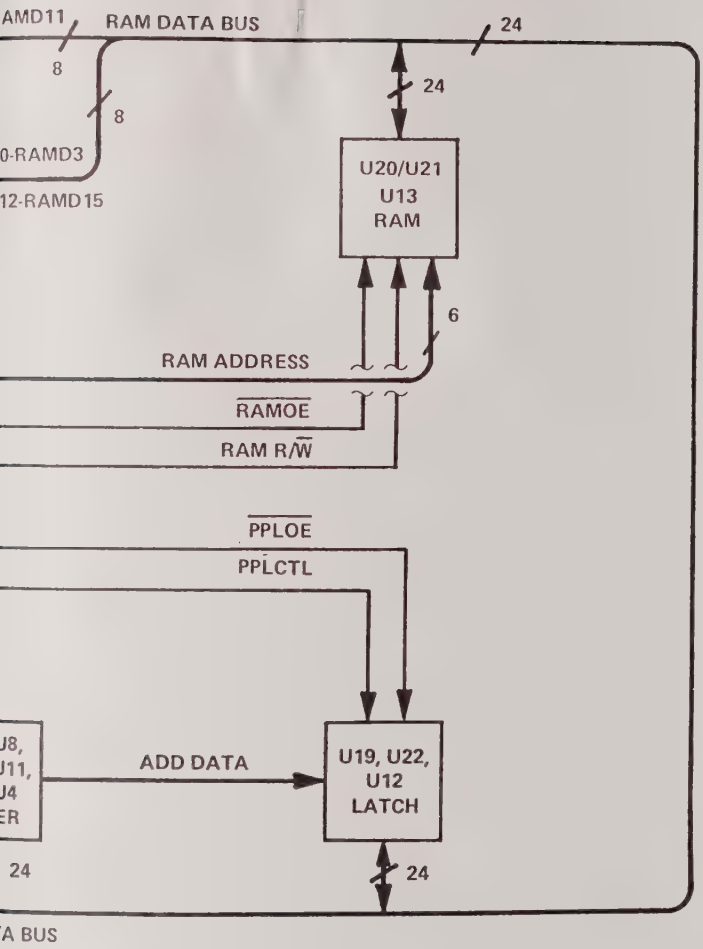
c. ACCUMULATOR BOARDS A6/A7. (See figure 2-13 for details of functional signal flow on Accumulator boards A6/A7.)

The event sequences controlling the accumulator data acquisition and averaging processes are initiated by timing and control board A4 in response to the CLKIN signal from PLL A5.

The digitized representation of the signal and reference inputs are supplied in serial form, together with a clock signal, from the A/D converters A12/A9. This data is clocked into the accumulator input latches and is latched to the accumulator A/D data bus, in parallel format, by the LATCH A/D signal. This data is then strobed to the RAM data bus by a preload output enable ($\overline{\text{PRLDOE}}$). This initial preload only occurs when a range or mode of measurement is changed. The RAM data is written to and read from RAM locations using the RAM R/$\overline{\text{W}}$ signal, when proper RAM locations are specified by the RAM address RAMDX0-5.

In general, the A/D data, consisting of 12 bits, is applied to a group of multiplexers. The multiplexers either select the A/D data inputs, or the RAM data from the RAM data bus; when the multiplexer outputs are equivalent to 1/16th of the old sample on the RAM data bus, and they are applied to a group of adders and summed with the old data present on the RAM data bus, together with a DATA +1 input (binary 1's complement). The resultant sample is equivalent to 15/16ths of the old data, which is stored in a group of latches. This process continues, whereby 1/16th of each new data sample is routed to the output of the multiplexers and is added to


FROM A/D CONV BOARD
SERIAL DATA
CLOCK
LATCH A/D
U24 BUF
10
8
TP3
TP2
TP1
U15 8-BIT SH REG/ LATCH
ADD0-ADD7
8
A/D DATA BUS
0-7
U16 BUF
RAMD
8-11
U17 BUF
RAM
RAM
U23 8-BIT SH REG/ LATCH
ADD8-ADD10
3
ADD11
U24 BUF
1
12
PRLDOE
RAM ADDRESS BUS RMADX0-RMADX5
6
FROM TMG & CONTROL BOARD
RAMOE
TP7
RAM R/W
TP5
PRLDOE
TP0
PPLOE
TP11
PPLCTL
TP13
DATA +1
TP9
MUX
TP8
DATA +1
ADD7-11
ADD0-11
5
TP4
SACXOE/RACXOE
MUX
RAM R/W
U1, U3, U5, U7, U9 INVERT MUX
24
16
μ PROC DATA BUS
DB0-DB15
16
U26/U27 LINE XCVRS
RAM DA
FROM A/D CONV. BD.
ADDDR (R, S)
ADOVLD (R, S)
DATA+1
5
CLEAR
OD
U14 OVLD DET
D5 DDRS (D7 DDRR)
D4 OVLDS (D6 OVLDR)
D8 ADDDRL
D9 ADOVLDL
FROM TMG & CONTROL BOARD
8
TP12
RESET
DB0-7
SFECTL/ RFECTL
TP6
U25 LATCH
MSR/AC
BYPASS/NORM
FILT
1000/1
RS0, RS1
DS0, DS1
RTOTAL



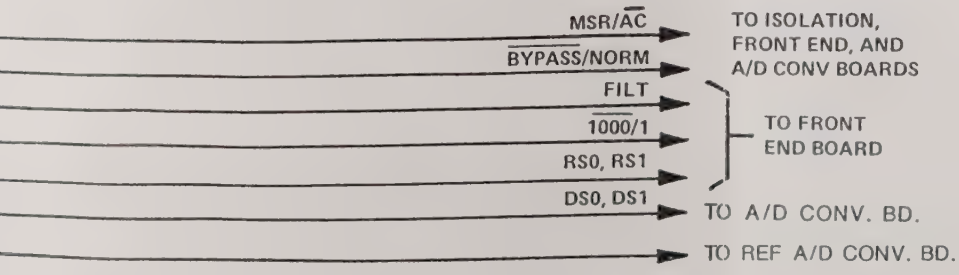


Figure 2-13. Accumulator Board A6/A7, Functional Signal Flow Diagram

15/16ths of the previous data sample, thus providing continuous sample averaging and update of each of the 64 samples. Each sample of averaged data is written into appropriate RAM locations specified by the RAM address generated by timing and control board A4. Signal and reference data is averaged at the same time. When each data sample has been acquired and processed, the RAM data is made available for transfer to the microprocessor data bus on a microprocessor read cycle (RAMR/$\overline{W}$ high). The microprocessor may read all 64 samples or less depending on the available time between samples. Averaging then takes place on the next sample. The microprocessor then performs the required DFT calculations on the sampled data.

2-8. DISPLAY/KEYBOARD SECTION FUNCTIONAL DESCRIPTION. (See figure 2-14)

The display function consists of display driver board A15A2 and display board A15A3; this function, when considered with integral keyboard A15A1, provides an interface between the DAV and the user.

a. DISPLAY DRIVER BOARD A15A2. (See figure 2-15 for details of functional signal flow on Display Driver board A15A2.)

As a synchronous peripheral device, display driver board A15A2 receives the microprocessor address contained in bits AB1-3 and 17-23; when the address strobe is received, the display driver issues 6800 to the microprocessor, indicating it to be a valid peripheral device. The microprocessor then sets the R/$\overline{W}$ input and asserts $\overline{VMA}$, indicating a valid memory address is on the bus. Data on the microprocessor bus is transferred to the display driver bus on a write cycle, whereby display data

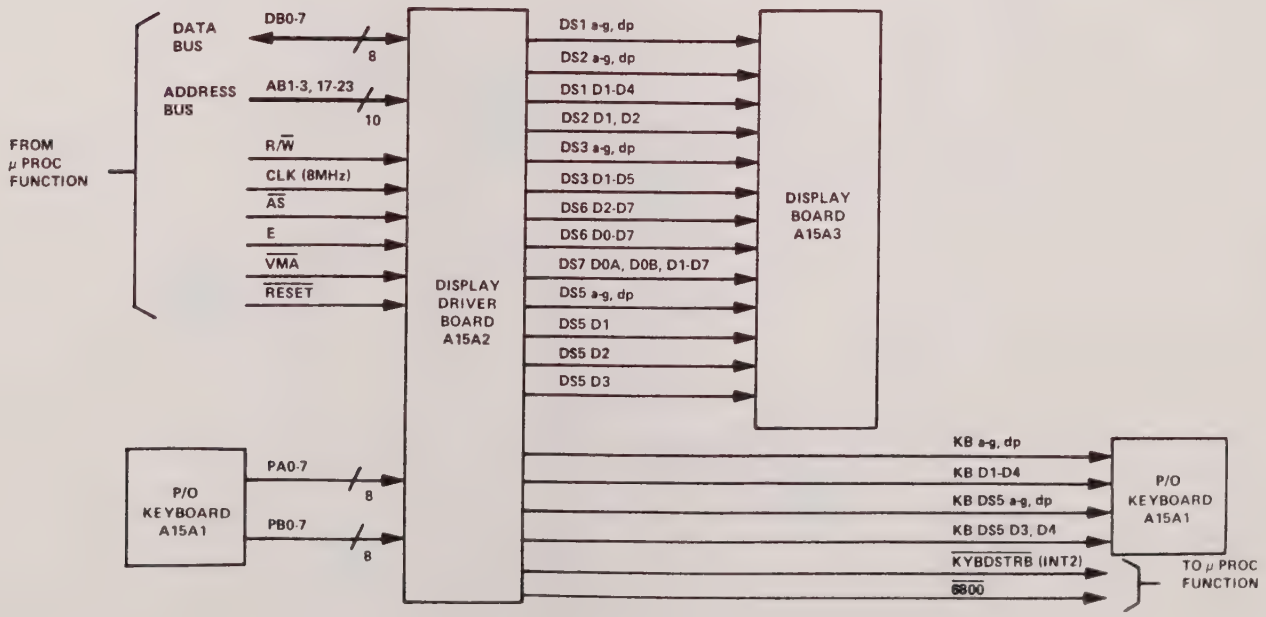
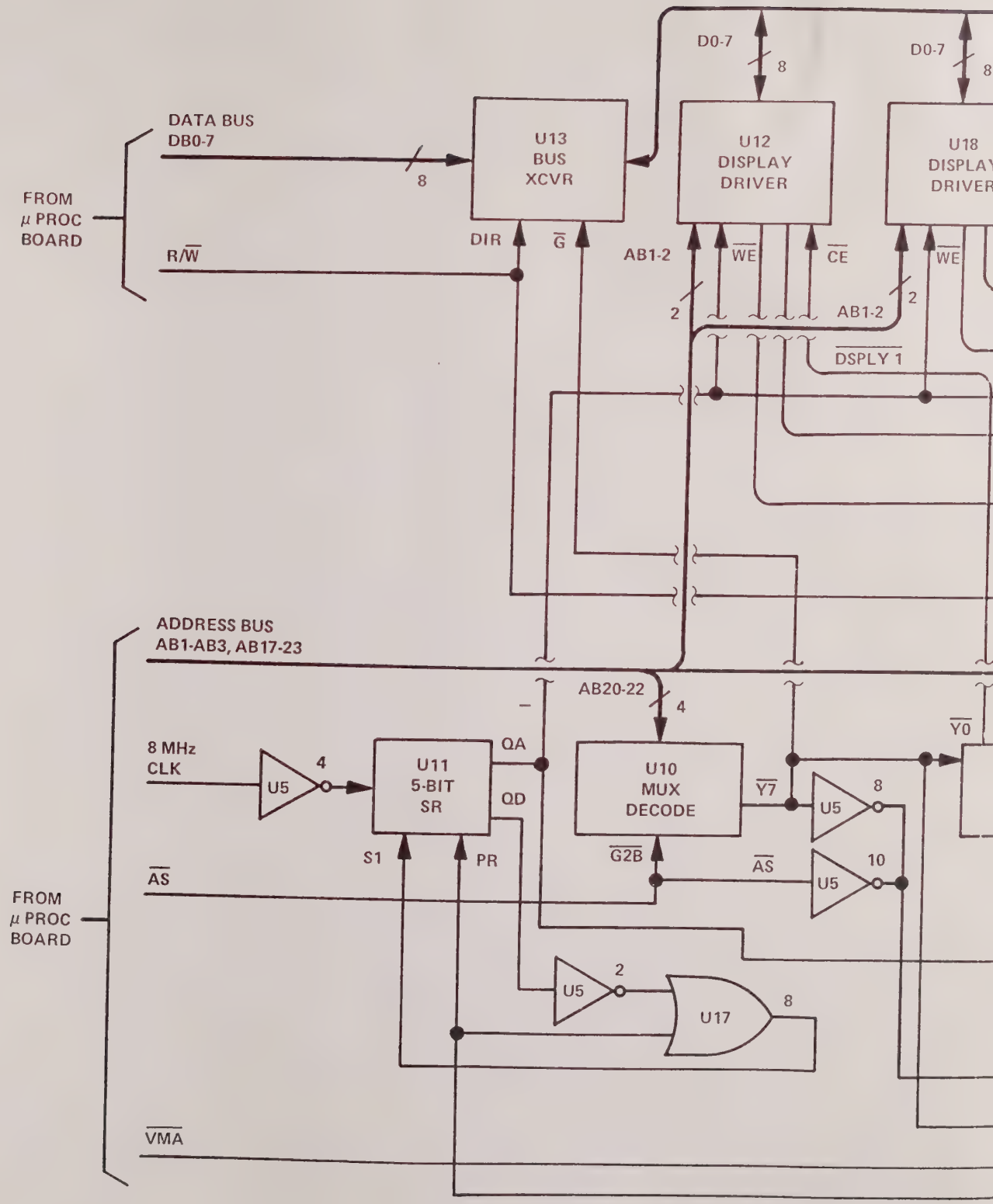


Figure 2-14. Display Function, Simplified Functional Diagram


DATA BUS
DB0-7
8
FROM
μ PROC
BOARD
R/W
U13
BUS
XCVR
DIR
G
D0-7
8
U12
DISPLAY
DRIVER
AB1-2
2
WE
CE
U18
DISPLAY
DRIVER
D0-7
8
WE
AB1-2
2
DSPLY 1
ADDRESS BUS
AB1-AB3, AB17-23
AB20-22
4
8 MHz
CLK
U5
4
U11
5-BIT
SR
QA
QD
S1
PR
U10
MUX
DECODE
G2B
Y7
Y0
U5
8
AS
U5
10
FROM
μ PROC
BOARD
U5
2
U17
8
VMA

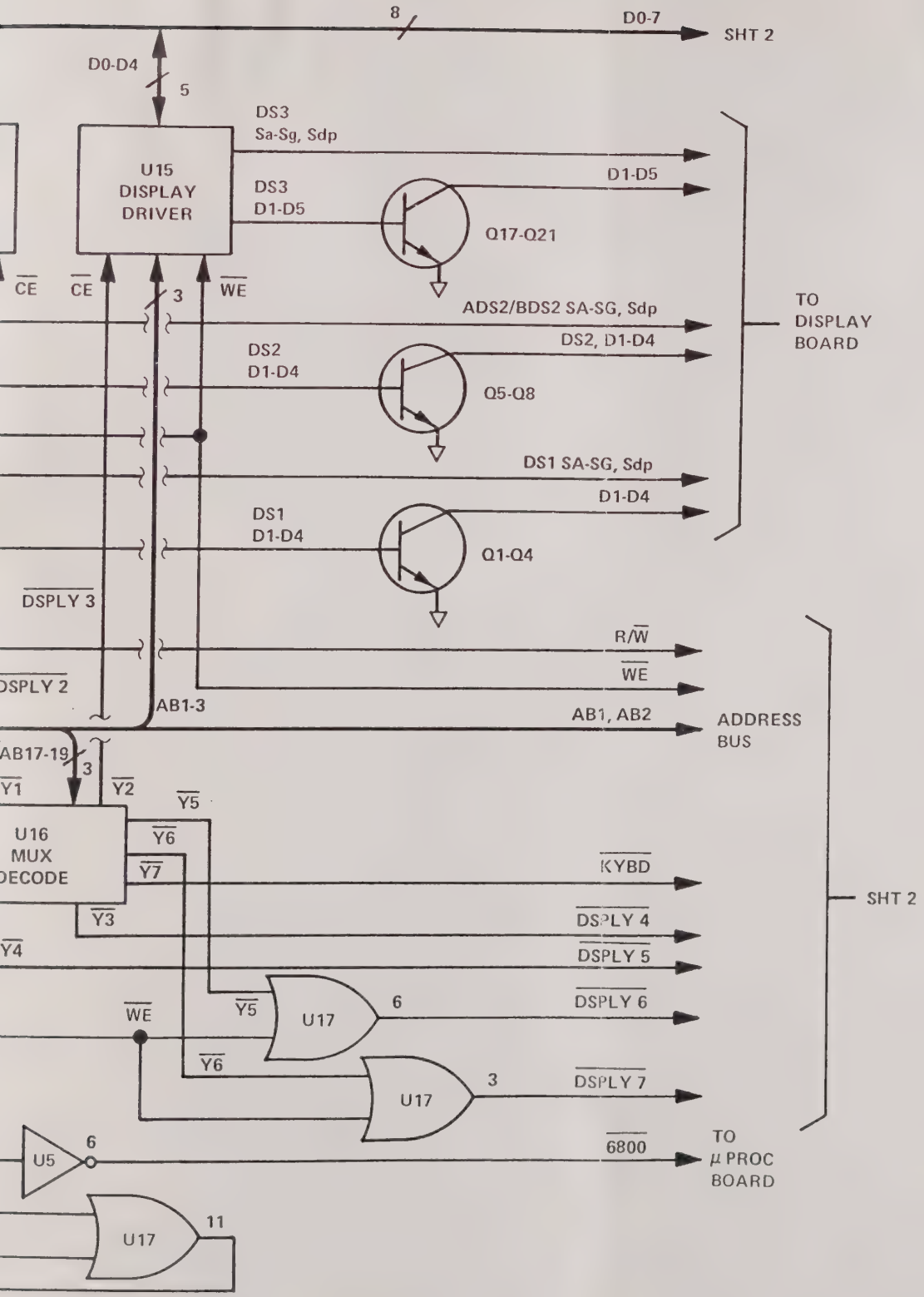
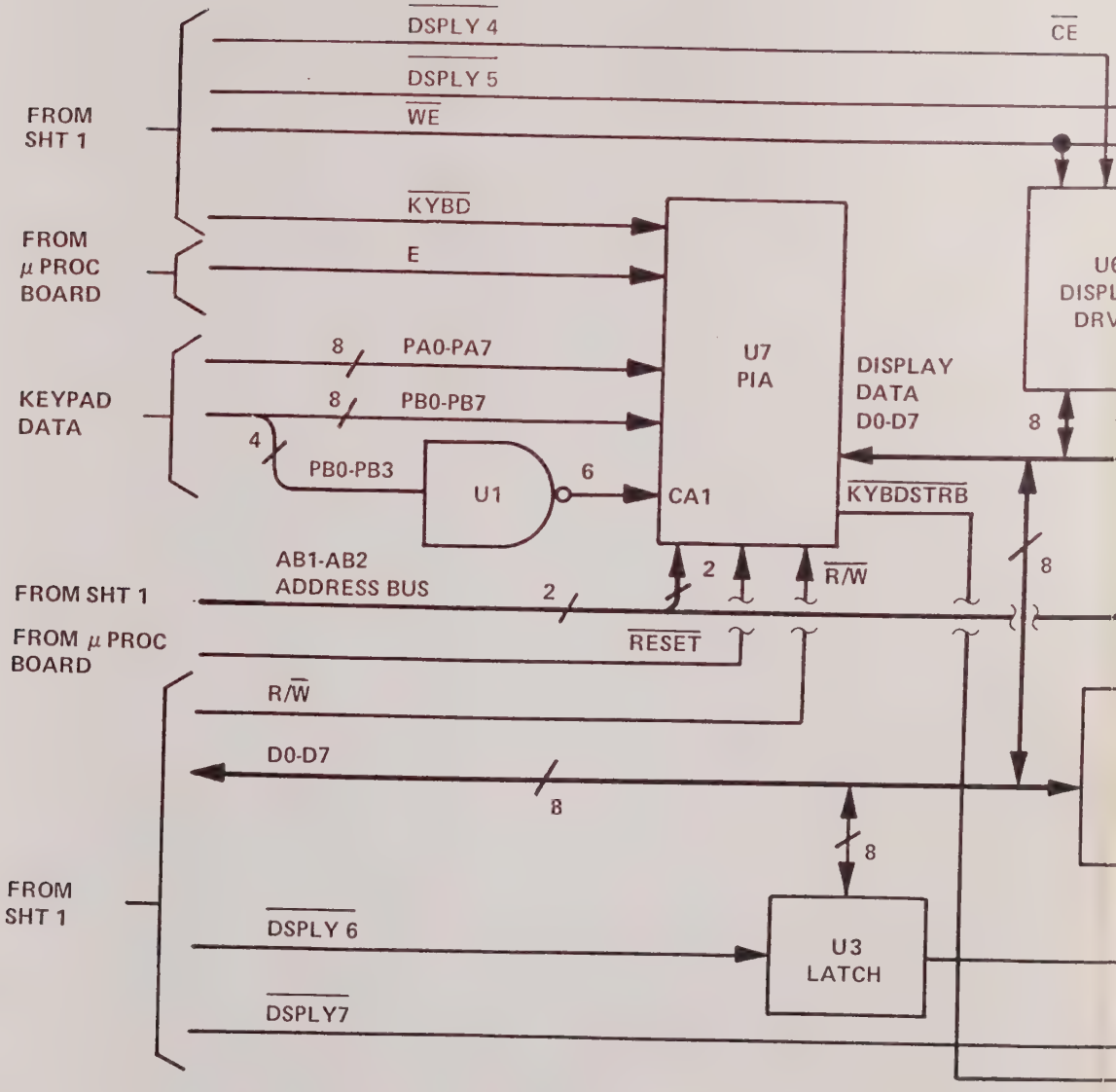


Figure 2-15. Display Driver Board A15A2, Functional Signal Flow Diagram (Sheet 1 of 2)


DSPLY 4
DSPLY 5
WE
CE
FROM SHT 1
KYBD
E
FROM μ PROC BOARD
8
PA0-PA7
8
PB0-PB7
KEYPAD DATA
4
PB0-PB3
U1
6
U7 PIA
CA1
DISPLAY DATA D0-D7
8
KYBDSTRB
AB1-AB2 ADDRESS BUS
2
2
R/W
8
FROM SHT 1
FROM μ PROC BOARD
RESET
R/W
D0-D7
8
8
FROM SHT 1
DSPLY 6
DSPLY7
U3 LATCH

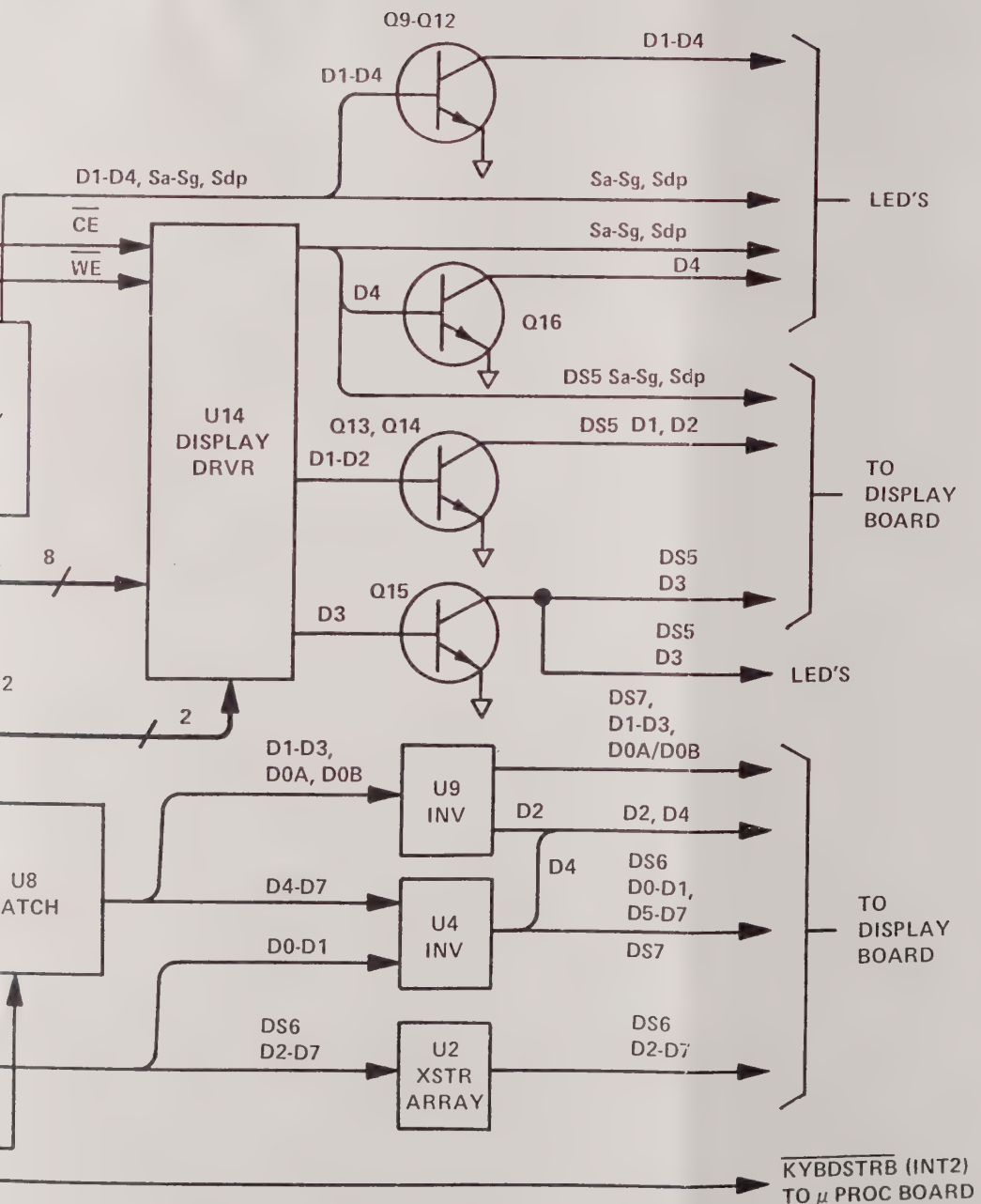


Figure 2-15. Display Driver Board A15A2, Functional Signal Flow Diagram (Sheet 2 of 2)

appears at the inputs to the display drivers and latches. On a read cycle, data, consisting of keyboard inputs from a peripheral interface adapter (PIA), is read to the microprocessor data bus.

The microprocessor address bus information contained in bits AB17-22 is decoded to generate seven sequential display strobes, one for each of the display drivers and one for the display latch. Display data is written into the drivers by the combination of microprocessor address bits AB1-3 and a write enable ($\overline{WE}$) strobe generated by a shift register which is clocked by the 8 MHz microprocessor input. The output data is strobed from the display drivers and latch to the display board which contains the displays and LEDs.

The last display strobe generated is used to scan the PIA on a microprocessor read cycle to detect the presence of keyboard information contained in the PIA buffer registers. Synchronous data transfer to the microprocessor occurs using the microprocessor enable (E) signal.

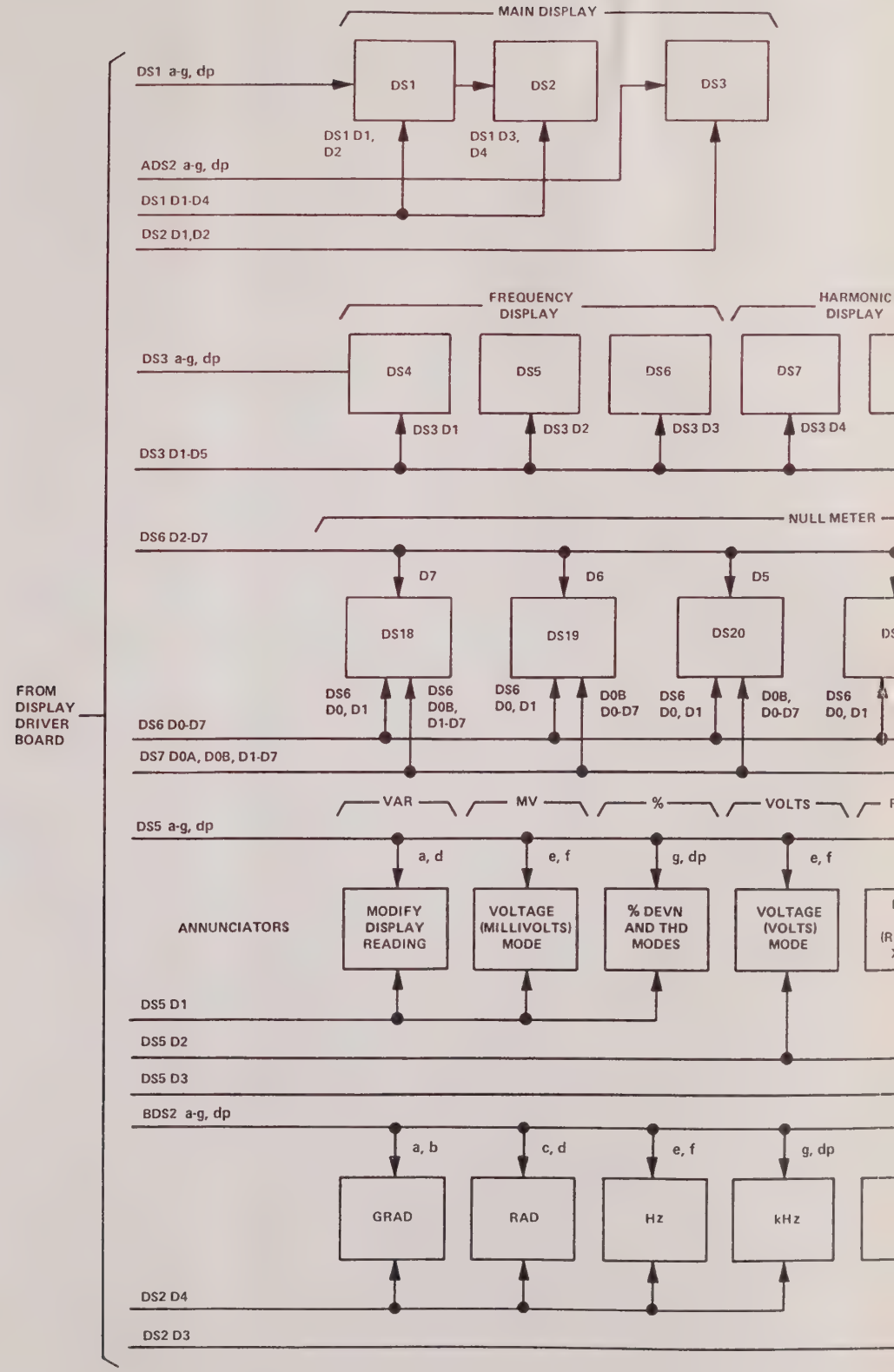
Whenever a keyboard key is pressed, a $\overline{KYBDSTRB}$ interrupt is generated and sent to the microprocessor as interrupt level 2 (INT 2); key depression is sensed by the PB0-3 inputs to the PIA.

b. DISPLAY BOARD A15A3. (See figure 2-16 for details of functional signal flow on Display board A15A3.)

The display board contains seven-segment displays, annunciator displays and null meter display. Keyboard A15A1 contains additional keypad LEDs. The main display consists of three dual-digit, 7-segment displays, DS1 through DS3, the frequency display consists of DS4 through DS6, and the harmonic display consists of DS7 and DS8. Also included on display board A15A3 are square LED annunciators for various "word" displays and a bar graph display. In addition, keyboard A15A1 has LEDs for each key.

2-9. INPUT/OUTPUT SECTION FUNCTION DESCRIPTION. (See figure 2-17.)

The Input/Output function consists of I/O board A3. I/O board A3 communicates with the microprocessor over the data bus to provide an interface with an external GPIB IEEE-488 bus. Address switch A17S1 provided on the DAV rear panel can be user-set to select the IEEE interface bus address. In addition, data operating mode format switches are provided for controlling IEEE-488 communications. I/O board A3 also converts digital in-phase and quadrature data to analog signals for external recording. Further, I/O board A3 accepts a TTL-compatible trigger signal from an external circuit to modify the front panel display or to generate service requests to the external IEEE bus or to update the track/hold mode.


MAIN DISPLAY
DS1 a-g, dp
DS1
DS2
DS3
DS1 D1, D2
DS1 D3, D4
ADS2 a-g, dp
DS1 D1-D4
DS2 D1,D2
FREQUENCY DISPLAY
HARMONIC DISPLAY
DS3 a-g, dp
DS4
DS5
DS6
DS7
DS3 D1
DS3 D2
DS3 D3
DS3 D4
DS3 D1-D5
NULL METER
DS6 D2-D7
D7
D6
D5
DS18
DS19
DS20
DS6 D0, D1
DS6 D0B, D1-D7
D0B D0-D7
FROM DISPLAY DRIVER BOARD
DS6 D0-D7
DS7 D0A, D0B, D1-D7
VAR
MV
%
VOLTS
DS5 a-g, dp
a, d
e, f
g, dp
e, f
ANNUNCIATORS
MODIFY DISPLAY READING
VOLTAGE (MILLIVOLTS) MODE
% DEVN AND THD MODES
VOLTAGE (VOLTS) MODE
DS5 D1
DS5 D2
DS5 D3
BDS2 a-g, dp
a, b
c, d
e, f
g, dp
GRAD
RAD
Hz
kHz
DS2 D4
DS2 D3

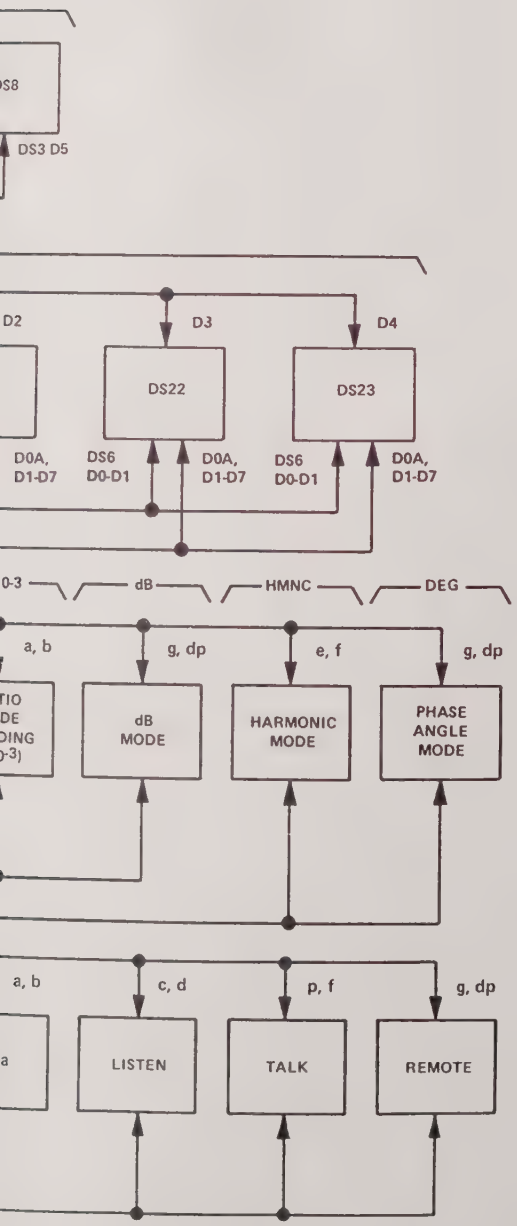
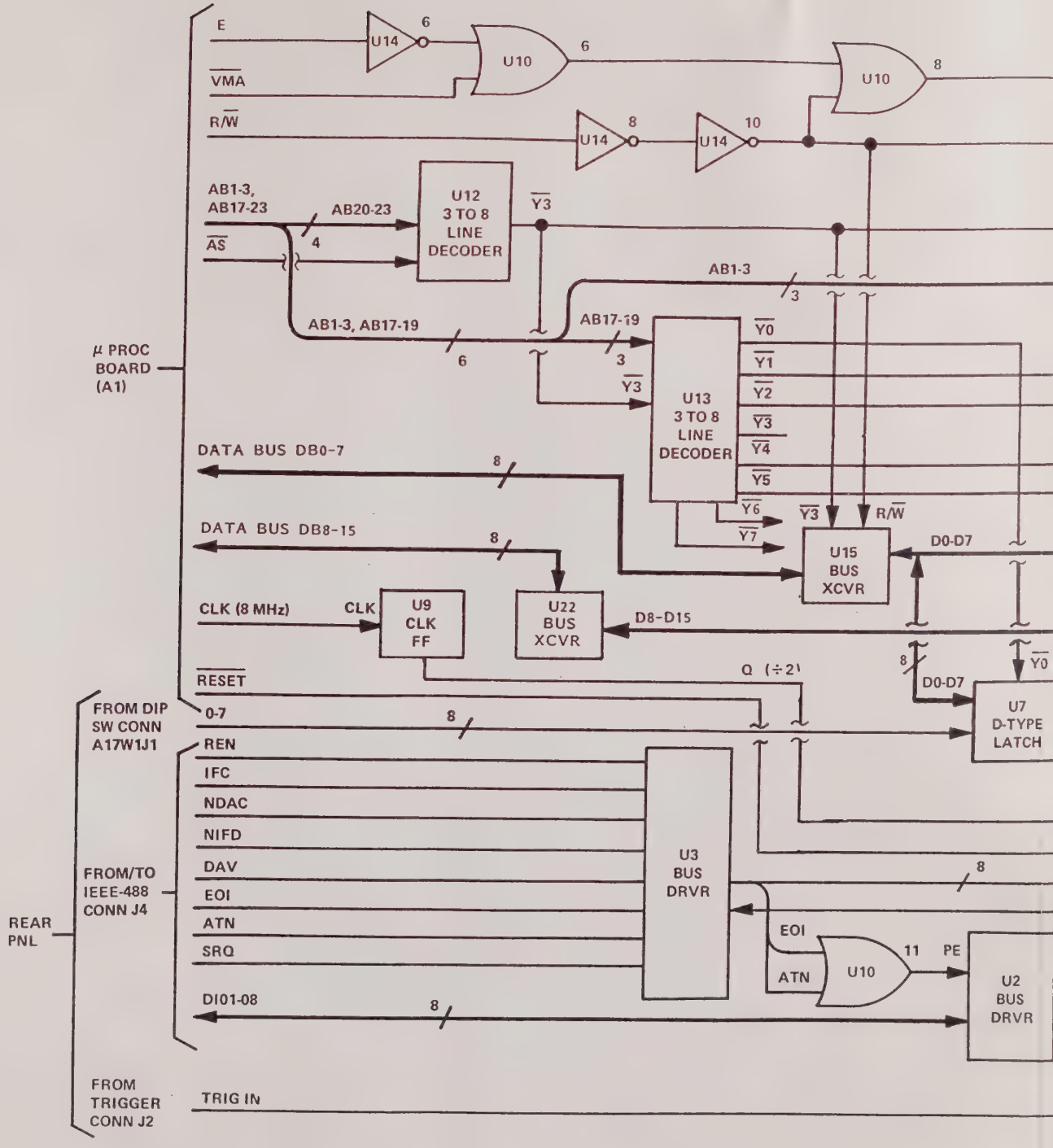


Figure 2-16. Display Board A15A3, Functional Signal Flow Diagram


E
VMA
R/W
U14
U10
AB1-3, AB17-23
AS
AB20-23
U12 3 TO 8 LINE DECODER
AB1-3
AB1-3, AB17-19
AB17-19
U13 3 TO 8 LINE DECODER
μ PROC BOARD (A1)
DATA BUS DB0-7
DATA BUS DB8-15
U15 BUS XCVR
D0-D7
CLK (8 MHz)
CLK
U9 CLK FF
U22 BUS XCVR
D8-D15
RESET
Q (÷2)
U7 D-TYPE LATCH
FROM DIP SW CONN A17W1J1
0-7
REN
IFC
NDAC
NFD
DAV
EOI
ATN
SRQ
FROM/TO IEEE-488 CONN J4
REAR PNL
U3 BUS DRVR
DI01-08
U2 BUS DRVR
PE
FROM TRIGGER CONN J2
TRIG IN

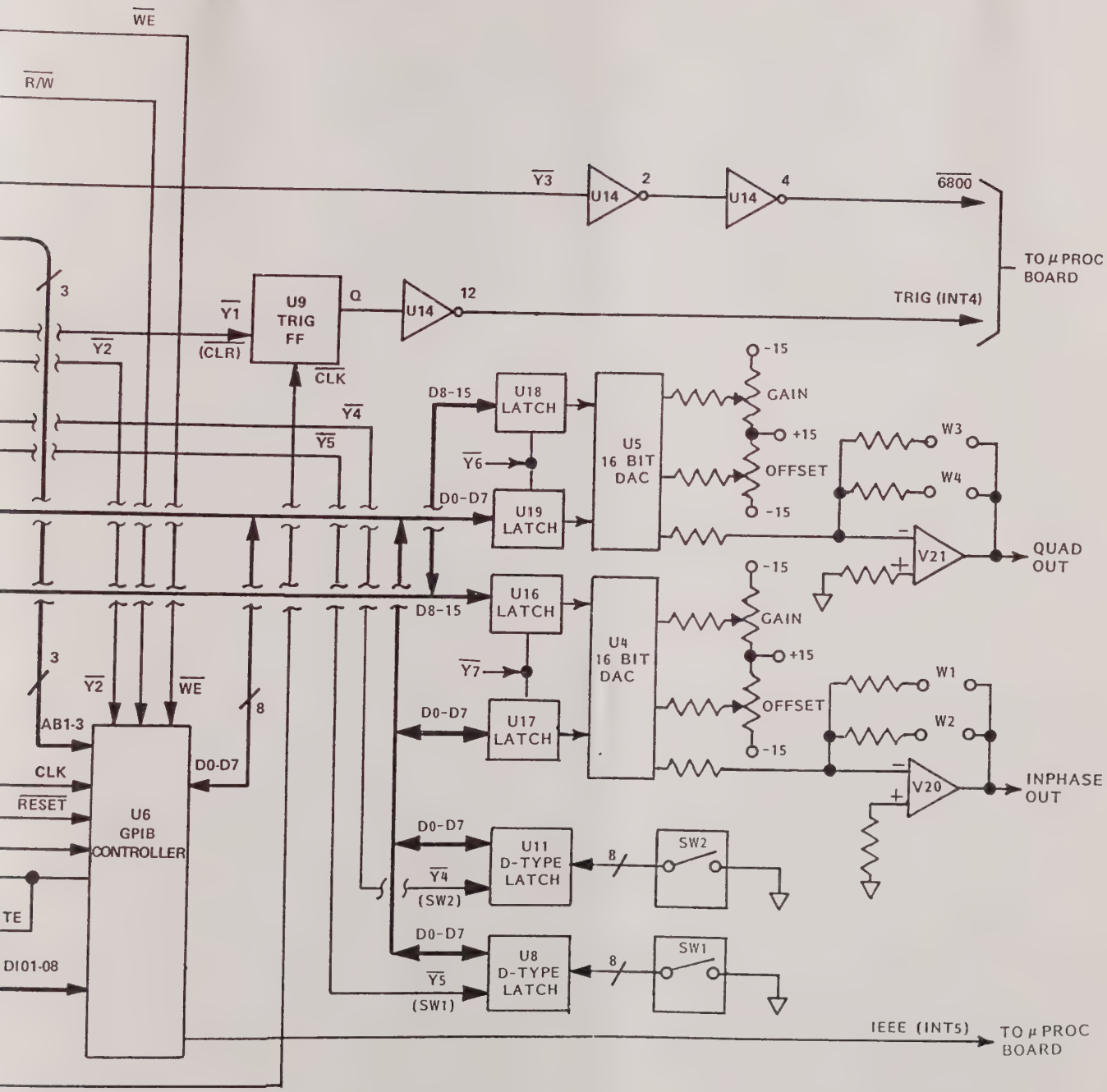


Figure 2-17. Input/Output (I/O) Board A3, Functional Signal Flow Diagram

a. WRITE CYCLE TIMING.

During a write cycle, data is transferred from the microprocessor data bus to I/O board A3. A write cycle is initiated when the microprocessor places the I/O board address on address bus lines AB1-3 and AB17-23, and asserts address strobe $\overline{AS}$ and R/$\overline{W}$. Address bus lines AB20-23 are decoded and an enable is supplied as the $\overline{6800}$ signal to the microprocessor. When the microprocessor receives the low $\overline{6800}$ input, the microprocessor asserts valid memory address $\overline{VMA}$ to I/O board A3. Microprocessor data on bus lines DB0-7 is transferred to the inputs of latch U7, GPIB controller U6, and dual D/A converter U4.

When GPIB adapter U6 is in the listen mode, U6 data is transferred to bus interface lines DI01-08. All IEEE-488 bus transaction timing is controlled by GPIB controller U6.

b. INTERRUPT AND READ CYCLE TIMING.

When data is to be transferred from the IEEE-488 bus to the microprocessor data bus, U6 provides an IEEE interrupt (INT5) to the microprocessor. The microprocessor decodes the interrupt level, sets function code bits FC0-2 high, places an interrupt level on address bus lines AB1-3, and asserts address strobe $\overline{AS}$. Since $\overline{AS}$ is asserted, $\overline{6800}$ is supplied to the microprocessor. The function code results in an internal interrupt request acknowledge ($\overline{IRQACK}$) which asserts valid peripheral address ($\overline{VPA}$) to cause autovectoring to the appropriate interrupt service routine.

When the microprocessor initiates a read cycle during an interrupt service routine the R/$\overline{W}$ input is set high, address is placed on the address bus lines, and $\overline{AS}$ is asserted. The address is decoded as before, except $\overline{WE}$ is now high which, together with high R/$\overline{W}$, causes U6 to transfer its internal register contents to data bus lines D0-7, and to the microprocessor data bus on lines DB0-7. Other read functions may access various input ports on I/O board A3.

c. RECORDER OUTPUT.

The recorder output is provided by two 16-bit multiplying digital-to-analog converters (DACs) U4 and U5. The converters receive data from the microprocessor that is equivalent to the front panel in-phase and quadrature readouts. Data is loaded into latches at the inputs of the two DACs from the common input data bus. DAC U4 provides the in-phase output. DAC U5 provides the quadrature readout.

d. TRIGGER INPUT.

The trigger input is used to generate interrupt level 4 to the microprocessor. This circuit is triggered by a TTL-compatible signal fed to the rear panel trigger input connector. The interrupt service routine for $\overline{TRIG}$, depending on the operating mode of the DAV, either updates the display or generates a service request over the GPIB interface. During the interrupt service, the microprocessor performs a normal read cycle.

e. GPIB INTERFACE.

The GPIB interface, controlled by GPIB controller U6, provides the interface between microprocessor board A1 and the IEEE-488 bus. For the talk function, the GPIB operates as an output port for the microprocessor; that is, it receives output data

from the microprocessor, stores it in internal registers and transmits the data onto the IEEE bus together with all handshaking and bus timing signals. For the listen function, U6 generates an interrupt which the microprocessor services by reading the status register and data register internal to U6.

2-10. AUTOCAL SECTION FUNCTIONAL DESCRIPTION. (See figure 2-18.)

The autocal section consists of Autocal board A8. Autocal board A8 generates a frequency and amplitude programmed sinewave output which is used to calibrate the measurement circuits, and a squarewave output used as one of the input signals to the phase comparator in the phase-locked loop circuit when in autocalibration mode. The basis of autocal board A8 is precision waveform generator U2 which is capable of producing sine and triangular output waveforms.

One of four frequency ranges is selected by the status of the four data bus lines, DB12 through 15, which are latched when autocal frequency enable, $\overline{\text{ACLFREQ}}$ appears from timing and control board A4. In addition, a 12-bit code is applied to a digital-to-analog converter from DB0 to DB11 when enable $\overline{\text{ACLFREQ}}$ is applied to its write input. The dc output voltage level produced selects the desired output frequency, with one frequency range.

The amplitude of the autocal output signal is controlled by a 12-bit input code, DB0-11, to a four quadrant multiplying digital-to-analog converter which is enabled by $\overline{\text{ACLCTL}}$.

A squarewave (ACLSQR) is applied as a reference signal to phase-locked loop board A5.

2-11. ISOLATION SECTION FUNCTIONAL DESCRIPTION. (See figure 2-19.)

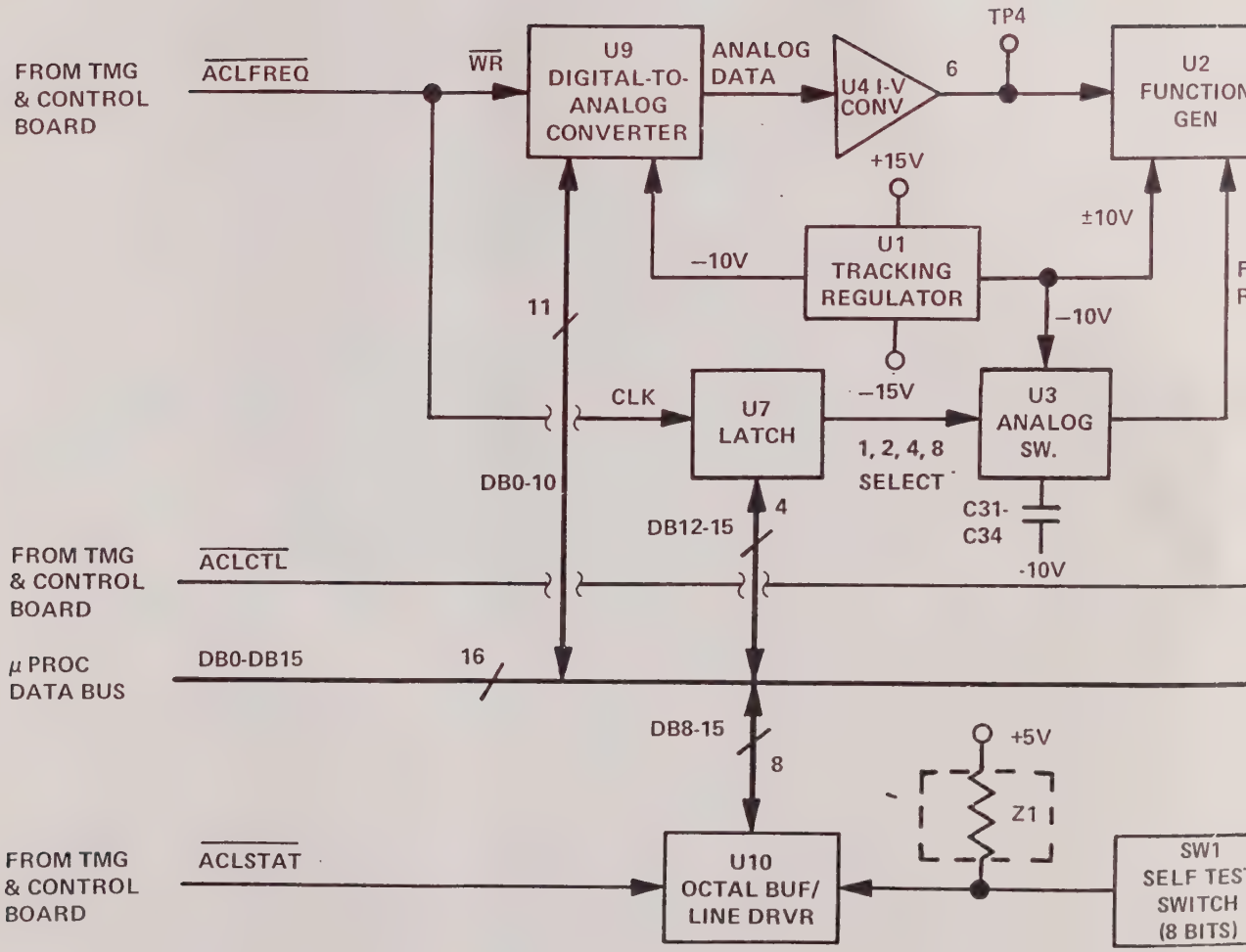
The Isolation section consists of Isolation assemblies A15A4/A15A5. Two functionally identical isolation assemblies, signal A15A4 and reference A15A5, maintain high-voltage, low-capacitance isolation between the signal and reference sections and provide for disconnecting the DAV input during autocalibration. During autocalibration, control signal MSR/$\overline{\text{AC}}$ is asserted and relays on the isolation board are de-energized. The relays open contacts disconnect the input signal from the front end boards and ground the open signal input lines.

2-12. POWER DISTRIBUTION. (See figure 2-20.)

The power distribution function contains a line entry module, main power transformer A17T1, main power supply A17PS1, signal isolated power supply A17PS3, reference isolated power supply A17PS2, and exhaust fan A17B1.

a. LINE POWER INPUT CIRCUIT.

Input power to the DAV is connected via a power cord, to the power input receptacle on the rear panel. Input power is 115/230V, 47-67 Hz, single phase. Input power is supplied to a line entry module containing an input fuse, LC line filter network and a means of switching between 115V and 230V operation. After filtering, the line voltage is supplied through the front panel POWER switch and back to the line entry


FROM TMG & CONTROL BOARD
ACLFREQ
WR
U9 DIGITAL-TO-ANALOG CONVERTER
ANALOG DATA
U4 I-V CONV
6
TP4
U2 FUNCTION GEN
+15V
±10V
U1 TRACKING REGULATOR
−10V
−10V
11
CLK
U7 LATCH
−15V
U3 ANALOG SW.
1, 2, 4, 8 SELECT
DB0-10
DB12-15
4
C31-C34
-10V
FROM TMG & CONTROL BOARD
ACLCTL
μ PROC DATA BUS
DB0-DB15
16
DB8-15
8
+5V
Z1
FROM TMG & CONTROL BOARD
ACLSTAT
U10 OCTAL BUF/ LINE DRVR
SW1 SELF TEST SWITCH (8 BITS)

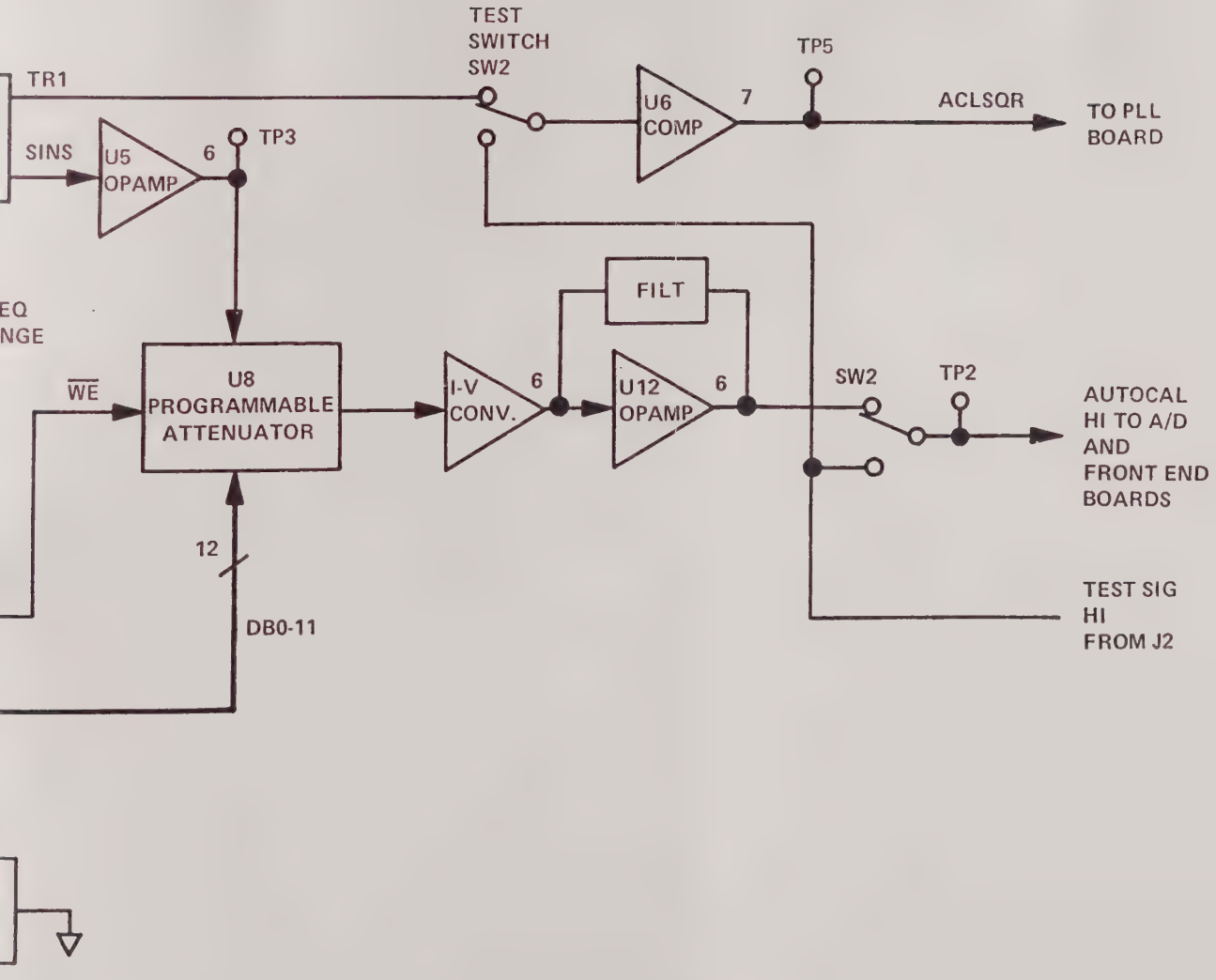


Figure 2-18. Autocalibration Board A8, Functional Signal Flow Diagram

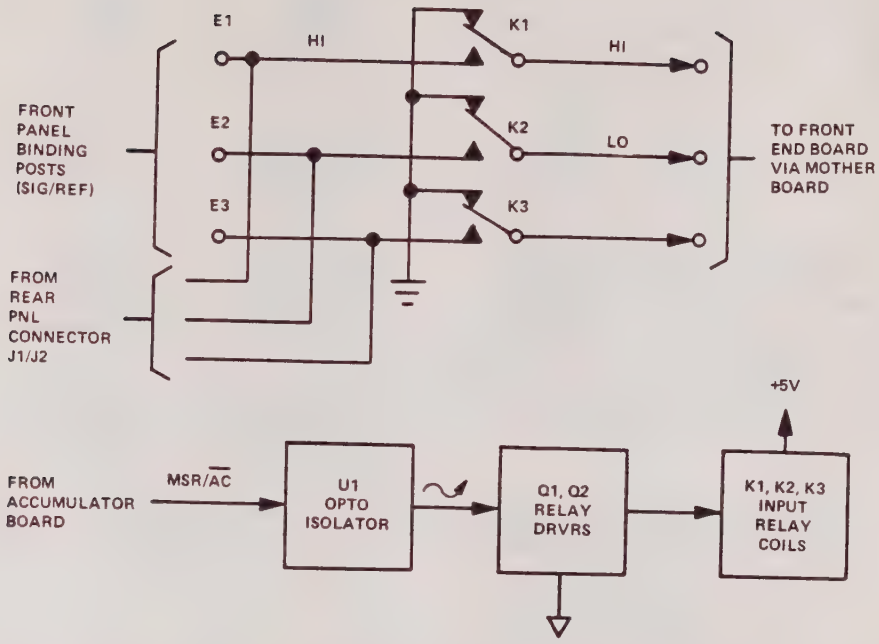


Figure 2-19. Isolation Board A15A4/A15A5, Functional Signal Flow Diagram

module to the line voltage selection circuit card and then to main power transformer A17T1, to signal and reference isolation power supplies A17PS3 and PS2, and to fan A17B1. The line voltage selection circuit card adapts the DAV power input circuits to 115 or 230 volts ac. (Refer to Model 2250 Instruction Manual.) Each power transformer has dual primaries to facilitate use at either 115V or 230V.

b. MAIN POWER SUPPLY A17PS1. (See figure 2-21 for details of functional signal flow within Main Power Supply A17PS1.)

The input power to transformer A17T1 is stepped down and supplied to main power supply A17PS1 which consists of ±5 Vdc and ±15 Vdc regulated power supplies. The ±5 Vdc and ±15 Vdc outputs are used to power all functions of the DAV except the signal and reference sections.

c. ISOLATED POWER SUPPLIES A17PS2 AND PS3. (See figure 2-22 for details of functional signal flow within Isolated Power Supplies A17PS2/A17PS3.)

Signal and reference isolated power supplies A17PS2/PS3 are identical, with each supply providing +5 Vdc and ±15 Vdc regulated outputs to power the respective signal and reference section consisting of the isolation board, front end board, filter board, and A/D converter board.

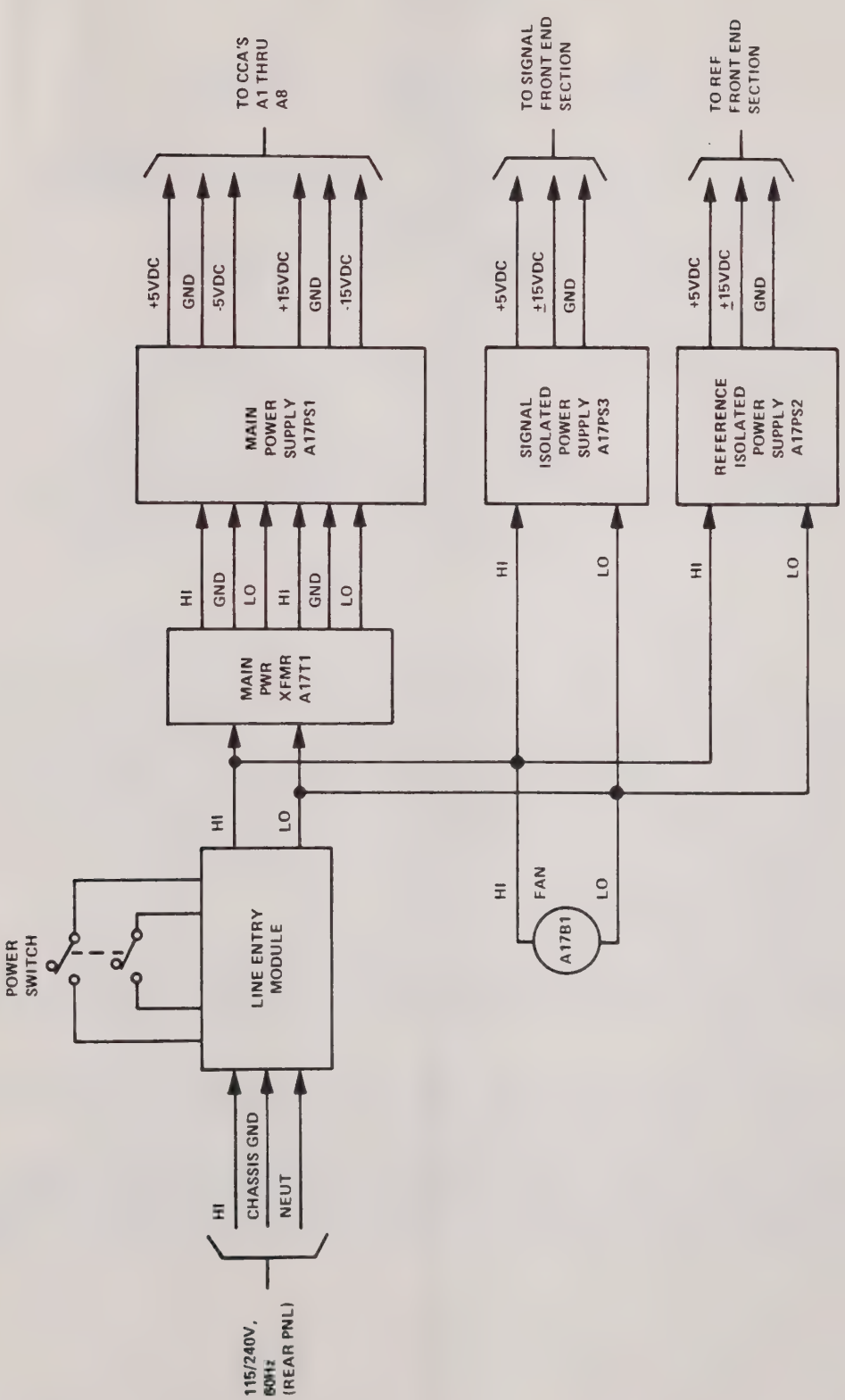
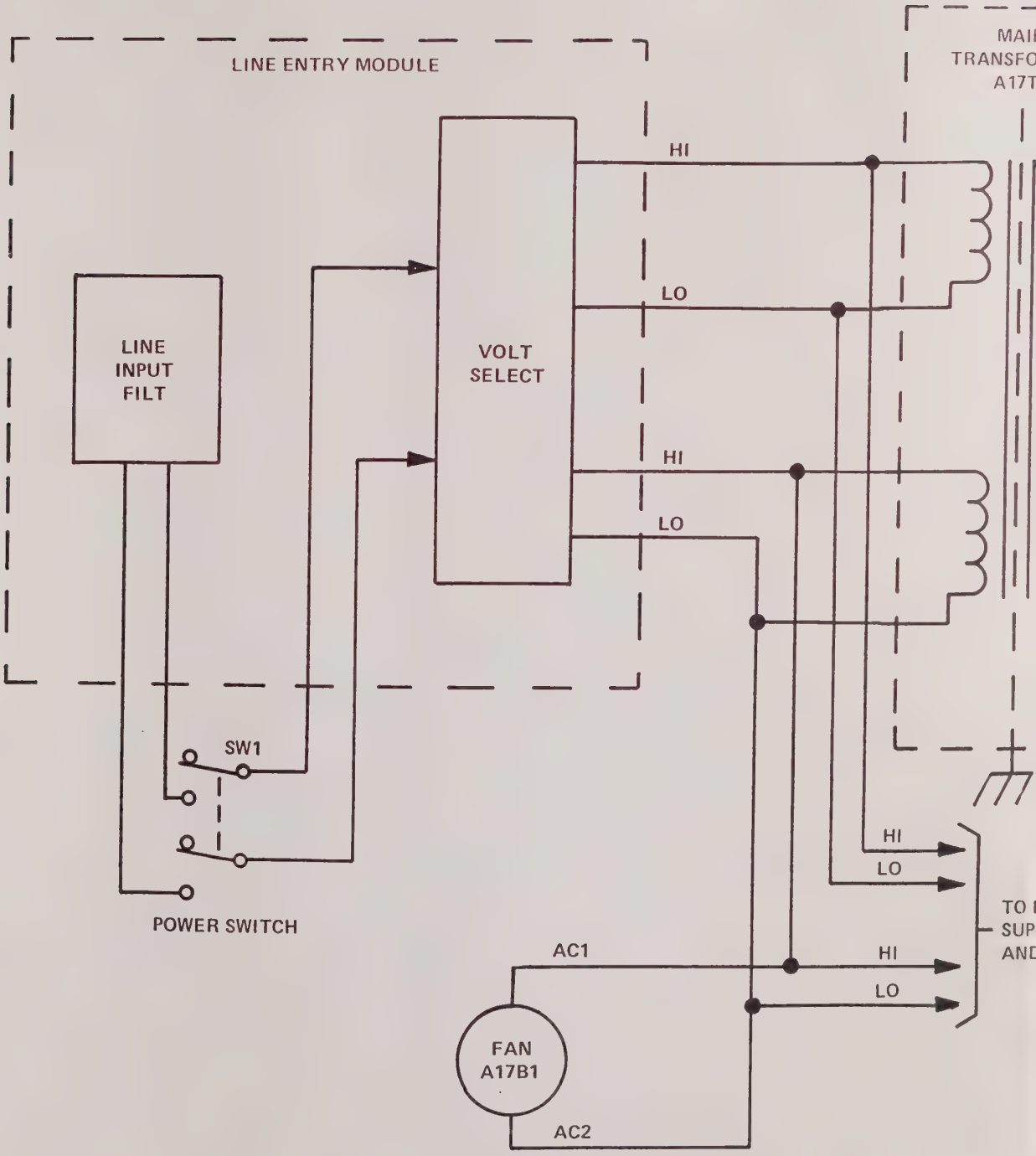


Figure 2-20. Power Distribution Function, Simplified Functional Diagram


LINE ENTRY MODULE
MAI
TRANSFO
A17T
HI
LO
HI
LO
LINE
INPUT
FILT
VOLT
SELECT
SW1
POWER SWITCH
HI
LO
TO
SUP
AND
AC1
HI
LO
FAN
A17B1
AC2

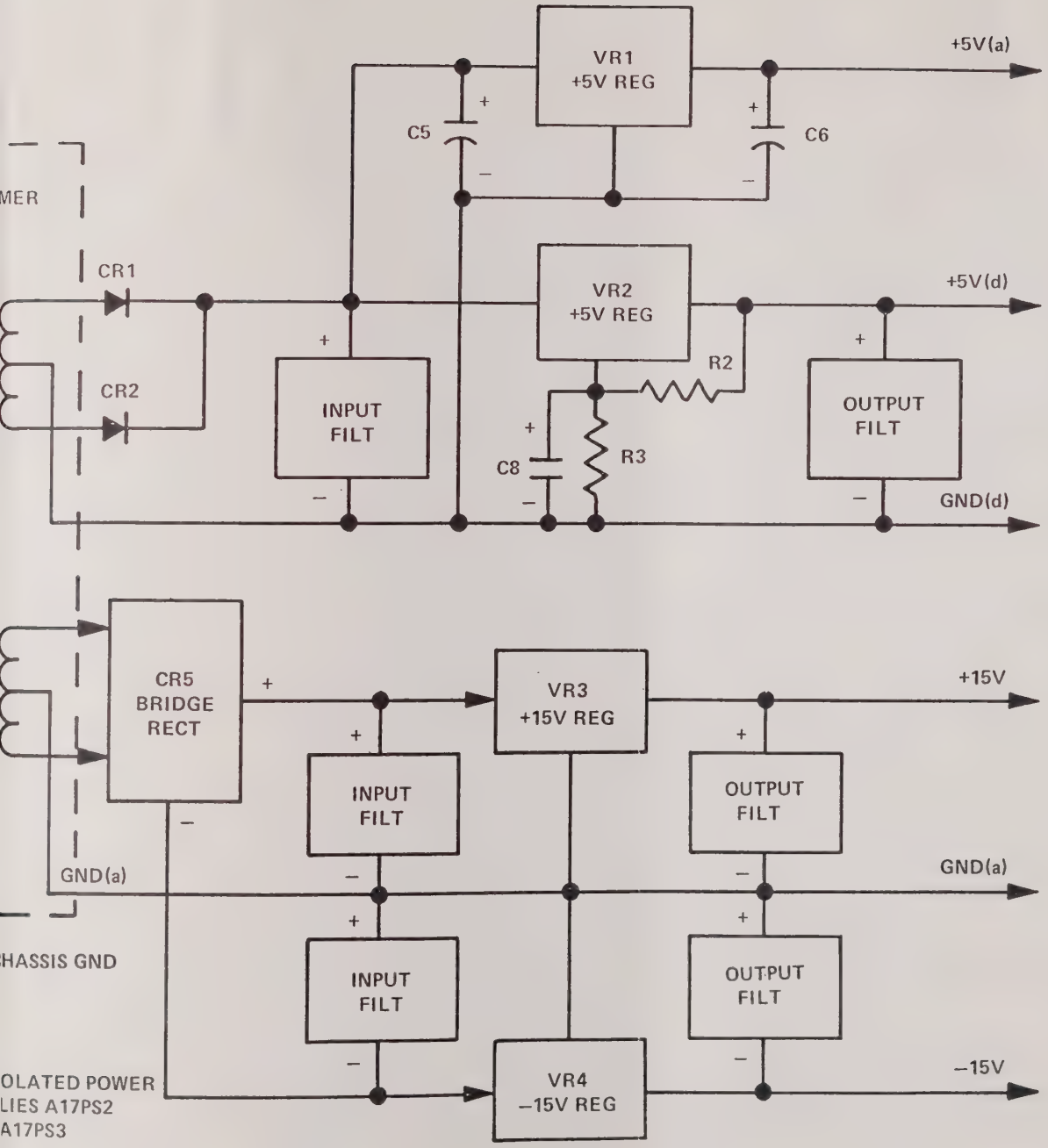


Figure 2-21. Main Power Supply A17PS1, Functional Signal Flow Diagram

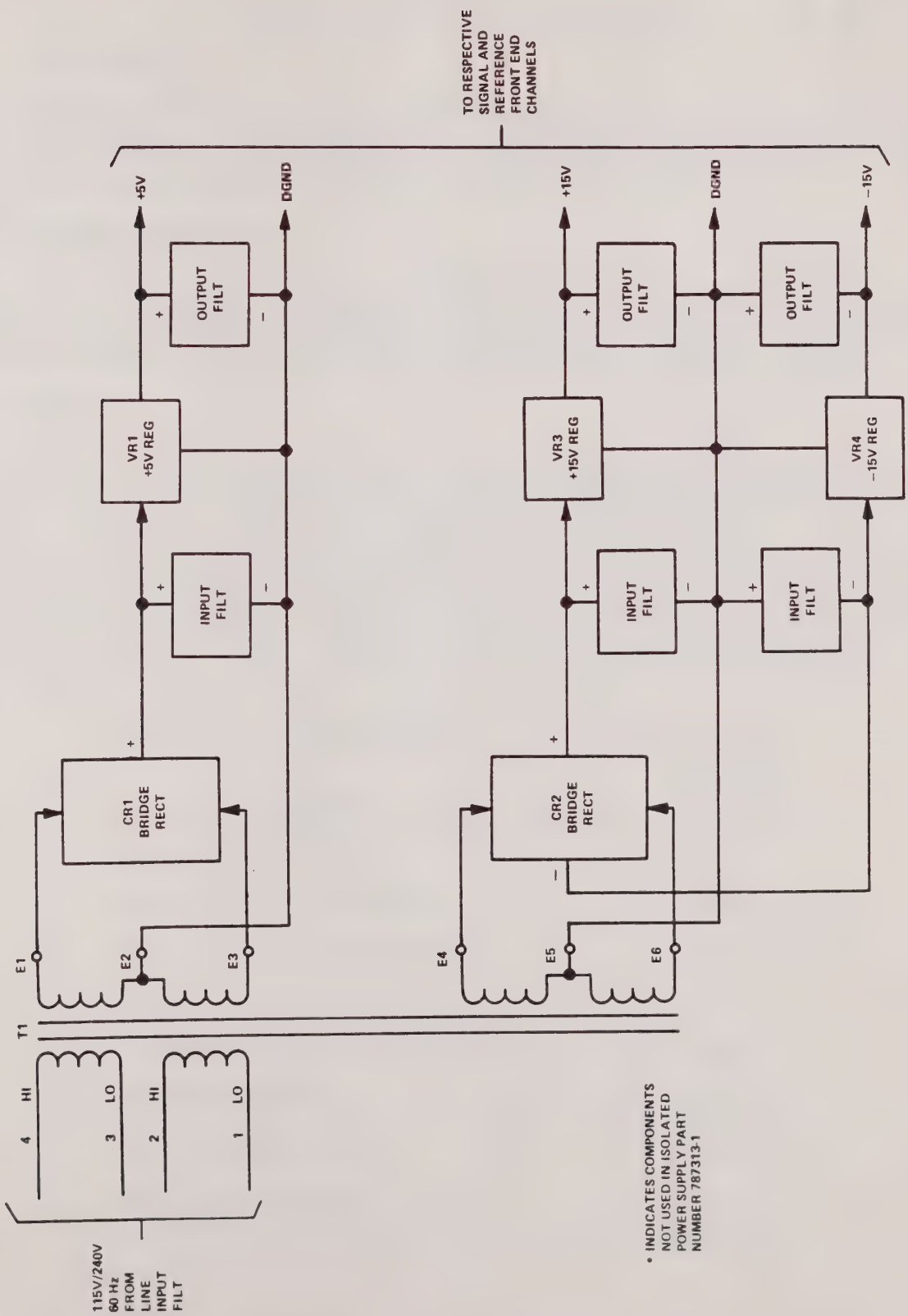


Figure 2-22. Isolated Power Supplies A17PS2/A17PS3, Functional Signal Flow Diagram

SECTION 3

CHECKOUT, ALIGNMENT AND CALIBRATION

3-1. INTRODUCTION.

This section contains checkout, alignment and calibration instructions for the DAV. The section begins with a schedule for the periodic performance of the various checkouts, alignments, and calibrations covered in this section. Table 1-4 lists the test equipment required to perform the procedures in this section.

3-2. PERFORMANCE SCHEDULE.

Table 3-1 lists the alignment procedures and subsequent performance tests recommended for performance on an annual basis. After repair or replacement of an assembly, all alignments pertaining to the repaired or replaced assembly must be performed followed by the complete checkout procedure provided in paragraph 3-3.

3-3. CHECKOUT.

Checkout for the DAV consists of the group of performance test procedures provided in the following subparagraphs. Each procedure is presented in a step-by-step format and references a test setup figure. The test setup figure illustrates the complement of test equipment necessary to perform the test and shows all the required interconnections between the test equipment and the DAV. (Procedures a through d do not require setup figures.) Refer to table 1-4 for specific test equipment requirements. In the procedures, data tables are referenced that provide specifications and tolerances for readings taken during checkout. If the result of any test is not as described in the procedure, refer to the troubleshooting procedures provided in section 4 of this manual. Pretest conditions are stated for each procedure.

Table 3-1. Annual Performance Tests and Calibration

PROCEDURE	REFERENCE PARAGRAPH
Autocal A8 Alignment	3-4c
Front End A14/A11 Alignment	3-4d
Phase-Locked Loop A5 Alignment	3-4e
A/D Converter A9/A12 Alignment	3-4f
I/O A3 Recorder Output Adjustment	3-4g
High Voltage Test	3-3e
Wideband Accuracy Test	3-3f
Phase Accuracy Check at 400 Hz	3-3h

a. CONTINUITY CHECK.

1. Pretest conditions:

(a) DAV turned off.
(b) Power cord removed from ac source.
(c) DAV top cover on.
(d) Test equipment on and warmed up.

2. Remove front and rear panel shorting links.

3. Using DMM, check continuity between terminals listed below. All resistances should be less than 0.1 ohm.

Power cord ground prong to Rear panel chassis ground
Power cord ground prong to Front panel chassis ground
Power cord ground prong to Top cover screw head
SIG HI input to Rear panel J1-A
SIG LO input to Rear panel J1-B
SIG GUARD input to Rear panel J1-C
Chassis to Rear panel J1-D
Chassis to Rear panel J2-D
REF HI input to Rear panel J2-A
REF LO input to Rear panel J2-B
REF GUARD input to Rear panel J2-C

b. GROUND ISOLATION CHECK.

1. Pretest conditions:

(a) DAV turned off.
(b) Power cord removed from ac source.
(c) DAV top cover on.
(d) Test equipment on and warmed up.

2. Using megohmmeter at 500 V dc, measure resistance between terminals listed below. All resistances should be greater than 100 megohms.

Rear panel CHS ground to Rear panel CKT ground
SIG LO input to SIG GUARD input
REF LO input to REF GUARD input

3. Connect the line cord to the ac voltage source and turn on DAV. Using a megohmmeter set at 500 V dc, measure resistance between terminals listed below. All resistances should be greater than 100 megohms.

WARNING

Be sure ac power source has a good quality safety (earth) ground. Do not touch chassis during Hypot tests.

Rear panel CHS ground to Rear panel CKT ground
SIG LO input to SIG GUARD input
REF LO input to REF GUARD input

4. Connect front and rear panel shorting links and install a jumper between SIG HI and SIG LO. Install another jumper between REF HI and REF LO. Use Hypot at 700 V rms for 2 seconds between terminals listed below. If any leakage or breakdown occurs (Hypot indicators light), test has failed.

SIG LO to Chassis ground
REF LO to Chassis ground

5. Turn off DAV and disconnect from ac power source. Remove rear panel shorting link and connect a jumper between HI and neutral prongs of power cord. Use Hypot at 1200 V rms for 2 seconds with DAV POWER switch on between terminals listed below. A leakage indication should occur at approximately 400 V, which is acceptable. Breakdown indicates failure.

CAUTION

If this test needs to be repeated, it must be performed at 900 V rms.

Power cord HI prong to Power cord ground prong

6. Install front and rear panel shorting links

c. SIGNAL AND REFERENCE ISOLATION CHECK.

1. Pretest conditions:

(a) DAV turned on.
(b) DAV top cover on.
(c) Test equipment on and warmed up.

2. Install a jumper between SIG HI and SIG LO. Install another jumper between REF HI and REF LO. Use Hypot at 750 V rms for 2 seconds between terminals listed below. If any leakage or breakdown occurs (Hypot indicators light), test has failed.

CAUTION

If this test needs to be repeated, it must be performed at 500 V rms.

WARNING

Be sure ac power source has a good quality safety (earth) ground. Do not touch chassis during Hypot tests.

SIG LO to Chassis gnd
REF LO to Chassis gnd
REF LO to SIG LO

3. Disconnect jumpers.

d. KEYBOARD/LAMP TEST.

The DAV is capable of a keyboard and display self test. To perform the test, proceed as follows:

1. Keyboard Test:

(a) Turn off DAV power switch.
(b) Remove DAV top cover (2, figure 5-1) by removing four screws (1).
(c) On Autocal A8, set DIP switch A8SW1 to binary 5 as follows:

A8SW1-5(D3) OFF	A8SW1-7(D1) OFF
A8SW1-6(D2) ON	A8SW1-8(D0) ON

(d) Turn on DAV power switch and allow DAV to initialize.
(e) Press in turn each of the 44 keyboard switches and observe that the corresponding LED lights. Observe also that as each new switch is pressed, the previously lit LED goes out. If any LED fails to light or fails to go out the test has failed.
(f) Turn off DAV and restore A8SW3 switches -5, -6, -7, and -8 to the OFF position.

2. Display test:

(a) Turn off DAV power switch.
(b) Remove DAV top cover (2, figure 5-1) by removing four screws (1).
(c) On Autocal A8, set DIP switch A8SW1 to binary 6 as follows:

A8SW1-5(D3) OFF	A8SW1-7(D1) ON
A8SW1-6(D2) ON	A8SW1-8(D0) OFF

(d) Turn on DAV power switch and observe that the DAV initializes and begins a sequence which exercises all displays and annunciators in the display window of the front panel in the sequence specified below. If any of the displays fails to follow the sequence, the test has failed.

Main Display (6 digits):	Each digit starting from the left cycles from 0 through 9 followed by the decimal point.
Frequency Display (3 digits):	Each digit starting from the left cycles from 0 through 9 followed by the decimal point.
Harmonic Display (2 digits):	Each digit starting from the left cycles from 0 through 9.
Annunciators:	All Annunciators light and go out in the following sequence:

REM
TALK
Listen
SRQ
SUM
AVG
DEG
dB
Volts
10^{-3}
MV
%
kHz
Hz
HMNC
VAR

e. HIGH VOLTAGE TEST.

WARNING

Use extreme caution during this test. Fatal shock hazard is present in circuits under test.

1. Pretest conditions:

   (a) Test set up as shown in figure 3-1.
   (b) DAV top cover on.
   (c) DAV set for TOTAL (SUM) operation (see Instruction Manual).
   (d) DAV and test equipment on and warmed up.
   (e) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
   (f) Press CLEAR VAR key to clear any preset variables from memory.

2. Set DMM to 500 V range. On DAV, press FUND key followed by 500 V range key.

NOTE

Pressing range key on DAV sets SIG channel only. REF channel range is selected automatically.

3. Adjust voltage standard output for 400 Hz, 500 V rms.
4. Observe that DAV initializes and locks.
5. After DAV initializes and locks, press CAL key.
6. Observe that DAV calibration sequence goes to completion.
7. Check DAV high voltage accuracy as follows:
   (a) On DAV, observe LED on READ REF key. If LED is lit, press READ REF key and observe that LED goes out (DAV set for SIG channel measurement).
   (b) On DAV, press FUND key.
   (c) Compare readings on DMM and DAV. Check to see that difference in FUND readings is within tolerance listed in table 3-2.
   (d) On DAV, press TOTAL key.
   (e) Compare readings on DMM and DAV. Check to see that difference in DAV TOTAL readings is within tolerance listed in table 3-2.

Table 3-2. High Voltage Test Specifications

DAV VOLTAGE RANGE	INPUT VOLTAGE	FUND/TOTAL SIG AND REF TOLERANCE SPECIFICATION
500 V	500 V rms	±1.25 V rms
500 V	200 V rms	±1.10 V rms
200 V	200 V rms	±0.20 V rms

   (f) On DAV, press READ REF key and observe that LED on READ REF key lights. (DAV set for REF channel measurement.)
   (g) Repeat step 7 (b) through 7 (e).
   (h) On DAV, press READ REF key and observe that LED on READ REF key goes out (DAV set for SIG channel measurement).
8. On voltage standard, adjust output for 200 V rms. (Readjust DMM.)
9. Observe that DAV initializes and locks.
10. Repeat step 7 (a) through 7 (h) using specifications in table 3-2 for 200 V input on DAV 500 V range.

NOTE

While performing step 7 (g), ensure that REF channel remains on 500 V range by observing that LED on 500 V range key remains lit.

WARNING: EXTREME CAUTION MUST BE USED WITH THIS SETUP - FATAL SHOCK HAZARD!!

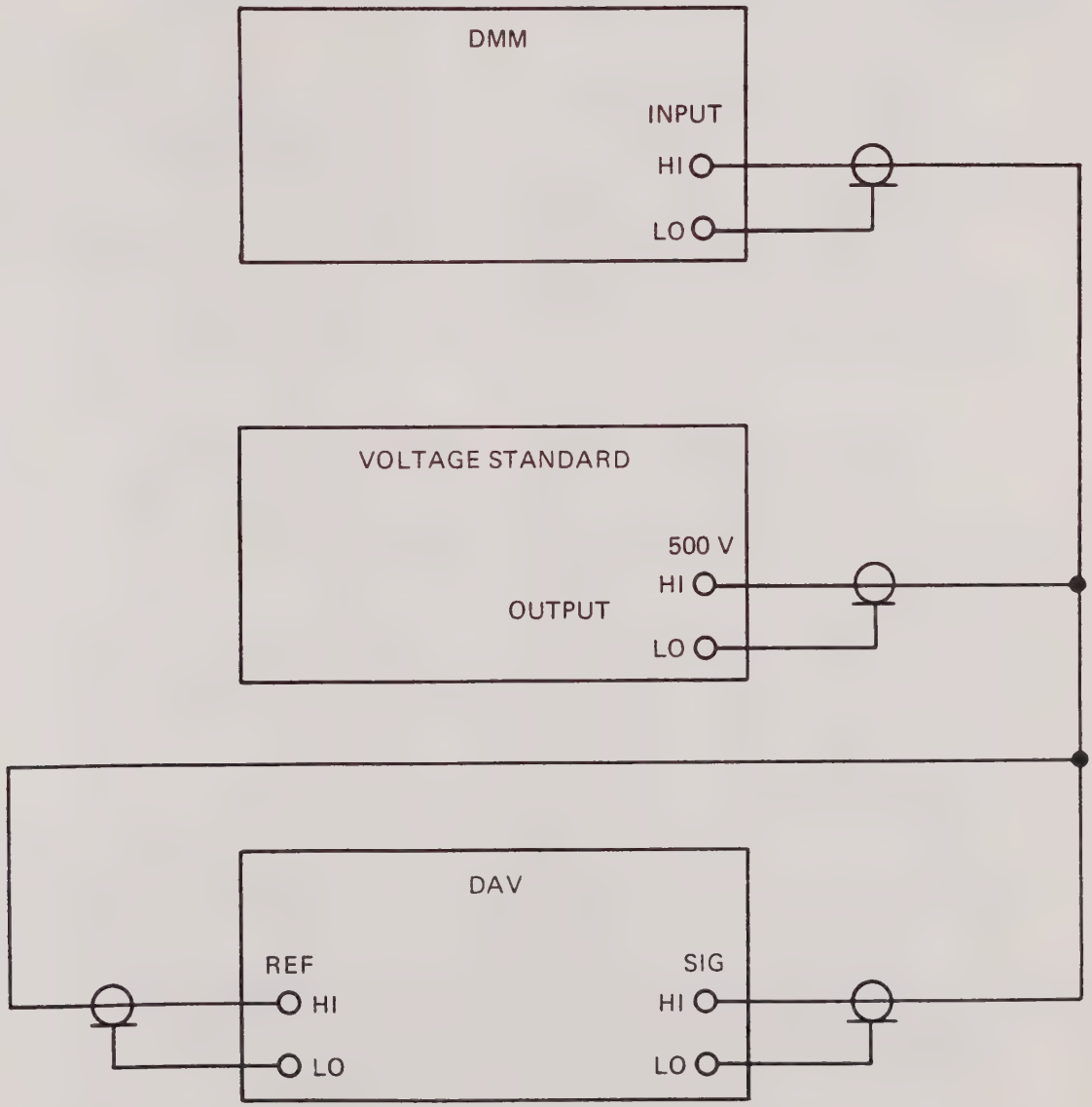


Figure 3-1. High Voltage Test Setup Diagram

11. Readjust voltage standard output to 180 V, press DAV 200 V range key.
12. Observe that DAV is locked.
13. Repeat step 7 (a) through (h) using specifications in table 3-2 for 180 V input on DAV 200 V range.

f. WIDEBAND ACCURACY TEST

1. Pretest conditions:

   (a) DAV top cover on.
   (b) DAV set for TOTAL (SUM) operation (see Instruction Manual).
   (c) DAV and test equipment on and warmed up. Phase generator output set to off.
   (d) Test setup as shown in figure 3-2 (setup A).
   (e) Ensure that the DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
   (f) Press CLEAR VAR to clear any preset variables from memory.
   (g) Press FUND key.

NOTE

While performing procedure reconfigure figure 3-2 setup as specified. Setup selected depends on test voltage and frequency. Refer to table 3-3 for proper setup and tolerance specifications.

2. On DAV, press 200 V range key and FUND key.
3. Set DMM to 100 V range.
4. Set up phase generator CH 2 output for 10 Hz, 9.0 V rms 0 ohms, sine wave.
5. Set up power amplifier for fixed gain of 10, ac coupling and 0 V offset.
6. Set phase generator output to on.
7. After DAV initializes and locks, press CAL key.
8. Observe calibration sequence goes to completion on DAV display panel.
9. With phase generator maintained at 10 Hz, (or frequency specified in table 3-3, for subsequent steps) test DAV wideband accuracy as follows:

   (a) On DAV observe LED on READ REF key. If lit, press READ REF key and observe that LED goes out (DAV set for SIG channel measurement).
   (b) Adjust phase generator voltage for first listing in table 3-3.
   (c) Set DMM to proper range as specified in table 3-3.
   (d) On DAV, press range key specified in table 3-3.

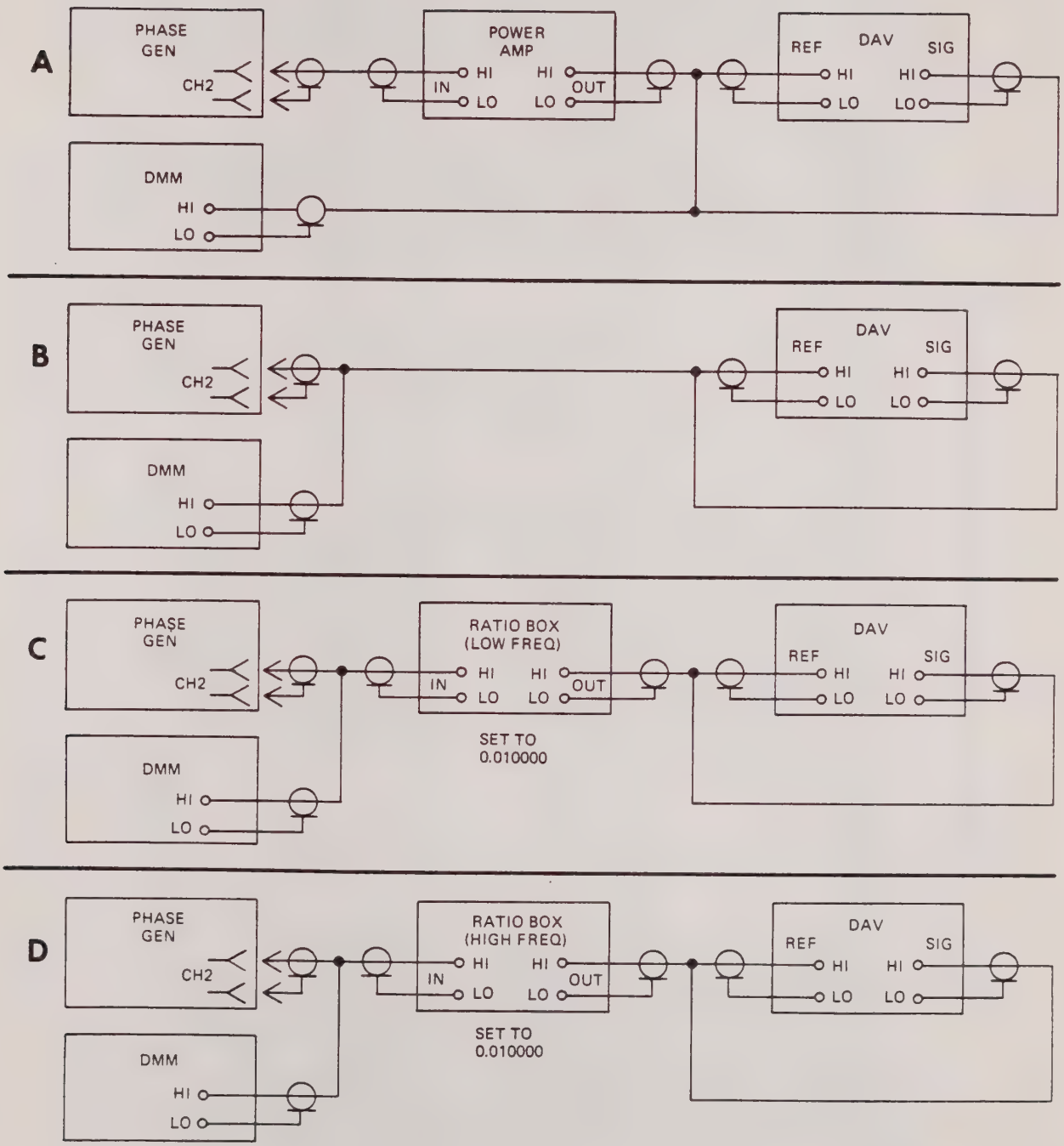


Figure 3-2. Wideband Accuracy Test Setup Diagram

Table 3-3. Wideband Accuracy Settings and Specifications

PHASE GENERATOR		TEST VOLTAGE	FIGURE 3-2 SETUP	DAV RANGE	DMM RANGE	DIVIDE DMM BY 100	DAV VOLTAGE TOLERANCE FUND AND TOTAL	DAV PHASE SPEC. DEGREES
FREQ	VOLT							
10 Hz	9.0 V	90 V	A	200 V	100 V	No	.290 V	0 +/- 0.10
10 Hz	4.5 V	45 V	A	200 V	100 V	No	.245 V	0 +/- 0.10
10 Hz	18.0 V	18.0 V	B	20 V	10 V	No	.0290 V	0 +/- 0.10
10 Hz	4.5 V	4.5 V	B	20 V	10 V	No	.02225 V	0 +/- 0.10
10 Hz	1.8 V	1.8 V	B	2 V	1 V	No	.00290 V	0 +/- 0.10
10 Hz	450 mV	4.5 mV	C	20 mV	1 V	Yes	.02225 mV	0 +/- 0.10
10 Hz	225 mV	2.25 mV	C	20 mV	300 mV	Yes	.021125 mV	0 +/- 0.10
50 Hz	9.0 V	90 V	A	200 V	100 V	No	.195 V	0 +/- 0.05
50 Hz	4.5 V	45 V	A	200 V	100 V	No	.145 V	0 +/- 0.05
50 Hz	18.0 V	18.0 V	B	20 V	10 V	No	.0190 V	0 +/- 0.05
50 Hz	4.5 V	4.5 V	B	20 V	10 V	No	.01225 V	0 +/- 0.05
50 Hz	1.8 V	1.8 V	B	2 V	1 V	No	.00190 V	0 +/- 0.05
50 Hz	450 mV	4.5 mV	C	20 mV	1 V	Yes	.01225 mV	0 +/- 0.05
50 Hz	225 mV	2.25 mV	C	20 mV	300 mV	Yes	.011125 mV	0 +/- 0.05
400 Hz	9.0 V	90 V	A	200 V	100 V	No	.195 V	0 +/- 0.05
400 Hz	4.5 V	45 V	A	200 V	100 V	No	.145 V	0 +/- 0.05
400 Hz	18.0 V	18.0 V	B	20 V	10 V	No	.0190 V	0 +/- 0.05
400 Hz	4.5 V	4.5 V	B	20 V	10 V	No	.01225 V	0 +/- 0.05
400 Hz	1.8 V	1.8 V	B	2 V	1 V	No	.00190 V	0 +/- 0.05
400 Hz	9.0 V	90 mV	C	200 mV	10 V	Yes	.145 mV	0 +/- 0.05
400 Hz	450 mV	4.5 mV	C	20 mV	1 V	Yes	.01225 mV	0 +/- 0.05
400 Hz	225 mV	2.25 mV	C	20 mV	300 mV	Yes	.011125 mV	0 +/- 0.05

Table 3-3. Wideband Accuracy Settings and Specifications (Continued)

PHASE GENERATOR FREQ	PHASE GENERATOR VOLT	TEST VOLTAGE	FIGURE 3-2 SETUP	DAV RANGE	DMM RANGE	DIVIDE DMM BY 100	DAV VOLTAGE TOLERANCE FUND AND TOTAL	DAV PHASE SPEC. DEGREES
1.5 kHz	9.0 V	90 V	A	200 V	100 V	No	.195 V	0 +/- 0.05
1.5 kHz	4.5 V	45 V	A	200 V	100 V	No	.145 V	0 +/- 0.05
1.5 kHz	18.0 V	18.0 V	B	20 V	10 V	No	.0190 V	0 +/- 0.05
1.5 kHz	4.5 V	4.5 V	B	20 V	10 V	No	.01225 V	0 +/- 0.05
1.5 kHz	1.8 V	1.8 V	B	2 V	1 V	No	.00190 V	0 +/- 0.05
1.5 kHz	9.0 V	90 mV	C	200 mV	10 V	Yes	.145 mV	0 +/- 0.05
1.5 kHz	450 mV	4.5 mV	C	20 mV	1 V	Yes	.01225 mV	0 +/- 0.05
1.5 kHz	225 mV	2.25 mV	C	20 mV	300 mV	Yes	.011125 mV	0 +/- 0.05
5.0 kHz	9.0 V	90 V	A	200 V	100 V	No	.228 V	0 +/- 0.05
5.0 kHz	4.5 V	45 V	A	200 V	100 V	No	.174 V	0 +/- 0.05
5.0 kHz	18.0 V	18.0 V	B	20 V	10 V	No	.0229 V	0 +/- 0.05
5.0 kHz	4.5 V	4.5 V	B	20 V	10 V	No	.0147 V	0 +/- 0.05
5.0 kHz	1.8 V	1.8 V	B	2 V	1 V	No	.00229 V	0 +/- 0.05
5.0 kHz	9.0 V	90 mV	C	200 mV	10 V	Yes	.174 mV	0 +/- 0.05
5.0 kHz	450 mV	4.5 mV	C	20 mV	1 V	Yes	.0147 mV	0 +/- 0.05
5.0 kHz	225 mV	2.25 mV	C	20 mV	300 mV	Yes	.01335 mV	0 +/- 0.05
20 kHz	9.0 V	90 V	A	200 V	100 V	No	.309 V	0 +/- 0.20
20 kHz	4.5 V	45 V	A	200 V	100 V	No	.2145 V	0 +/- 0.20
20 kHz	18.0 V	18.0 V	B	20 V	10 V	No	.0336 V	0 +/- 0.20
20 kHz	4.5 V	4.5 V	B	20 V	10 V	No	.0174 V	0 +/- 0.20
20 kHz	1.8 V	1.8 V	B	2 V	1 V	No	.00336 V	0 +/- 0.20
20 kHz	9.0 V	90 mV	D	200 mV	10 V	Yes	.228 mV	0 +/- 0.20
20 kHz	450 mV	4.5 mV	D	20 mV	1 V	Yes	.0174 mV	0 +/- 0.20
20 kHz	225 mV	2.25 mV	D	20 mV	300 mV	Yes	.01470 mV	0 +/- 0.20

Table 3-3. Wideband Accuracy Settings and Specifications (Continued)

PHASE GENERATOR FREQ	PHASE GENERATOR VOLT	TEST VOLTAGE	FIGURE 3-2 SETUP	DAV RANGE	DMM RANGE	DIVIDE DMM BY 100	DAV VOLTAGE TOLERANCE FUND AND TOTAL	DAV PHASE SPEC. DEGREES
32 kHz	9.0 V	90 V	A	200 V	100 V	No	.546 V	0 +/- 0.32
32 kHz	4.5 V	45 V	A	200 V	100 V	No	.393 V	0 +/- 0.32
32 kHz	18.0 V	18.0 V	B	20 V	10 V	No	.0582 V	0 +/- 0.32
32 kHz	4.5 V	4.5 V	B	20 V	10 V	No	.03255 V	0 +/- 0.32
32 kHz	1.8 V	1.8 V	B	2 V	1 V	No	.00582 V	0 +/- 0.32
32 kHz	9.0 V	90 mV	D	200 mV	10 V	Yes	.411 mV	0 +/- 0.32
32 kHz	450 mV	4.5 mV	D	20 mV	1 V	Yes	.03255 mV	0 +/- 0.32
32 kHz	225 mV	2.25 mV	D	20 mV	300 mV	Yes	.028275 mV	0 +/- 0.32
54 kHz	9.0 V	90 V	A	200 V	100 V	No	.960 V	0 +/- 0.54
54 kHz	4.5 V	45 V	A	200 V	100 V	No	.600 V	0 +/- 0.54
54 kHz	18.0 V	18.0 V	B	20 V	10 V	No	.1140 V	0 +/- 0.54
54 kHz	4.5 V	4.5 V	B	20 V	10 V	No	.0465 V	0 +/- 0.54
54 kHz	1.8 V	1.8 V	B	2 V	1 V	No	.01140 V	0 +/- 0.54
54 kHz	9.0 V	90 mV	D	200 mV	10 V	Yes	.690 mV	0 +/- 0.54
54 kHz	450 mV	4.5 mV	D	20 mV	1 V	Yes	.0465 mV	0 +/- 0.54
54 kHz	225 mV	2.25 mV	D	20 mV	300 mV	Yes	.03525 mV	0 +/- 0.54
100 kHz	9.0 V	90 V	A	200 V	100 V	No	1.320 V	0 +/- 1.00
100 kHz	4.5 V	45 V	A	200 V	100 V	No	.780 V	0 +/- 1.00
100 kHz	18.0 V	18.0 V	B	20 V	10 V	No	.1590 V	0 +/- 1.00
100 kHz	4.5 V	4.5 V	B	20 V	10 V	No	.05775 V	0 +/- 1.00
100 kHz	1.8 V	1.8 V	B	2 V	1 V	No	.01590 V	0 +/- 1.00
100 kHz	9.0 V	90 mV	D	200 mV	10 V	Yes	.915 mV	0 +/- 1.00
100 kHz	450 mV	4.5 mV	D	20 mV	1 V	Yes	.05775 mV	0 +/- 1.00
100 kHz	225 mV	2.25 mV	D	20 mV	300 mV	Yes	.040875 mV	0 +/- 1.00

(e) On DAV, press FUND key.
(f) Verify that difference between readings on DAV and DMM is within tolerance as specified in table 3-3 (divide DMM reading by 100 if specified in table 3-3).
(g) On DAV press TOTAL key.
(h) Verify that difference between readings on DAV and DMM is within tolerance as specified in table 3-3 (divide DMM reading by 100 if specified in table 3-3).
(i) On DAV, press PHASE ANGLE key.
(j) Verify reading on DAV is within tolerance as specified in table 3-3.
(k) On DAV, press READ REF key. Observe LED on READ REF key is lit (DAV set for REF channel measurement).
(l) Repeat steps (e) through (h).
(m) On DAV, press READ REF key and observe that LED on READ REF key goes out (DAV set for SIG channel measurement).
(n) Repeat steps (b) through (m) for remaining test setup "A", 10 Hz (or frequency specified in table 3-3, for subsequent steps) settings listed in table 3-3.
(o) Turn phase generator output off.
(p) Reconfigure test setup for "B" configuration as shown in figure 3-2.
(q) Set DMM range to setting specified for first setup "B" test.
(r) Press DAV range key indicated for first setup "B" test.
(s) Set DAV to TOTAL (AVG) mode by setting all switches on Autocal CCA A8SW1 DIP switch to the OFF position.
(t) Turn phase generator output on.
(u) Repeat steps (b) through (m) for all test setup "B", 10 Hz (or frequency specified in table 3-3, for subsequent steps) settings listed in table 3-4.
(v) Turn phase generator output off.
(w) Reconfigure test setup for "C" (or "D" for frequencies of 20 kHz or higher) configuration as shown in figure 3-2.
(x) Set DMM range to setting specified for first setup "C" (or "D") test.
(y) Press DAV range key indicated for first setup "C" (or "D") test.
(z) Turn phase generator output on.
(aa) Repeat steps (b) through (m) for all test setup "C" (or "D"), 10 Hz (or frequency specified in table 3-3, for subsequent steps) settings listed in table 3-3.
(ab) Turn phase generator off.

10. Reconfigure test setup for "A" configuration as shown in figure 3-2.

11. On phase generator, adjust output frequency to 50 Hz (or next frequency specified in table 3-3, for subsequent steps).

12. Set DMM range to 100 V.

13. On DAV, press 200 V range key.

14. On phase generator, set output to on.

15. After DAV initializes and locks, press CAL key.

16. Observe calibration sequence goes to completion on DAV display panel.

17. Repeat step 9 for all 50 Hz (or frequency specified in table 3-3, for subsequent steps) test voltage levels specified in table 3-3.

18. Repeat steps 10 through 17 for all frequencies specified in table 3-3.

g. RATIO ACCURACY TEST.

1. Pretest conditions:

(a) DAV top cover on.
(b) DAV and test equipment on and warmed up. Phase generator output set to off.

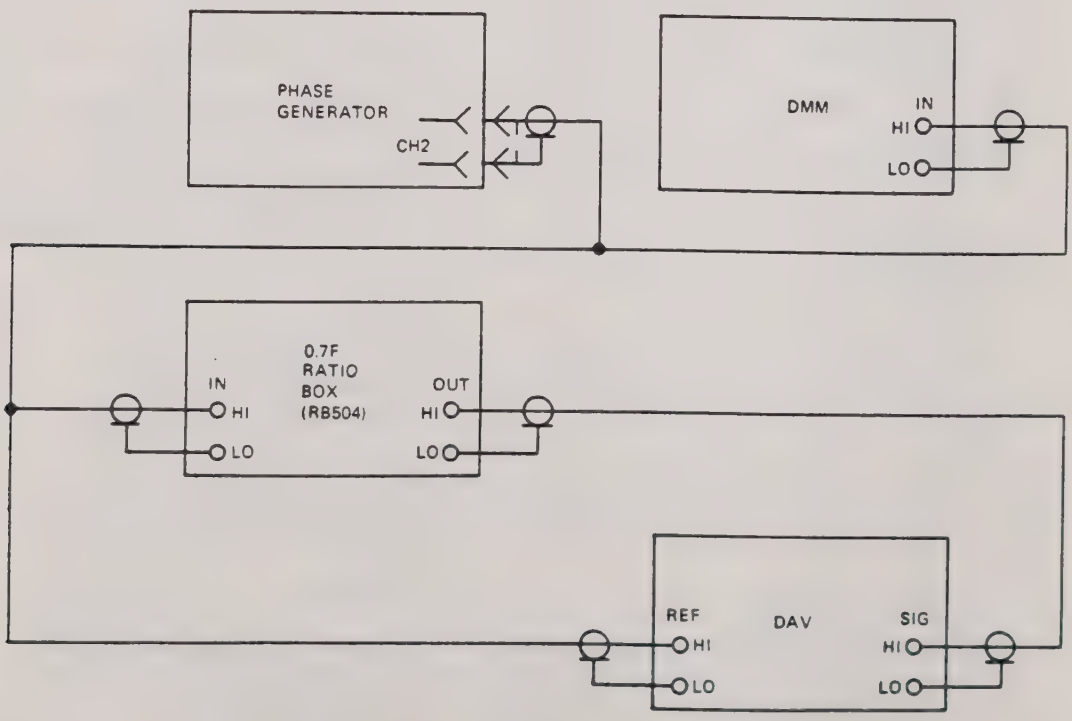


Figure 3-3. Ratio Accuracy Test and Recorder Output and Bar Graph Test, Test Setup Diagram

(c) Test set up as shown in figure 3-3.
(d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
(e) Press CLEAR VAR key to clear any preset variables from memory.
(f) Press FUND key.

2. Set ratio box to 1.000000.

3. On phase generator, set CH 2 output for a 400 Hz, 10 V rms, 0 ohms, sine wave.

4. Set phase generator output to on.

5. Adjust phase generator for 10 V ±0.1 V rms reading on DAV display.

6. After DAV initializes and locks, press CAL key.

7. Observe calibration sequence goes to completion on DAV display.

8. On DAV, press FUND key and then RATIO key.

9. Set ratio box to settings indicated in table 3-4.

10. On DAV, press ratio range key indicated in table 3-4.

Table 3-4. Ratio Accuracy Test Specifications

RATIO BOX SETTING	DAV RATIO RANGE KEY	NOMINAL DAV READING	RATIO ACCURACY TOLERANCE SPECIFICATION
1.00000	1R	1.0000	±0.0015
0.10000	0.1R	100.00×10^{-3}	$\pm 0.15 \times 10^{-3}$
0.01000	0.01R	10.000×10^{-3}	$\pm 0.15 \times 10^{-3}$
0.00100	0.01R	1.000×10^{-3}	$\pm 0.010 \times 10^{-3}$

11. Observe that DAV readings are within tolerance as specified in table 3-4.

12. Repeat steps 9 through 11 until all ratio box settings covered in table 3-4 have been satisfied.

13. Adjust ratio box until DAV display reads a ratio of exactly 0.5000.

14. On DAV, press 0.1R range key and dB key. Displayed value should read -6.02 ±0.01 dB.

h. PHASE ACCURACY CHECK AT 400 Hz.

1. Pretest conditions:

   (a) DAV top cover on.
   (b) DAV and test equipment on and warmed up. Phase generator output set to off.
   (c) Test set up as shown in figure 3-4.
   (d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
   (e) Press CLEAR VAR key to clear any preset variables from memory.
   (f) Press FUND key.

2. On phase generator, set channel 1 and channel 2 outputs for a 400 Hz, 10 V rms, 0 ohms, sine wave, 0° phase angle.

3. Set phase generator output to on.

4. After DAV initializes and locks, press CAL key.

5. Observe calibration sequence goes to completion on DAV display panel.

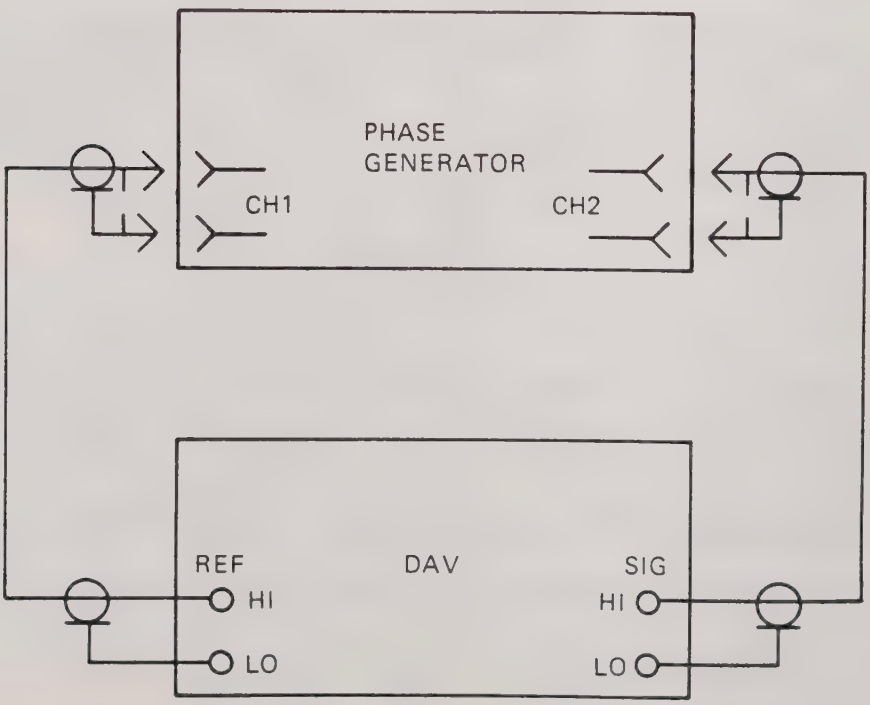


Figure 3-4. Phase Accuracy, Phase Variable, and Square Wave Sensitivity Test, Test Setup Diagram

6. On DAV, press PHASE ANGLE key.

7. On phase generator, set CH 2 to each phase angle listed in table 3-5 and check DAV display at each angle. (Refer to step 8 for additional readings to be taken at 45°.) Readings on DAV display should be within tolerance as specified in table 3-5 at each setting.

8. At 45°, normalize ratio mode by performing the following steps:

   (a) On DAV, press FUND, RATIO, VAR SCALE, and ENTER keys, in that sequence.
   (b) After DAV initializes and locks, press IN PHASE key. Check that reading on DAV display is within tolerance listed in table 3-5.
   (c) On DAV, press QUAD key. Check that reading on DAV display is within tolerance listed in table 3-5.
   (d) On DAV, press CLEAR VAR key.
   (e) On DAV, press PHASE ANGLE key. Go to next phase angle setting in table 3-5.

Table 3-5. Phase Accuracy at 400 Hz Test Specifications

PHASE ANGLE DATA: 400 Hz, 10 V

ANGLE IN DEGREES	PHASE ANGLE TOLERANCE SPECIFICATION	IN-PHASE RATIO/ QUAD RATIO SPECIFICATION (45° ONLY)
0	±0.05°	
1	±0.05°	
5	±0.05°	
30	±0.05°	
45	±0.05°	0.70711 ± 0.0013
60	±0.05°	
90	±0.05°	
120	±0.05°	
135	±0.05°	
150	±0.05°	
180	±0.05°	
225	±0.05°	
270	±0.05°	
359	±0.05°	
0	±0.05°	

i. SQUARE WAVE SENSITIVITY CHECK.

1. Pretest conditions:

   (a) DAV top cover on.
   (b) DAV and test equipment on and warmed up. Phase generator output set to off.
   (c) Test set up as shown in figure 3-4.
   (d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
   (e) Press CLEAR VAR key to clear any preset variables from memory.
   (f) Press FUND key.

2. On phase generator, set channel 1 and channel 2 outputs for 400 Hz, 5 V peak-to-peak, 0 ohms, 0° phase angle, square wave.

3. Set phase generator output to on.

4. ON DAV, press PHASE ANGLE key.

5. Observe that DAV initializes and locks.

6. On phase generator, adjust CH 2 for phase angle of 2.2°. Check that DAV display reads 2.2° ± 0.05°.

j. PHASE VARIABLES CHECK.

1. Pretest conditions:

   (a) DAV top cover on.
   (b) DAV and test equipment on and warmed up. Phase generator output set to off.
   (c) Test set up as shown in figure 3-4.
   (d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
   (e) Press CLEAR VAR key to clear any preset variables from memory.
   (f) Press FUND key.

2. On phase generator, set channel 1 and channel 2 outputs for a 400 Hz, 5 V rms, 0 ohms, sine wave.

3. Set phase generator output to on.

4. When DAV initializes and locks, press CAL key.

5. Observe calibration sequence goes to completion on DAV display, then press PHASE ANGLE key.

6. On phase generator, adjust CH 2 phase angle for a reading of 90.00o ± 0.01o on DAV display.

7. On DAV, press in turn PHASE OFFSET, 9, 0, and ENTER keys. Display for 90° offset should read 0.00° ±0.01°.

8. On DAV, press CLEAR VAR key. Display should read 90.00° ±0.01°.

9. On DAV, press in turn VAR SCALE, 2, and ENTER keys. Display should read 180.00° ±0.02°.

10. On DAV, press CLEAR VAR key.

11. On phase generator, adjust CH 2 phase angle output for a reading of 270.00° ±0.01° on DAV display.

12. On DAV, press PHASE ANGLE key and then press ±180° key. Display should read -90.00° ±0.01°.

13. On DAV, press CLEAR VAR key.

k. COMMON MODE REJECTION.

1. Pretest conditions:

   (a) DAV top cover on.
   (b) DAV and test equipment on and warmed up. Phase generator output set to off.
   (c) Test set up as shown in figure 3-5.
   (d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
   (e) Press CLEAR VAR key to clear any preset variables from memory.
   (f) Press FUND key.

2. On phase generator, set CH 2 output for 400 Hz, 10 V rms, 0 ohms, sine wave.

3. Set phase generator output to on.

4. After DAV initializes and locks, press FUND key.

5. Adjust power amplifier for a gain of 10, ac coupling, and 0 V offset.

6. Observe that voltage measured on the DMM is approximately 100 V rms.

7. On DAV, press CAL key.

8. Observe calibration sequence goes to completion.

9. On DAV, press 20 mV range key, RATIO, and dB keys.

10. Verify reading on display is more negative than -126 dB.

11. Adjust phase generator output to 999 Hz.

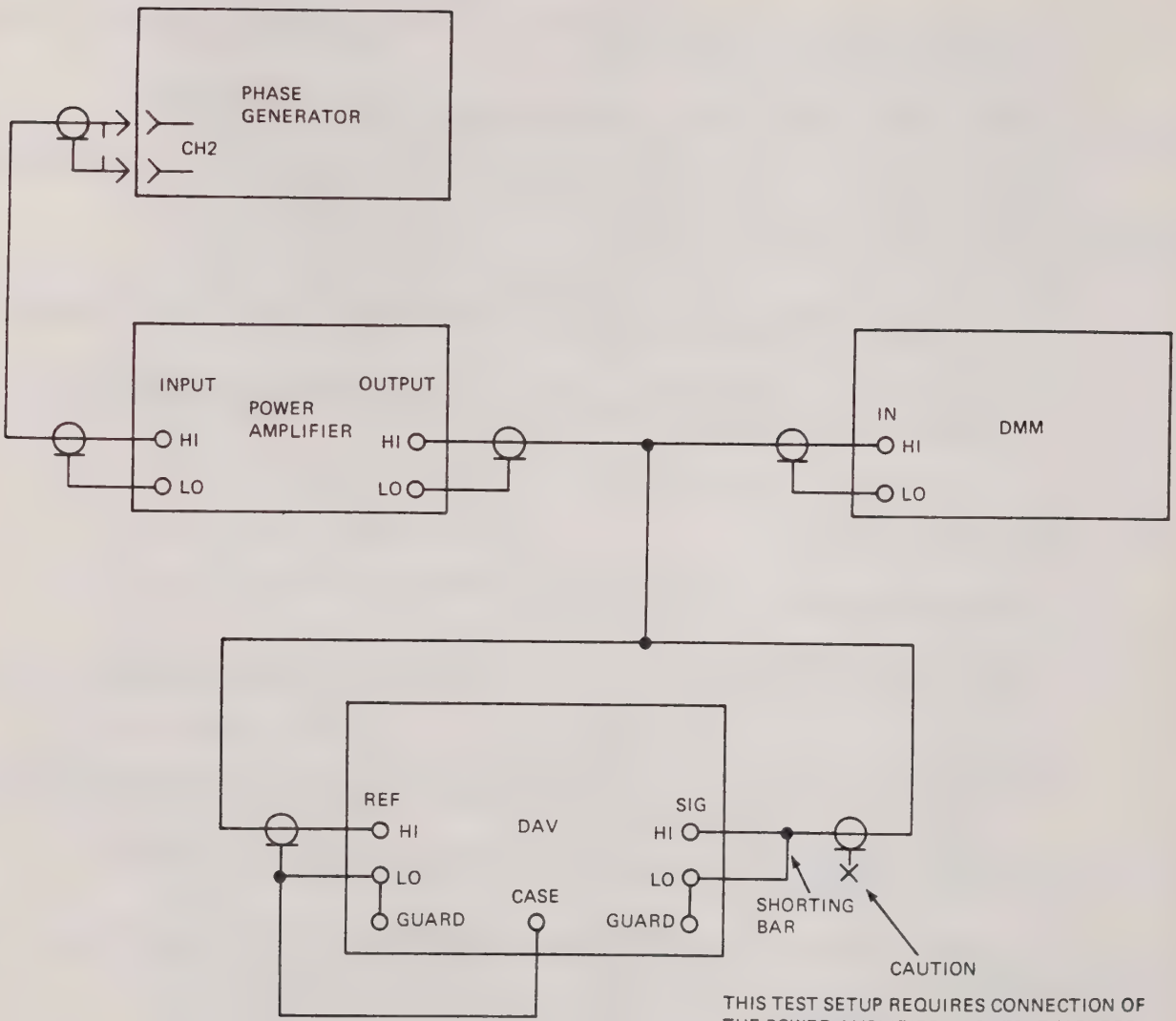


Figure 3-5. Common Mode Rejection, Test Setup Diagram

12. On DAV, press in turn FREQ, 9,9,9, and ENTER keys.

13. Repeat steps 6 through 10.

14. On DAV, press CLEAR VAR key and adjust phase generator to 5 kHz.

15. Repeat steps 6 through 10 except reading on display should be more negative than -110 dB.

16. Adjust phase generator output frequency to 32 kHz.

17. Repeat steps 6 through 10 except reading on display should be more negative than -100 dB.

l. TOTAL MODE NOISE TEST.

1. Pretest conditions:

(a) DAV top cover on.
(b) DAV set for TOTAL (SUM) operation (see Instruction Manual).
(c) DAV and test equipment on and warmed up. Phase generator output set to off.
(d) Test set up as shown in figure 3-6.
(e) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
(f) Press CLEAR VAR key to clear any preset variables from memory.
(g) Press FUND key.

2. On phase generator, set CH 2 output for 400 Hz, 10 V rms, 0 ohms, sine wave.

3. Set phase generator output to on.

4. Observe that DAV initializes and locks.

5. On DAV, press TOTAL and AUTORANGE keys.

6. Observe that DAV ranges down to 20 mV range as indicated by LED on 20 mV range key.

7. Observe that DAV total mode noise reading is 35 uV maximum.

m. TOTAL HARMONIC DISTORTION TEST.

1. Pretest conditions:

(a) DAV top cover on.
(b) DAV and test equipment on and warmed up. Phase generator output set to off.

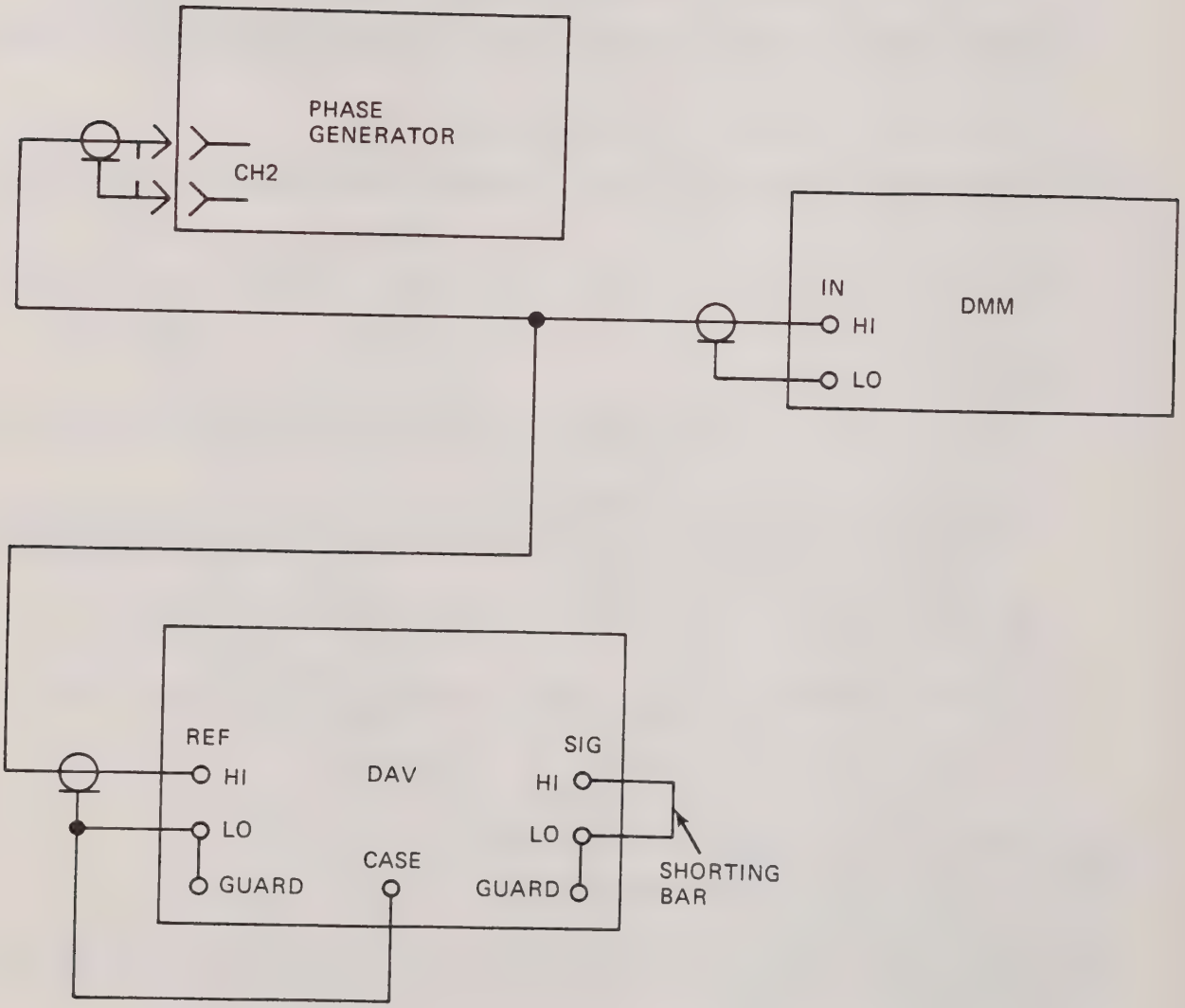


Figure 3-6. Total Mode Noise, Test Setup Diagram

(c) Test set up as shown in figure 3-7.
(d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
(e) Press CLEAR VAR key to clear any preset variables from memory.
(f) Press FUND key.

2. On phase generator, set CH 2 output for 400 Hz, 10 V rms, 0 ohms, sine wave.

3. Set phase generator output to on.

4. On DAV, press AUTORANGE and THD keys.

5. Observe that sine wave distortion as read on distortion analyzer is less than V 0.05%.

6. Observe distortion reading on DAV is within ±0.03% of distortion analyzer reading.

7. On phase generator, set CH 2 output for a 400 Hz, 10 V peak-to-peak, triangle wave.

8. Observe that DAV triangle wave distortion as read on DAV display is within ±1.0% of distortion analyzer reading.

n. HARMONIC MEASUREMENT TEST.

1. Pretest conditions:

(a) DAV top cover on.
(b) DAV and test equipment on and warmed up. Phase generator output set to off.
(c) Test set up as shown in figure 3-7. Do not connect distortion analyzer.
(d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
(e) Press CLEAR VAR key to clear any preset variables from memory.
(f) Press FUND key.

2. On phase generator, set CH 2 output for 400 Hz triangle wave, 3.47 V peak-to-peak.

3. Set phase generator output to on.

4. Observe that DAV initializes and locks.

5. On DAV, press in turn TOTAL, 2 V range, OFFSET, 1, and ENTER keys.

6. On phase generator, adjust amplitude for null on DAV bar meter at bottom of DAV display.

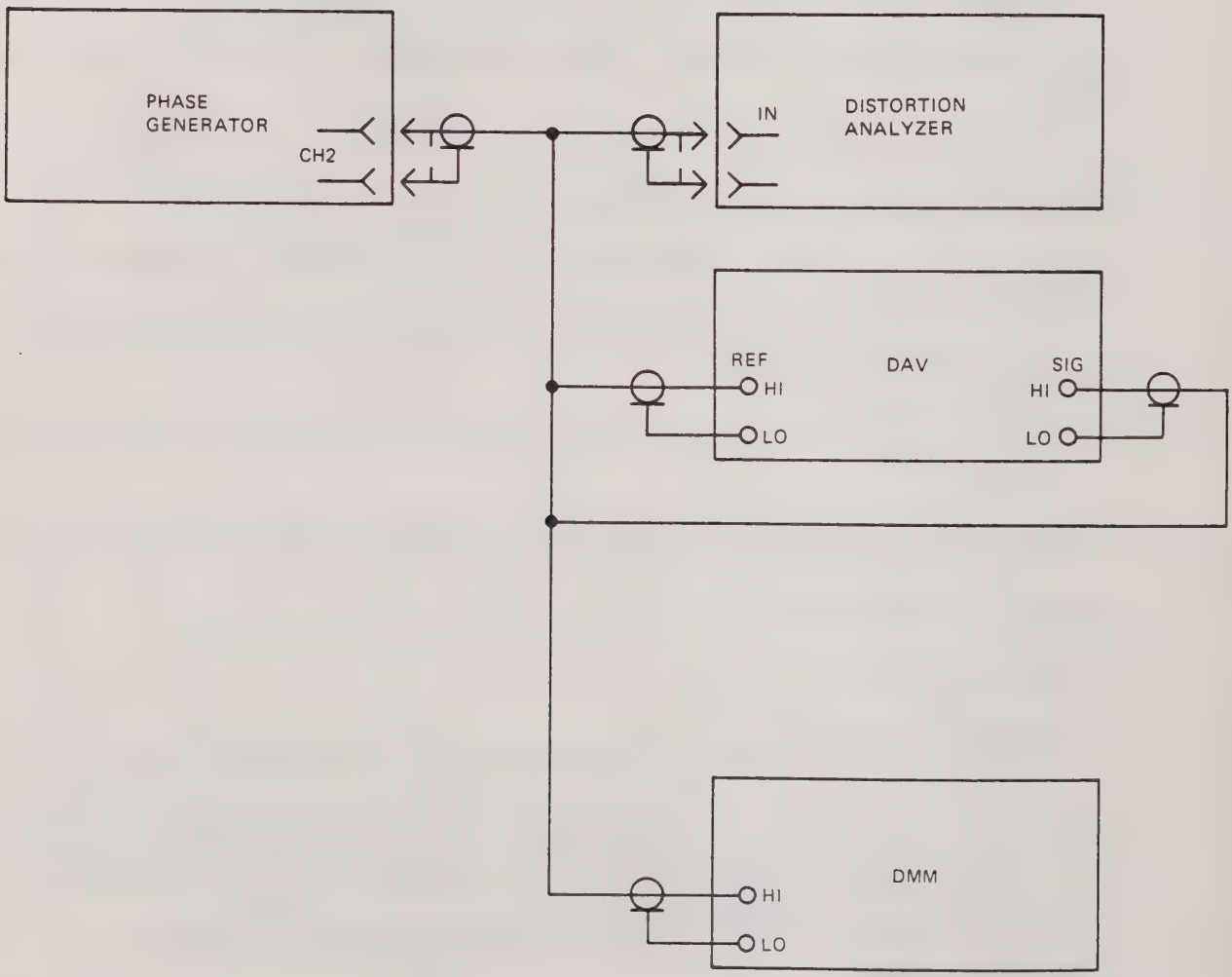


Figure 3-7. Harmonic Distortion, Harmonic, Frequency Measurement and Lock Time, Cal Time, Test Setup Diagram

7. On DAV, press CLEAR VAR key. Compare DMM and DAV display readings. Check to see that difference in TOTAL voltage readings is within tolerance as specified in table 3-6.

8. On DAV, press FUND key. Verify FUND voltage reading is within tolerance as specified in table 3-6.

9. On DAV, press PHASE ANGLE key. Verify reading is within tolerance as specified in table 3-6.

10. On DAV, press FUND, then in turn HMNC, 3, and ENTER keys. Verify harmonic voltage reading is within tolerance as specified in table 3-6.

11. On DAV, press PHASE ANGLE key. Verify that reading is within tolerance as specified in table 3-6.

12. Repeat steps 10 and 11 for remaining harmonics listed in table 3-6.

o. FREQUENCY MEASUREMENT TEST.

1. Pretest conditions:

(a) DAV top cover on.

Table 3-6. Harmonic Measurement (400 Hz Triangle Wave) Test Specifications

HARMONIC	VOLTAGE	HARMONIC VOLTAGE TOLERANCE SPECIFICATION	PHASE ANGLE	HARMONIC PHASE ANGLE TOLERANCE SPECIFICATION
TOTAL	1.0000 V	0.0015 V	--	--
FUND	0.9927	0.0015 V	0°	±0.05°
3rd	0.1103 V	0.0011 V	180°	±0.15°
5th	0.0397 V	0.0010 V	0°	±0.25°
7th	0.0203 V	0.0010 V	180°	±0.70°
9th	0.0123 V	0.0010 V	0°	±0.90°

(b) DAV and test equipment on and warmed up. Phase generator output set to off.
(c) Test set up as shown in figure 3-7. Do not connect distortion analyzer.
(d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.

NOTE

In procedures that follow, use a stopwatch to get a reading on elapsed time between time CAL key is pressed and time calibration sequence stops (CAL display ends).

5. On DAV, press CAL key while starting stopwatch. Elapsed time on stopwatch to end of calibration sequence should be less than 60 seconds.

6. Repeat step 5 for other three frequencies listed in table 3-9. Elapsed time to end of calibration sequence should be within tolerance as specified in table 3-9 for each frequency.

Table 3-9. CAL Time Test Specification

FREQUENCY	CAL TIME TOLERANCE SPECIFICATION (MAXIMUM)
10 Hz	70 seconds
400 Hz	40 seconds
20 kHz	23 seconds
100 kHz	20 seconds

r. IEEE TEST.

1. Pretest conditions:

   (a) DAV top cover on.
   (b) DAV and test equipment on and warmed up. Phase generator output set to off.
   (c) Test set up as shown in figure 3-8.
   (d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
   (e) Press CLEAR VAR key to clear any preset variables from memory.
   (f) Press FUND key.

2. On phase generator, set CH 2 output for 400 Hz, 5.0 V peak-to-peak, 0 ohms, sine wave.

3. Set phase generator output to on.

4. Observe that DAV initializes and locks.

5. Observe LED on LOCAL key. If lit, press LOCAL key and observe that LED goes out.

6. Load IEEE Test Program into IEEE controller. (See figure 3-9 for listing.)

7. Set IEEE address on DAV as shown in figure 3-8.

8. Run IEEE Test Program and follow instructions on CRT.

9. Verify data with sample data sheet shown in figure 3-10.

s. RECORDER OUTPUT AND BAR GRAPH TEST.

1. Pretest conditions:

   (a) DAV top cover on.
   (b) Set up recorder output for 2.0 V = full scale output (see Instruction Manual).
   (c) DAV and test equipment on and warmed up. Phase generator output set to off.

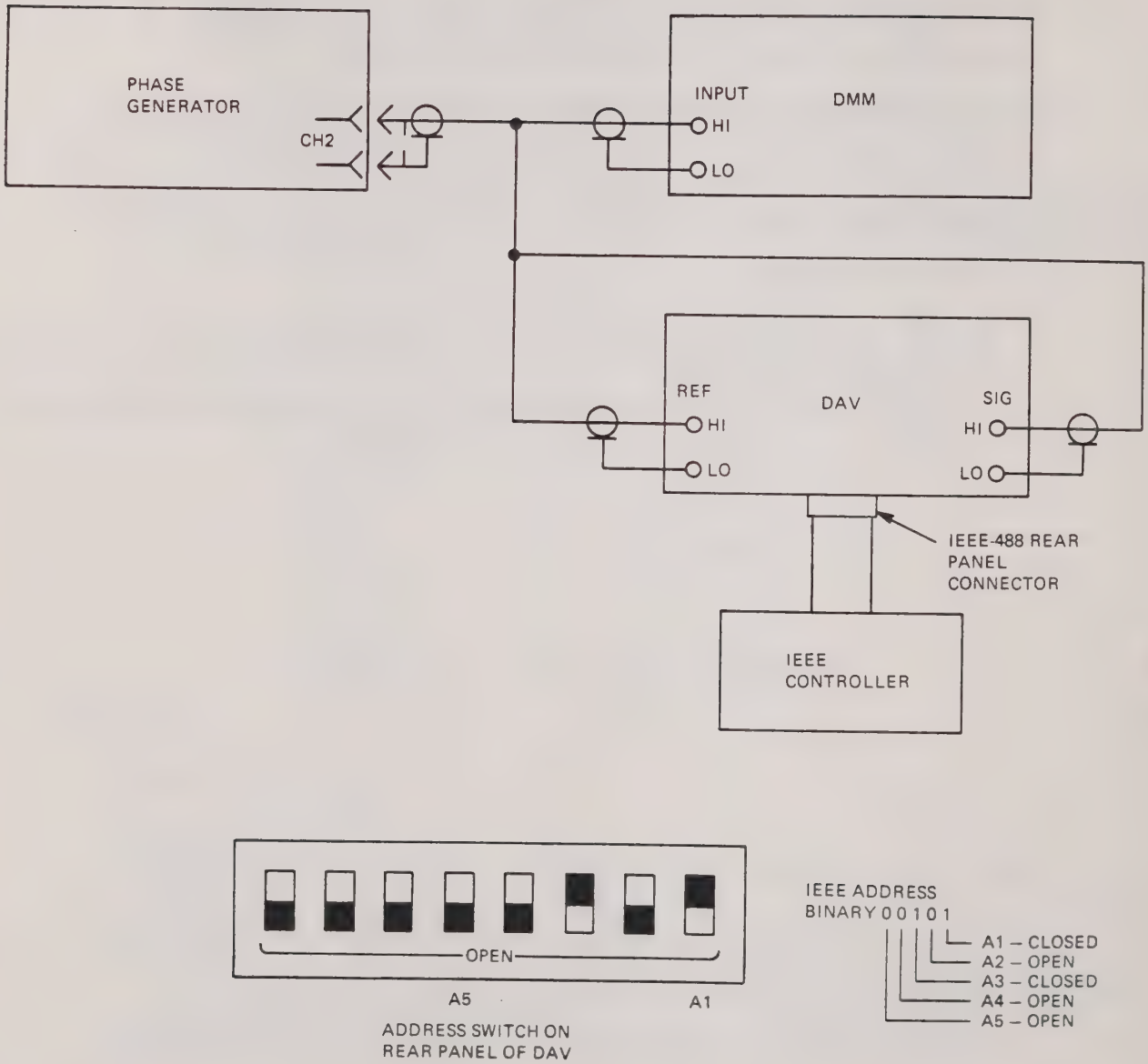


Figure 3-8. IEEE Tests, Test Setup Diagram

```
10 CLEAR
20 PRINT "********************************"
30 PRINT "IEEE TEST PROGRAM MODEL 2250"
40 PRINT "********************************"
50 PRINT "NORTH ATLANTIC IND."
60 PRINT "JUNE 2, 1985"
70 PRINT "********************************"
80 PRINT
90 PRINT "PRESENT STATUS IS"
100 PRINT
110 DIM S$[400]
120 OUTPUT 705 ;"STA"
130 ENTER 705 ; S$
140 PRINT S$
150 PRINT
160 PRINT
170 OUTPUT 705 ;"INX FREQ"
180 ENTER 705 ; F
190 PRINT "FREQUENCY =";F;"Hz"
200 OUTPUT 705 ;"SET AVRG 0.05"
210 OUTPUT 705 ;"SET CALB"
212 OUTPUT 705 ;"INX MAIN"
215 ENTER 705 ; C$
217 DISP C$
220 IF C$=" CAL" THEN 215
230 PRINT
240 PRINT
250 PRINT
260 OUTPUT 705 ;"SRX VOLT 20"
270 WAIT 3000
280 OUTPUT 705 ;"FNC RMSV"
290 WAIT 3000
300 OUTPUT 705 ;"INX MAIN"
310 ENTER 705 ; T
320 PRINT "TOTAL =";T;"VOLTS"
330 PRINT
340 PRINT
350 OUTPUT 705 ;"FNC FUND"
360 WAIT 3000
370 OUTPUT 705 ;"INX MAIN"
380 ENTER 705 ; V
390 PRINT "FUND =";V;"VOLTS"
400 PRINT
410 PRINT
420 OUTPUT 705 ;"FNC INPH"
430 WAIT 3000
440 OUTPUT 705 ;"INX MAIN"
450 ENTER 705 ; I
460 PRINT "INPH =";I;"VOLTS"
470 PRINT
480 PRINT
490 OUTPUT 705 ;"FNC QUAD"
```

Figure 3-9. IEEE Test Program (Sheet 1 of 2)

```
500 WAIT 3000
510 OUTPUT 705 ;"INX MAIN"
520 ENTER 705 ; Q
530 PRINT "QUAD =";Q;"VOLTS"
540 PRINT
550 PRINT
560 OUTPUT 705 ;"FNC PANG"
570 WAIT 3000
580 OUTPUT 705 ;"INX MAIN"
590 ENTER 705 ; P
600 PRINT "PHASE ANGLE =";P;"DEGREES"
610 PRINT
620 PRINT
630 OUTPUT 705 ;"FNC DSTR"
640 WAIT 4000
650 OUTPUT 705 ;"INX MAIN"
660 ENTER 705 ; D
670 PRINT "THD =";D;"%"
680 DISP "OBSERVE THE FRONT PANEL AND"
690 DISP "VERIFY EACH RANGE CHANGE" @ BEEP 10, 1500
700 WAIT 3000
710 OUTPUT 705 ;"FNC RMSV"
720 WAIT 3000
730 OUTPUT 705 ;"SRX VOLT AUTO"
740 WAIT 3000
750 OUTPUT 705 ;"SRX VOLT 500"
760 WAIT 3000
770 OUTPUT 705 ;"SRX VOLT 200"
780 WAIT 3000
790 OUTPUT 704 ;"SRX VOLT 20"
800 WAIT 3000
810 OUTPUT 705 ;"SRX VOLT 2"
820 WAIT 3000
830 OUTPUT 705 ;"SRX VOLT .2"
840 WAIT 3000
850 OUTPUT 705 ;"SRX VOLT .02"
860 WAIT 3000
870 OUTPUT 705 ;"SRX VOLT AUTO"
880 WAIT 3000
890 DISP "OBSERVE THE FRONT PANEL AND"
900 DISP "VERIFY AN OFFSET OF -45 DEGREES"
910 DISP "IS ENTERED" @ BEEP 10, 1500
920 WAIT 3000
930 OUTPUT 705 ;"FNC PANG"
940 WAIT 3000
950 OUTPUT 705 ;"SET POFF 45.00"
960 WAIT 3000
970 OUTPUT 705 ;"SET POFF 0"
980 WAIT 3000
990 LOCAL 705
1000 PRINT "TEST COMPLETE"
1010 END
```

Figure 3-9. IEEE Test Program (Sheet 2 of 2)

****

IEEE TEST PROGRAM MODEL [illegible]

****

NORTH ATLANTIC IND.

JUNE 1,1985

****

PRESENT STATUS IS

[illegible]

FREQUENCY = [illegible] Hz

TOTAL = [illegible] VOLTS

FUND = [illegible] VOLTS

INPH = [illegible] VOLTS

QUAD = [illegible] VOLTS

PHASE ANGLE = [illegible] DEGREES

THD = [illegible] %

TEST COMPLETE

Figure 3-[illegible]. Sample Data Sheet for IEEE Test

(c) Test set up as shown in figure 3-11.
(d) Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
(e) Press CLEAR VAR key to clear any preset variables from memory.
(f) Press FUND key.

2. On phase generator, set CH 2 output for 400 Hz, 1 V rms, 0 ohms, sine wave.

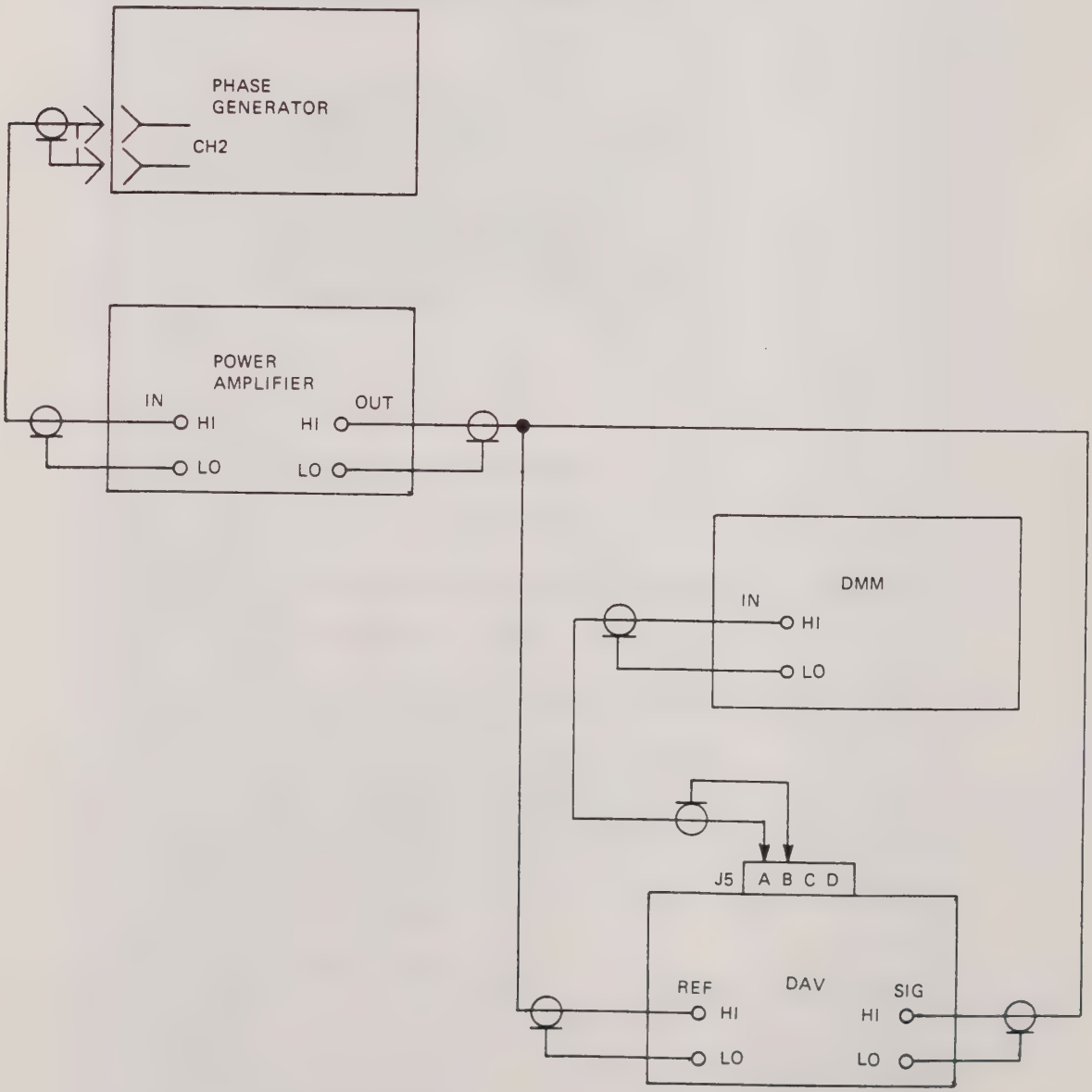


Figure 3-11. Recorder Output and Bar Graph Test

3. Set phase generator output to on.

4. Adjust power amplifier for variable gain, ac coupling, and 0 volts offset.

5. After DAV initializes and locks, press CAL key.

6. On DAV, press 100 V range key.

7. Adjust power amplifier for a reading of 20.2 ±0.01 V rms on DAV display.

8. While observing null meter at bottom of DAV display, sweep signal input from 20 V to 0 V, using power amplifier gain adjustment. Check that each bar graph segment lights in sequence.

9. On DAV, press in turn the VAR SCALE, +/-, and 1 keys.

10. Repeat step 8. Observe operation of left half of null meter is normal.

11. On DAV, press CLEAR VAR key and adjust power amplifier for reading of 20 ±0.01 V rms on DAV display.

12. Using DMM, measure dc voltage between J5-A (HI) and J5-B (LO) on rear panel. Check that reading is within tolerance listed in table 3-10.

13. Repeat step 12 but measure between J5-C (HI) and J5-D (LO) on rear panel.

14. On DAV, press in turn PHASE OFFSET, 2, 7, 0, and ENTER keys (sets 270° offset). Repeat steps 12 and 13. Check to see readings are within tolerance listed in table 3-10.

15. On DAV, press in turn PHASE OFFSET, 1, 3, 5 and ENTER keys (sets 135° offset). Repeat steps 12 and 13. Check to see readings are within tolerance listed in table 3-10.

Table 3-10. Recorder Output Test Specifications

OFFSET SETTING	PHASE ANGLE READING	TOLERANCE SPECIFICATION
		In Phase Output J5-A and B
-	0°	2 ±.003 V dc
270	90°	0±.003 V dc
135	225°	-1.414 ±.0027 V dc
		Quad Output J5-C and D
-	0°	0 ±.003 V dc
270	90°	2 ±.003 V dc
135	225°	-1.414 ±.0027 V dc

3-4. ALIGNMENT.

A complete alignment procedure for the DAV is given in the following subparagraphs. These procedures may be performed as a set as part of periodic maintenance. Alternately, a specific procedure may be used to adjust an individual assembly following repair or replacement of that assembly. (Refer to table 3-11 for the required sequence of alignment procedures.) Each procedure is presented in a step-by-step format and references a test setup figure. The test setup figure illustrates the complement of test equipment necessary to perform the alignment and shows all the required interconnections between the test equipment and the DAV. (Refer to table 1-6 for specific test equipment requirements and figure 6-27 for test point and DIP switch locations.) Prior to performing a complete DAV alignment or a single alignment procedure, establish the pretest conditions presented in paragraph 3-4.a. and perform the prealignment test provided in paragraph 3-4.b. If during performance of any alignment procedure, the required results cannot be attained, refer to the troubleshooting procedures provided in section 4 of this manual.

Table 3-11. Alignment Procedure Sequence

NOTE

If more than one board is out of alignment then the complete alignment procedure must be performed.

Ref. Des.	Alignment Description
A5	Phase-Locked Loop (PLL) Board
A8	Autocal Board
A9/A12	A/D Converter Timing
A9/A12	A/D Converter Offset and Gain
A11/A14	Front End Offset
A9/A12	A/D Converter TOTAL (AVG) Offset
A11/A14	Front End Frequency Response
A3	I/O Recorder Output

a. PRETEST CONDITIONS.

The following pretest conditions are common to all the alignment procedures. Establish these conditions prior to performing each procedure.

1. DAV top cover off.
2. DAV and test equipment on and warmed up for 30 minutes.
3. Variable signal source output set to minimum value.
4. Ensure that DAV is not in READ REF or RATIO mode by observing LEDs on READ REF and RATIO keys. If either LED is lit, press corresponding key and observe that LED goes out.
5. Press CLEAR VAR key to clear any preset variables from memory.
6. Press FUND key.

b. PREALIGNMENT TEST.

Perform the following prealignment test prior to performing a complete DAV alignment or following the repair or replacement of any assembly.

1. Adjust all trimpots on the assembly being aligned to their center positions (approximately nine turns from either end). If a complete alignment of the DAV is being performed, adjust all trimpots to their center positions.
2. Connect variable signal source to DAV reference input terminals as shown in figure 3-12. (DAV signal input terminals should be left unconnected.)
3. Set variable signal source for 500 Hz, 10 V rms.

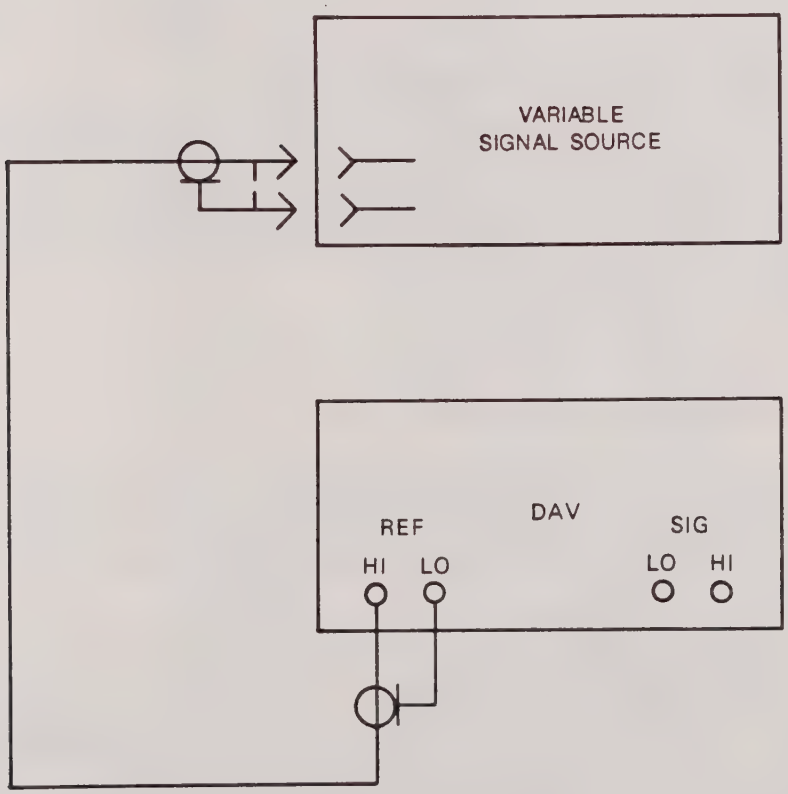


Figure 3-12. Prealignment Test Setup Diagram

4. On DAV, turn on power and verify that checksum appears on front panel display for a few seconds.

5. On DAV, press FUND key and verify that DAV locks at input frequency.

6. On DAV, press READ REF key, observe LED on READ REF key is lit, and DAV display reads approximately 10 V.

7. On DAV, press READ REF key and observe that LED on READ REF key goes out.

c. PHASE LOCKED LOOP (PLL) A5 ALIGNMENT.

To align Phase Locked Loop (PLL) A5, proceed as follows:

1. Set up equipment as shown in figure 3-13.
2. On Phase Locked Loop (PLL) A5, connect DMM between test points TP6 (HI) and TP7 (LO).
3. Adjust variable signal source to 110 Hz, 10 ±0.5 V rms and connect to DAV REF and SIG inputs.
4. Set DAV to FUND mode by pressing FUND key.
5. After DAV locks onto input frequency (NO LOC indication disappears), adjust A5R67 for a reading of 3.5 ±0.02 V dc on DMM (1.3 +0.1, -0 V dc for assemblies 787192-1 revision D or higher).
6. Adjust variable signal source for 1100 Hz, 10 ±0.5 V rms.
7. After DAV locks (NO LOC indication disappears), adjust A5R66 for a reading of 3.5 ±0.02 V dc on DMM (1.3 +0.1, -0 V dc for assemblies 787192-1 revision D or higher).

d. AUTOCAL A8 ALIGNMENT.

To align Autocal A8, proceed as follows:

1. Set up equipment as shown in figure 3-14.
2. On Autocal A8, set DIP switch A8SW1-1 to the ON position. This enables the step-by-step calibration mode.
3. Connect the distortion analyzer and oscilloscope to A8TP3 using A8J2-2 as ground.
4. On DAV, press FUND key.
5. On DAV, press FREQ, 1, 0, 0, 0, 0, ENTER in that order. This enters a frequency preset of 10.0 kHz.
6. On DAV, press CAL key. Observe that a calibration sequence begins and pauses with a phase angle displayed on the main display and the digit "1" displayed on the harmonic display.
7. Repeatedly press ENTER key until harmonic display has incremented to "7".
8. Verify that the signal at A8TP3 is roughly sinusoidal, 10 kHz ±900 Hz and approximately 13.0 volts peak-to-peak symmetrical about ground. (The exact values will be specified later.)
9. Disconnect oscilloscope and frequency counter.
10. On Autocal A8, adjust A8R6 for a minimum reading on the distortion analyzer.
11. On Autocal A8, adjust A8R8 for a minimum reading on the distortion analyzer.
12. On Autocal A8, adjust A8R9 for a minimum reading on the distortion analyzer.

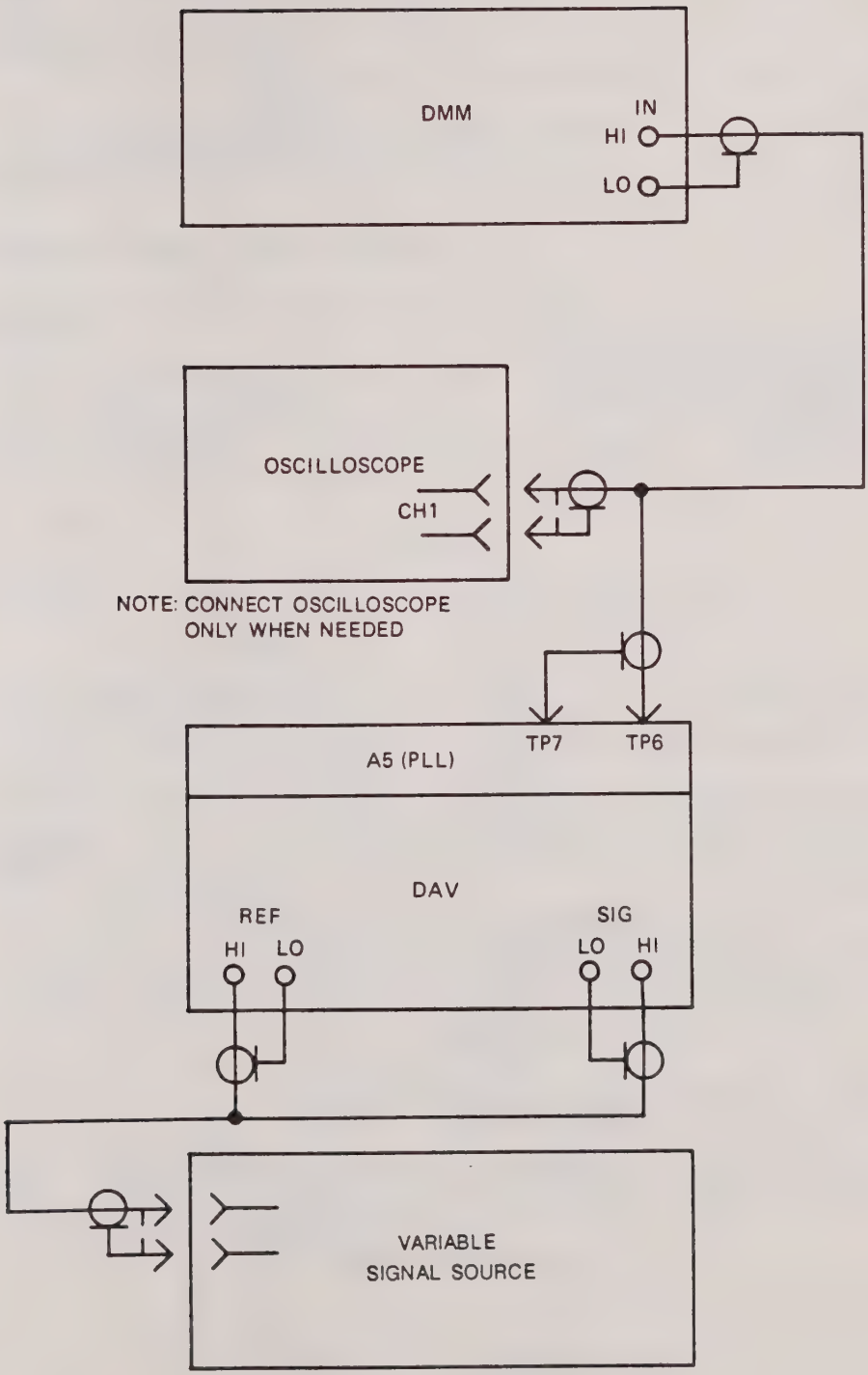


Figure 3-13. Phase Locked Loop Adjustment, Test Setup Diagram

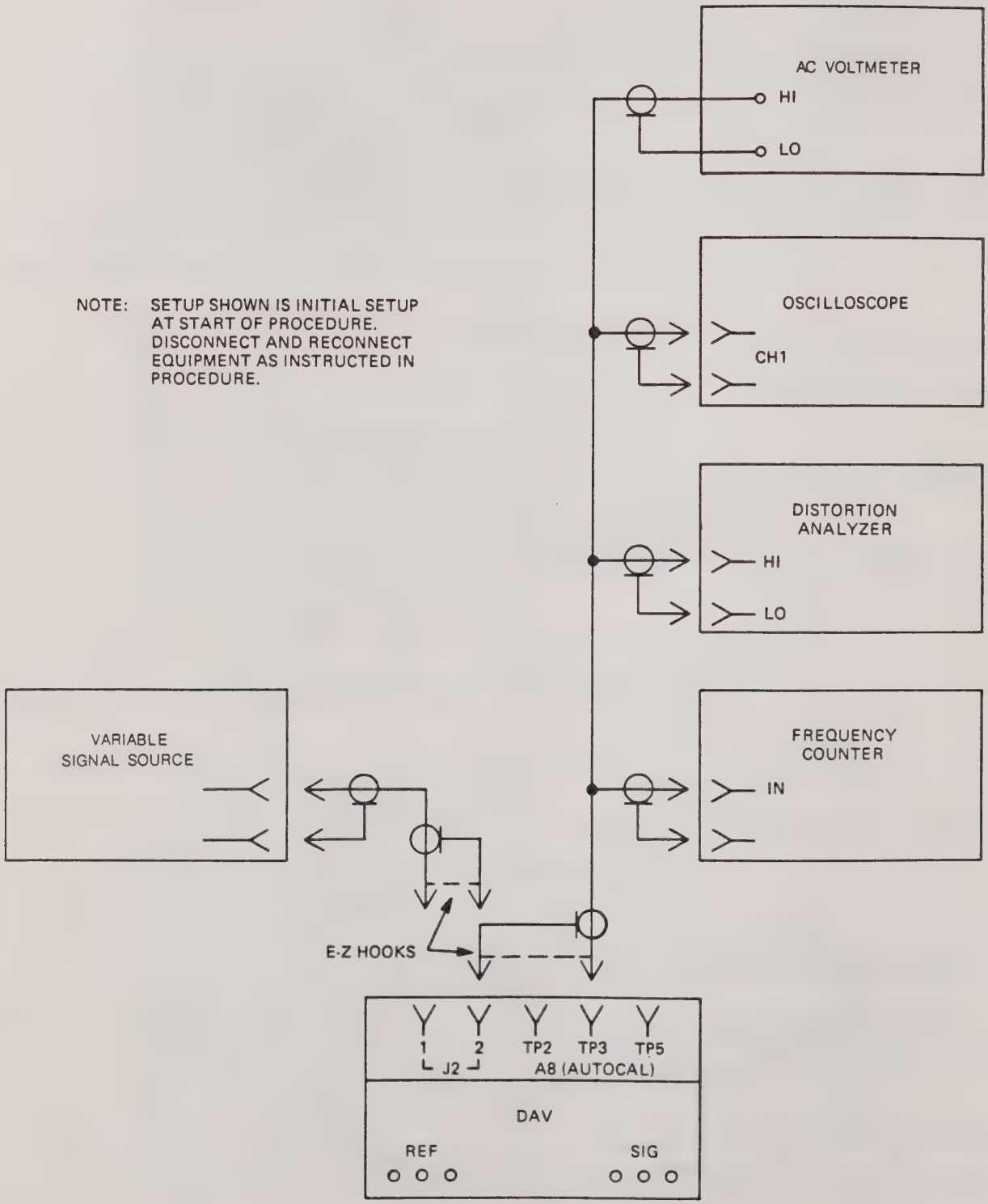


Figure 3-14. Autocal A8 Alignment, Test Setup Diagram

13. Repeat steps 10 through 12 as many times as necessary to bring the distortion reading to less than 0.60%.
14. Disconnect the distortion analyzer and connect ac voltmeter to A8TP3 with A8J2-2 as the ground.
15. On Autocal A8, adjust A8R13 for an indication at A8TP3 of 4.6 ±.005 V rms.
16. On Autocal A8, return DIP switch A8SW1-1 to the off position. This disables the step-by-step calibration mode.
17. Turn DAV power switch off and back on before continuing tests.

e. A/D CONVERTER A9/A12 TIMING ALIGNMENT.

To align A/D Converter A9/A12 timing, proceed as follows:

1. Set up equipment as shown in figure 3-15.
2. On DAV turn off power.
3. Remove Reference A/D Converter A9.
4. Install extender card (NAI Part No. 787731) in slot J10 and install Reference A/D Converter A9 removed in step 3 into extender card.

CAUTION

Be sure board is correctly oriented in extender card before turning on power.

5. Connect oscilloscope channel 1 probe to TP43 on extender card (use TP50 as ground). This signal is called START.
6. Connect oscilloscope channel 2 probe to TP42 on extender card (use TP50 as ground). This signal is called DONE.
7. Set oscilloscope to trigger on channel 1, time base to 0.2 microsecond per division, and each vertical amplifier to 2 volts per division.
8. Adjust variable signal source to 400 Hz, 10 ±0.5 V rms and connect to DAV REF and SIG inputs.
9. Turn on DAV power and observe that DAV locks.
10. On Reference A/D Converter A9, adjust A9R37 until time from rising edge of START signal to rising edge of DONE signal is between 1.9 and 2.0 microseconds. This timing is measured at the 2.4-volt point on each positive going edge. (See waveforms shown in figure 3-16.)
11. Turn off DAV power.
12. Remove extender card with Reference A/D Converter A9, remove Reference A/D Converter from extender card, and reinstall Reference A/D Converter A9 into slot J10.
13. Remove Signal A/D Converter A12, install extender card in slot J13, and install Signal A/D Converter A12 into extender card.
14. On DAV turn on power.

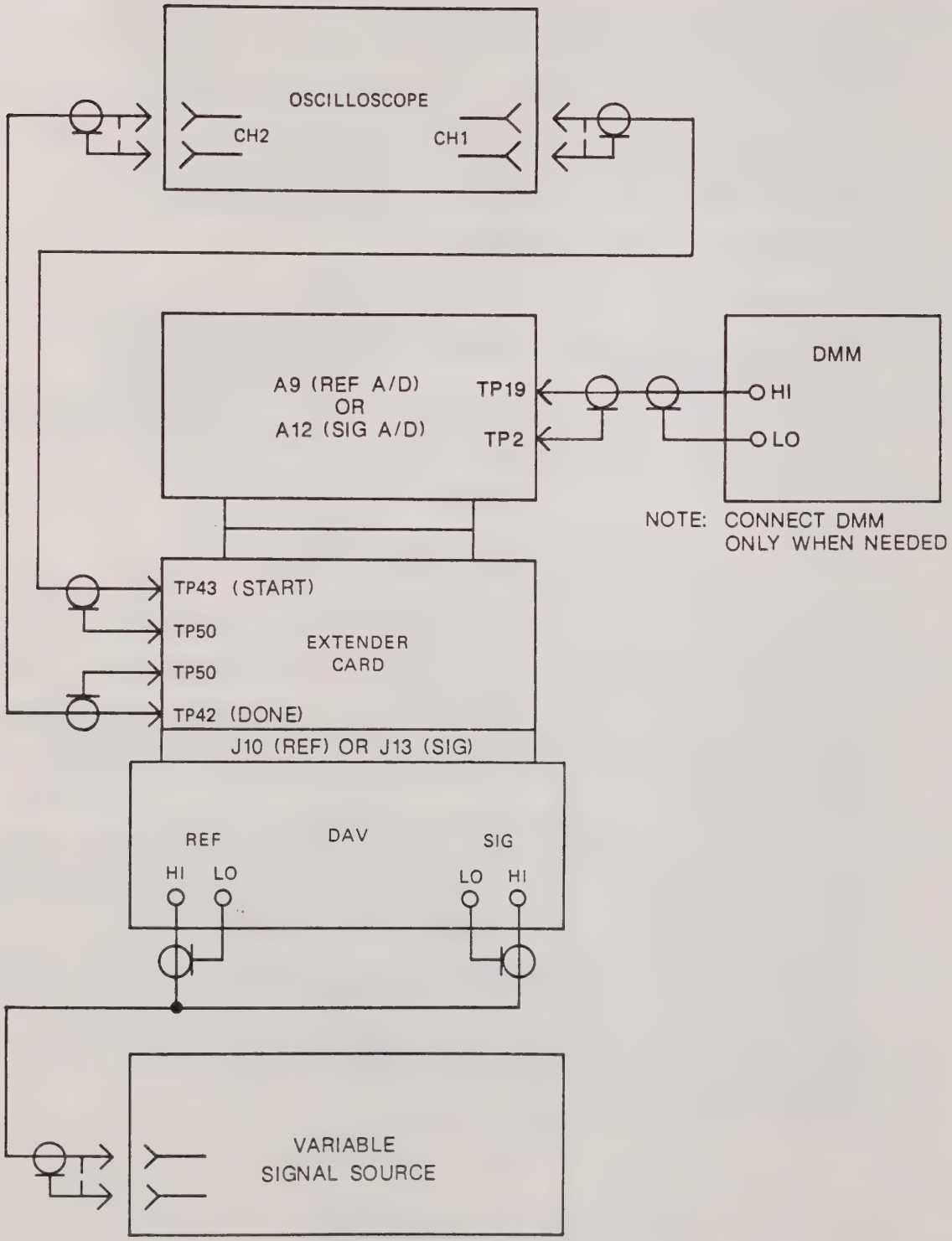
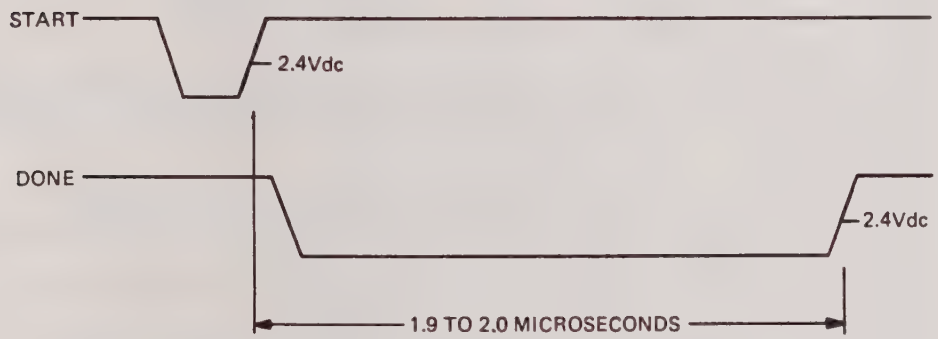


Figure 3-15. A/D Converter A9/A12 Timing Adjustment, Test Setup Diagram

15. Repeat steps (4) through (10) for Signal A/D Converter A12 with extender card in slot J13 and adjust A12R37 for the specified timing (figure 3-16).
16. On DAV turn off power.
17. Remove extender card with Signal A/D Converter, remove Signal A/D Converter from extender card, and install Signal A/D Converter A12 in slot J13.
18. On DAV turn on power.
19. Connect DMM to monitor Reference A/D Converter A9 A9TP19 (HI) and A9TP2 (LO).
20. Adjust A9R41 for 4.69 ±0.01 V dc as read on DMM.
21. Connect DMM to monitor Signal A/D Converter A12 A12TP1 using A12TP6 as ground.
22. Adjust A12R41 for 4.69 ±0.01 V dc as read on DMM.



NOTE: RISING AND FALLING EDGES OF WAVEFORMS ARE EXAGERATED FOR ILLUSTRATION PURPOSES.

Figure 3-16. A/D Converter A9/A12, Timing Adjustment Waveforms

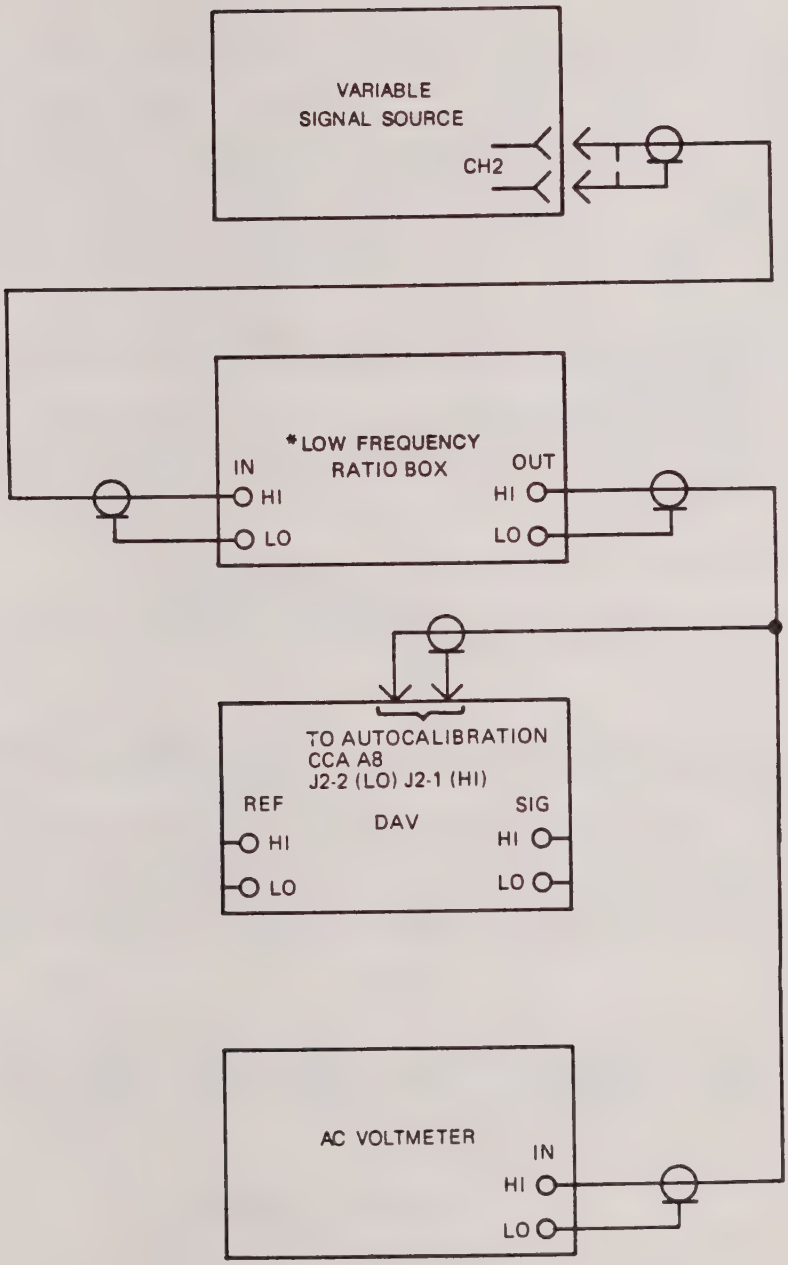
f. A/D CONVERTER A9/A12 OFFSET AND GAIN ADJUSTMENT.

To adjust A/D Converter A9/A12 offset and gain, proceed as follows:

1. Set up equipment as shown in figure 3-17.
2. Set variable signal source for 400 Hz, 0.75000 ±0.0001 V rms (use Low Frequency ratio box for fine adjustment, if needed). Monitor and readjust signal source prior to each adjustment.
3. Connect a cable from variable signal source to Autocal A8 A8J2-1 (HI) and A8J2-2 (LO). (Use shortest possible RG-58U coaxial cables for connections.)
4. On Autocal A8, set switch A8SW2 towards the front of DAV.
5. Set Autocal A8 switch A8SW1 for SIG A/D Converter Offset adjustment. Refer to table 3-12 for offset and gain adjustment switch settings.
6. Set Signal A/D Converter A12 switch A12SW1 toward the front of DAV.
7. Monitor main display and adjust A12R7 on Signal A/D Converter A12 for an exact reading of 0 (zero).
8. Set Signal A/D Converter A12 for SIG A/D Converter Gain adjustment (table 3-12).
9. On the Signal A/D Converter A12 set switch A12SW1 toward the rear of the DAV.
10. Monitor main display and adjust A12R9 on Signal A/D Converter for an exact reading of 20000.
11. Repeat steps 5 through 10 to obtain specified readings. (Note: These readings interact with one another and may change during adjustment.)
12. Set switch A8SW1 on Autocal A8 for REF A/D Converter Offset adjustment (table 3-12).
13. Set A9SW1 toward front of DAV on Reference A/D Converter A9.
14. Monitor main display and adjust A9R7 on Reference A/D Converter A9 for an exact reading of 0 (zero).
15. Set switch A8SW1 on Autocal A8 for REF A/D Converter Gain adjustment (table 3-12).
16. Set A9SW1 on Reference A/D Converter A9 toward rear of DAV.
17. Monitor main display and adjust A9R9 on Reference A/D Converter A9 for an exact reading of 20000.
18. Repeat steps 12 through 17 to obtain specified readings. (NOTE: These readings interact with one another and may change during adjustment.)
19. Set Reference A/D Converter A9 switch A9SW1 and Signal A/D Converter A12 switch A12SW1 toward rear of DAV.
20. On Autocal A8, remove cable from A8-J2 and set all A8SW1 switches OFF.
21. Turn DAV off and back on again.

Table 3-12. A/D Converter Offset and Gain Adjustment

Adjustment Procedure	Switch Setting			Main Display
	A8SW1-8	A8SW1-7	A8SW1-6	
None	OFF	ON	OFF	Normal
SIG A/D Converter Offset A12R7	ON	OFF	OFF	0
SIG A/D Converter Gain A12R9	ON	ON	OFF	20000
REF A/D Converter Offset A9R7	OFF	ON	OFF	0
REF A/D Converter Gain A9R9	OFF	OFF	ON	20000



NOTE: USE SHORTEST POSSIBLE COAXIAL CABLES RG-58U FOR ALL CONNECTIONS.

*Low Frequency Ratio Box is used for fine adjustments of input Signal Source. Omit ratio box if Signal Source can be adjusted to .75000 V rms.

Figure 3-17. A/D Converter A9/A12 Offset and Gain Adjustment, Test Setup Diagram

g. FRONT END A11/A14 OFFSET ALIGNMENT.

To align Front End A11/A14, proceed as follows:

1. Set up equipment as shown in figure 3-18.
2. Install shorting jumper between DAV SIG HI and SIG LO. Install another jumper between DAV REF HI and REF LO.
3. Set DAV to TOTAL (AVG) mode by setting all A8SW1 switches to OFF position. On DAV press TOTAL key followed by 20 mV range key.
4. On Signal Front End A14, connect DMM between test points A14TP3 (HI) and A14TP2 (LO).
5. Adjust A14R14 for a reading of less than 40 microvolts dc.
6. On Signal Front End A14, connect DMM between test points A14TP6 (HI) and A14TP10 (LO).
7. Adjust A14R10 for a reading of less than 12 mV dc.
8. On Reference Front End A11, connect DMM between test points A11TP3 (HI) and A11TP2 (LO).
9. Adjust A11R14 for a reading of less than 40 microvolts.
10. On Reference Front End A11, connect DMM between test points A11TP6 (HI) and A11TP10 (LO).
11. Adjust A11R10 for a reading of less than 12 millivolts dc.

h. A/D CONVERTER A9/A12 TOTAL(AVG) OFFSET ALIGNMENT.

To align A/D Converter A9/A12 TOTAL(AVG) offset, proceed as follows:

NOTE

The following steps are for A/D Converter A9/A12 assemblies NAI part no. 787664 revision E or higher.

1. Set DAV to TOTAL(AVG) mode by setting all A8SW1 switches to OFF position.
2. Press TOTAL key. Verify that AVG indicator is lit.
3. Connect shorting jumpers between inputs A12TP1 and A12TP2 on Signal A/D Converter A9 and between A9TP1 and A9TP2 on Reference A/D Converter A12.

NOTE

In the following steps, tap the TOTAL key while making adjustments. This eliminates the effects of display hysteresis.

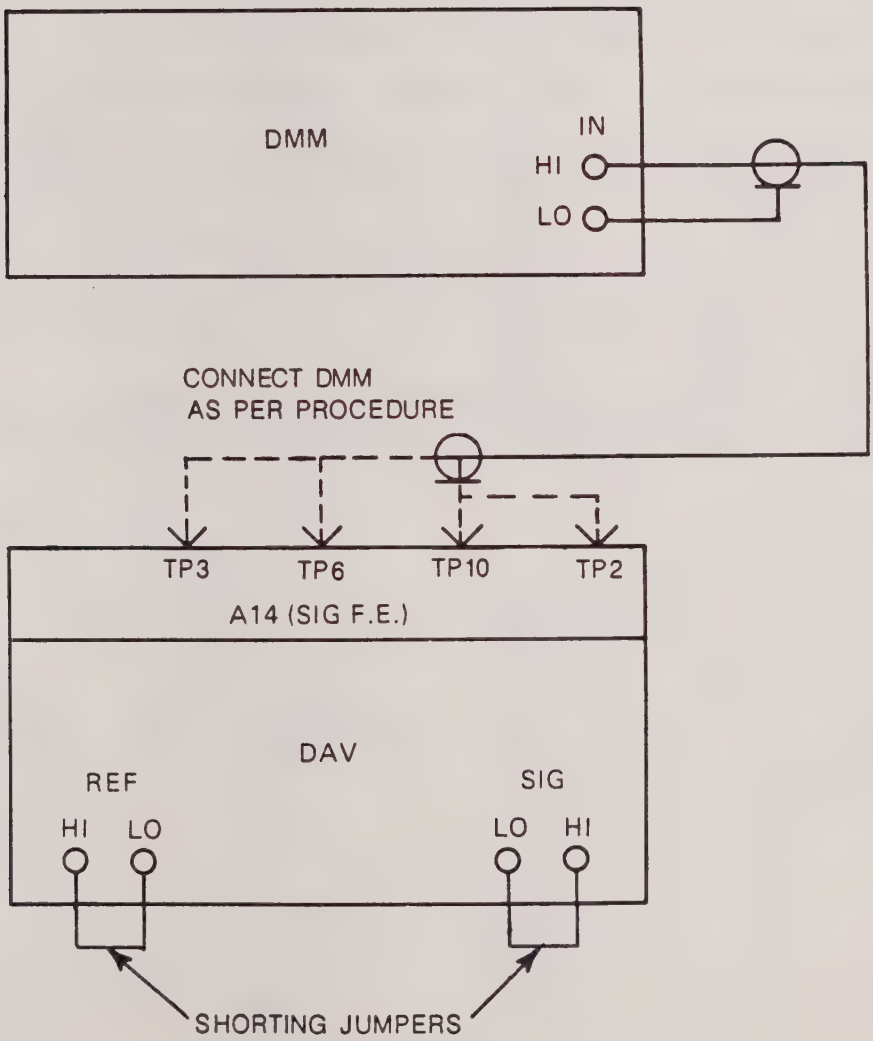


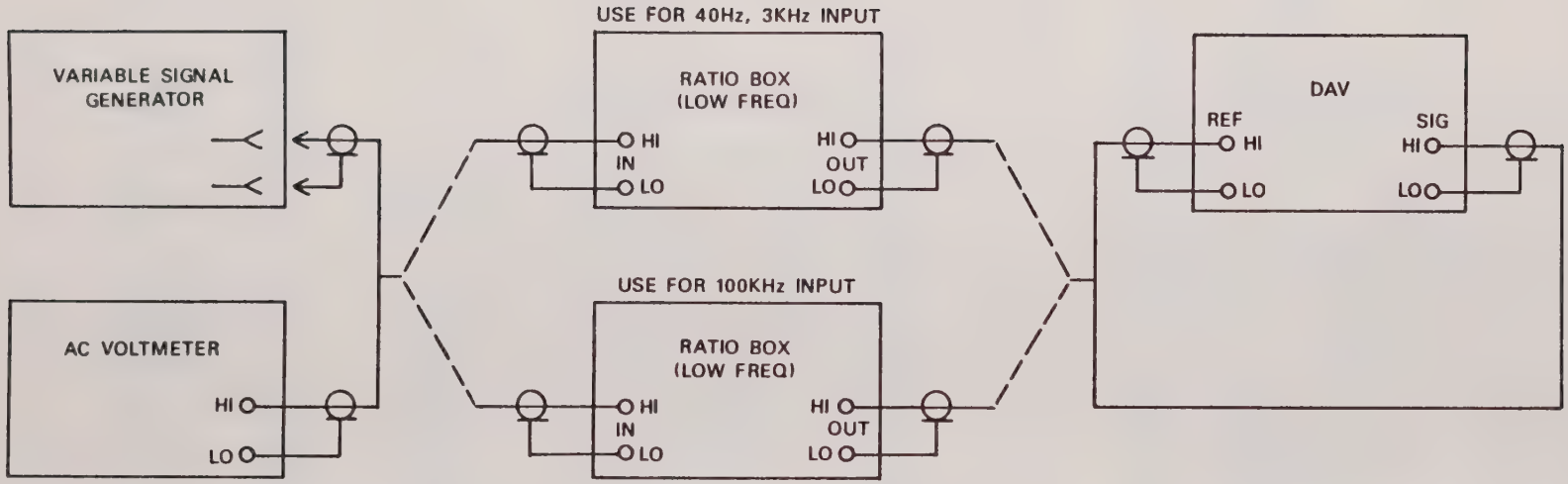
Figure 3-18. Front End A11/A14 Offset Adjustment, Test Setup Diagram

4. Set DAV for a SIG channel measurement (READ REF key LED not lit) and press the 20 mV range key.
5. On Signal A/D Converter A12, adjust A12R71 for a reading of 0.000 (zero) on DAV display.
6. Set DAV for a REF channel measurement (READ REF key LED lit) and 20 mV range.
7. On Reference A/D Converter A9, adjust A9R71 for a reading of 0.000 (zero) on the DAV display.
8. Remove jumpers from circuit cards A9 and A12.

i. FRONT END A11/A14 FREQUENCY RESPONSE ADJUSTMENT.

To adjust Front End A11/A14 frequency response, proceed as follows:

1. Set up equipment as shown in figures 3-19 or 3-20. (Figure 3-20 is an alternate test setup which incorporates an ac voltage calibrator, if available.)
2. Clear calibration correction factors from memory by setting DIP switch A8SW1-8 on Autocal board to ON position.
3. Wait two seconds and then set DIP switch A8SW1-8 to OFF position.
4. Turn DAV power off and then on. (All switches on A8SW1 should be in the OFF position.)
5. Connect variable signal source through Low Frequency Ratio Box (figure 3-19) or directly (figure 3-20) to DAV REF and SIG inputs.
6. Adjust variable signal source to 40 Hz, 9.000 $\pm$.001 V rms.



NOTE

Variable signal source remains set to 9 ±.001 V rms throughout adjustment procedure. Voltage input to DAV varies by setting Ratio Box as shown in table below.

Ratio Box Settings			DAV Input
Ratio	Frequency		
	High	Low	Voltage
1.000000	----	40 Hz	9 V
0.001000	----	40 Hz	9 mV
0.001000	100 kHz	----	9 mV
1.000000	----	3 kHz	9 V
1.000000	100 kHz		9 V

Figure 3-19. Front End A11/A14, (P/N 787505-1)
Frequency Response Adjustment, Test Setup Diagram

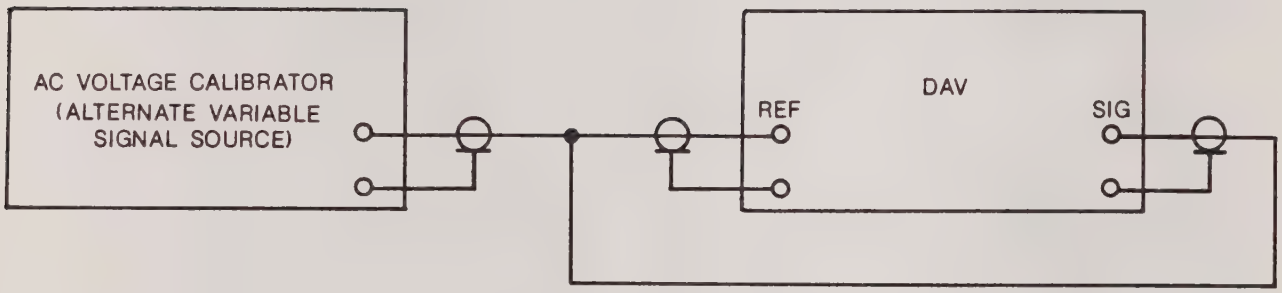


Figure 3-20. Front End A11/A14 (P/N 787505-1) Frequency Response Adjustment, Alternate Test Setup Diagram

7. Set DAV to TOTAL and AUTO RANGE. DAV display should indicate approximately 9 V rms.
8. Record DAV SIG TOTAL and REF TOTAL readings.
9. Adjust variable signal source to 9.000 ±.001 mV rms.
10. Record DAV SIG TOTAL and REF TOTAL readings. DAV display should indicate approximately 9 mV rms.
11. Adjust variable signal source to 100 kHz, 9.000 ±.001 mV rms. (Disconnect Low Frequency Ratio Box and connect High Frequency Ratio Box if figure 3-19 setup is used.)

NOTE

If C37 cannot be adjusted to the reading in the following steps, select-at-test capacitor C46 may need to be replaced. The value of C46 may vary within a range of 0-5 pf.

12. Set DAV for SIG channel measurement (READ REF key LED not lit) and adjust capacitor A14C37 on Signal Front End A14 to obtain the same reading as in step 10.
13. Set DAV for REF channel measurement and adjust capacitor A11C37 on Reference Front End A11 to obtain the same reading as in step 10.
14. Adjust variable signal source to 3.00 kHz, 9.000 ±.001 V rms. (Disconnect High Frequency Ratio Box and connect Low Frequency Ratio Box if figure 3-19 setup is used.)

15. Set DAV for SIG channel measurement (READ REF key LED not lit) and adjust capacitor A14C3 on Signal Front End A14 to obtain the same reading as in step 8.
16. Set DAV for REF channel measurement (READ REF key LED lit) and adjust capacitor A11C3 on Reference Front End A11 to obtain the same reading as in step 8.
17. Adjust variable signal source to 100 kHz, 9.000 ±.001 V rms. (Disconnect Low Frequency Ratio Box and connect High Frequency Ratio Box if figure 3-19 setup is used.)
18. Set DAV for SIG channel measurement (READ REF key LED not lit) and adjust resistor A14R41 on Signal Front End A14 to obtain the same reading as in step 8 ±.025 V.
19. Set DAV for REF channel measurement (READ REF key LED is lit) and adjust resistor A11R41 on Reference Front End A11 to obtain the same reading as in step 8 ±.025 V.
20. Repeat steps 14 through 19 until all readings are within specifications.
21. Recheck alignment readings per paragraph 3-4.f A/D Converter Offset and Gain Adjustment.

j. I/O A3 RECORDER OUTPUT ADJUSTMENT.

To adjust the I/O A3 recorder output, proceed as follows:

1. Set up equipment as shown in figure 3-21.
2. Verify that I/O A3 is set for 2 V full scale. (Install jumper blocks at locations A3W2 and A3W4 and disconnect jumpers from locations A3W1 and A3W3 as necessary.)
3. Set variable signal source for 400 Hz, 2.000 ±.001 V rms and connect to DAV REF and SIG inputs.
4. On DAV, press IN PHASE key. After DAV locks at input frequency, press CAL key.
5. After DAV completes autocalibration, set DAV for SIG channel measurement (READ REF LED not lit).
6. Disconnect input from DAV SIG input and connect a shorting jumper between SIG HI and SIG LO.
7. Using a DMM, monitor J5-A using J5-B as ground. (Recorder output pin connections are listed in table 3-13.)
8. On I/O A3, adjust A3R1 for 0 ±0.5 mV dc.
9. Using a DMM, monitor J5-C using J5-D as ground (see table 3-13).
10. On I/O A3, adjust A3A4 for 0 ±0.5 mV dc.

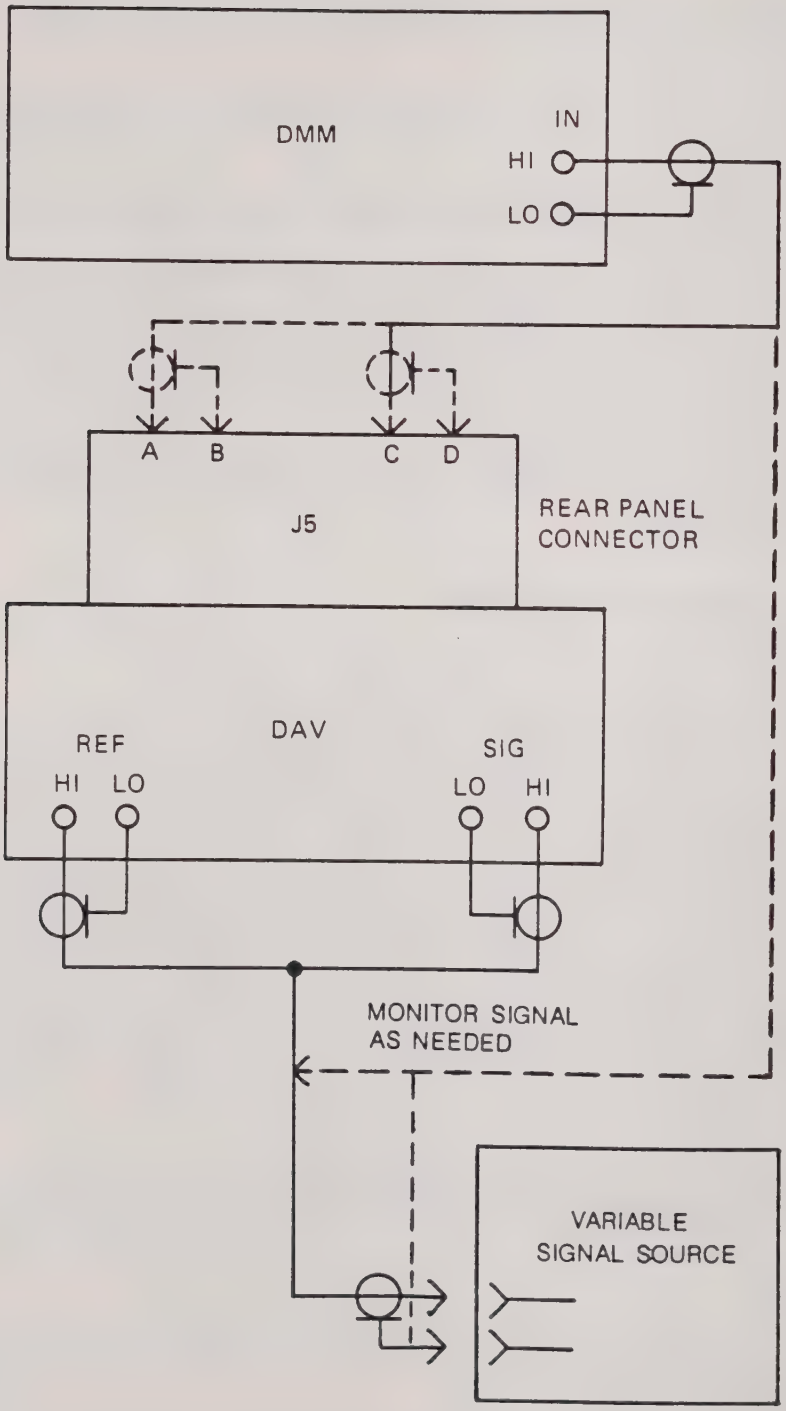


Figure 3-21. Recorder Output Adjustment, Test Setup Diagram

Table 3-13. Recorder Output Pin Connections

Signal Name	J5 Connection (Rear Panel)
INPHASE HI	A
INPHASE LO	B
QUAD HI	C
QUAD LO	D

11. Remove shorting jumper from DAV SIG input terminals and connect variable signal source. Readjust as necessary to 400 Hz, 2 ±0.001 V rms.
12. Press 2 V range key.
13. Adjust variable signal source for a DAV display reading of 2.0000 ±0.0001 V rms.
14. Using a DMM, monitor J5-A using J5-B as ground (see table 3-13).
15. On I/O A3, adjust A3R2 for 2 ±0.5 mV dc.
16. Using a DMM, monitor J5-C using J5-D as ground (see table 3-13.)
17. On I/O A3, adjust A3R3 for 2 ±0.5 mV dc.
18. On DAV, press CLEAR VAR key.

3-5. CALIBRATION.

Calibration of the DAV is accomplished by performing the complete alignment procedure provided in paragraph 3-4 and the High Voltage Test (paragraph 3-3.e), Wideband Accuracy Test (paragraph 3-3.f), and Phase Accuracy Test (paragraph 3-3.h). When calibrating, all test equipment used must be traceable to a National Bureau of Standards standard. Refer to table 1-6 for a list of test equipment required for calibration.

MODEL 2250

SECTION 4

TROUBLESHOOTING

4-1. INTRODUCTION

This section contains troubleshooting procedures for the DAV. A list of typical symptoms is contained in tables 4-1 through 4-5. The symptoms listed occur as a result of failures encountered during checkout tests, alignments, and during normal operation. Table 4-6 contains step by step procedures for locating a defective circuit card assembly or module. The functions of many of the circuit card assemblies are interdependent on others, thereby making troubleshooting difficult. The preferred technique for quick isolation of a defective circuit card assembly or module is to use a set of spare circuit cards to make trial replacements. However, if spare circuit cards are not readily available, isolation to the most likely defective circuit card assembly or module is facilitated by the procedures contained herein.

4-2. TROUBLESHOOTING PROCEDURE

When a failure is encountered during checkout tests, alignment, or during normal operation of the DAV, perform the steps in the following subparagraphs to isolate the faulty circuit assembly or module. During the troubleshooting process, refer to the detailed schematic and interconnection diagrams and to the parts location diagrams.

a. PRELIMINARY CHECKS

Turn off the DAV power switch and disconnect the DAV from the ac line. Remove circuit card assemblies (CAAs) A1, A10, and A13 (refer to section 5 for removal and replacement instructions). Connect the DAV to the ac line and turn on the power switch. Use a DMM with test probes to carefully probe the connectors on motherboard A16A1, and verify that the power supply voltages are as shown below. If any of these voltages do not appear as shown, refer to the symptom chart in table 4-1 for the recommended troubleshooting step(s). When complete, turn off the DAV power switch and disconnect the DAV from the ac line. Reinstall CCAs A1, A10, and A13.

SUPPLY	CONNECTOR	GROUND PIN	POWER SUPPLY	PIN SPECIFICATION
Main A17PS1	A16J2	50	49	+5.1 V ± 5%
Main A17PS1	A16J2	1	52	-15 V ± 5%
Main A17PS1	A16J2	1	3	+5 V ± 5%
Ref Isol A17PS2	A16J11	5	3	+15 V ± 5%
Ref Isol A17PS2	A16J11	5	4	-15 V ± 5%
Ref Isol A17PS2	A16J11	6	7	+5 V ± 5%
Sig Isol A17PS3	A16J14	5	3	+15 V ± 5%
Sig Isol A17PS3	A16J14	5	4	-15 V ± 5%
Sig Isol A17PS3	A16J14	6	7	+5 V ± 5%

b. DETERMINATION OF SYMPTOM

Examine the types of symptoms listed in tables 4-1 through 4-5 and determine which best describes the DAV failure encountered. The step number listed in the right hand column refers to a step in the troubleshooting procedure listed in table 4-6.

c. ISOLATION OF DEFECTIVE CIRCUIT CARD OR MODULE

Proceed to the step in table 4-6 which was referenced by a symptom in tables 4-1 through 4-5. Follow the procedure indicated to find the defective circuit card assembly or module.

d. REPAIR OF DEFECTIVE CIRCUIT CARD OR MODULE

Remove and replace the defective circuit card assembly or module (refer to Section 5). At the discretion of the maintenance technician, the defective circuit card assembly or module may be repaired using standard troubleshooting techniques and shop practices. Refer to Section 2, Theory of Operation for detailed theory, schematic diagrams, parts lists, and component locator information.

NOTE

In the procedures of table 4-6 it may sometimes be necessary to mount the circuit card assembly under evaluation on an extender card to gain access to the appropriate test points. In such cases, the DAV must be turned off, the extender card must be installed on to the appropriate circuit card assembly, and the troubleshooting procedure step (or several steps) must be repeated.

In the paragraphs which follow, "low frequency" refers to frequencies below 20 kHz; "low voltages" refer to voltages below 1 volt.

Table 4-1. Power Failures

POWER SUPPLY	SYMPTOM	TABLE 4-6 STEP
Main A17PS1	+5 V (digital) missing, incorrect value, or noisy.	16
Main A17PS1	+5 V (analog) missing, incorrect value, or noisy.	16
Main A17PS1	+15 V missing, incorrect value, or noisy.	16
Main A17PS1	-15 V missing, incorrect value, or noisy	16
Reference isolated A17PS2	+5 V missing, incorrect value, or noisy.	24
Reference isolated A17PS2	+15 V missing, incorrect value, or noisy.	24
Reference isolated A17PS2	-15 V missing, incorrect value, or noisy.	24
Signal isolated A17PS3	+5 V missing, incorrect value, or noisy.	20
Signal isolated A17PS3	+15 V missing, incorrect value, or noisy.	20
Signal isolated A17PS3	-15 V missing, incorrect value, or noisy.	20

Table 4-2. Checkout Test Failures

FAILED TEST	TABLE 4-6 STEP
1. Continuity check.	1
2. Ground isolation check.	6, 8 (SIG), 9 (REF)
3. Signal/reference isolation check.	10
4. Keyboard test.	50
5. Display test.	49
6. High voltage test.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
7. Wideband accuracy test	
a. Amplitude, low frequencies.	40, 28
b. Amplitude, high frequencies.	40, 28
c. Phase, low frequencies.	40, 28
d. Phase, high frequencies.	40, 28
8. Ratio accuracy test.	40, 28
9. 400 Hz phase accuracy test.	40, 28
10. Square wave phase sensitivity test.	40, 30, 31
11. Phase variables test.	120
12. Common mode rejection test.	1, 3, 10, 11, 12, 13, 14, 15
13. Total mode noise test.	40, 28
14. Total harmonic distortion test.	40, 28
15. Harmonic measurement test.	40, 28
16. Frequency measurement test.	40 (REF channel failure), 28
17. Lock time test.	29u
18. Calibration time test.	29
19. IEEE-488 interface test.	44
20. Recorder output test.	45, 46
21. Bargraph test.	49

Table 4-3. Alignment Failures

SYMPTOM	STEP
1. Fails prealignment test.	47
2. Autocal A8 Alignment	
a. Unable to enter step-by-step calibration mode.	41
b. Unable to obtain preliminary alignment output of approximately 13 V at 10 kHz.	40
c. Unable to adjust symmetry with A8R6.	121
d. Unable to adjust sinewave distortion with A8R8, R9.	121
e. Unable to adjust sinewave amplitude with A8R13.	40, 121
f. Unable to obtain proper autocal square wave at A8TP5.	122
g. Unable to obtain proper autocal outputs with input to A8J2 alignment signal connector.	123
3. Front End A11/A14 Alignment	
a. Unable to adjust TP3 offset using A11/A14 R10.	40, 29z, 29aa, 124, 125
b. Unable to adjust TP6 offset using A11/A14 R10.	40, 29z, 29aa, 124, 125
c. Unable to adjust frequency response using A11/A14 C3.	40, 126, 127
4. Phase Lock Loop A5 Alignment	
a. Unable to adjust A5TP6 VCO input voltage in upper four bands.	36, 128, 130
b. Unable to adjust A5TP6 VCO input voltage in lower four bands.	36, 129, 131
c. Excessive ripple at A5TP6 in upper four bands.	36, 128, 130
d. Excessive ripple at A5TP6 in lower four bands.	36, 129, 131
e. Unable to lock at one or more band end frequencies.	36, 130, 131
5. A/D Converter A9/A12 Alignment	
a. Unable to adjust conversion time with A9/A12 R37.	40, 132, 133
b. Unable to enter one or more alignment test modes.	41
c. Unable to adjust offset.	40, 134, 135
d. Unable to adjust gain.	40, 134, 135
6. I/O Board A3 Alignment	
a. Unable to adjust in phase recorder output.	45
b. Unable to adjust quadrature recorder output.	46

Table 4-4. Operational Failures

SYMPTOM	STEP
1. DAV will not complete power-up initialization and display checksum.	47
2. DAV will not complete autocalibration sequence.	29
3. DAV keyboard is unresponsive.	50
4. DAV display is unresponsive.	49, 36
5. IEEE-488 interface is unresponsive.	44
6. Inaccurate reading in TOTAL mode.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
7. Inaccurate reading in FUND mode.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
8. Inaccurate reading in INPH mode.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
9. Inaccurate reading in QUAD mode.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
10. Inaccurate reading in PHASE ANGLE mode.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
11. Inaccurate reading in THD mode.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
12. Inaccurate reading of harmonic amplitude.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
13. Inaccurate reading of harmonic phase.	40, 1, 3, 10, 11, 12, 13, 14, 15, 28
14. Displayed value is unstable.	40, 36, 28
15. Displayed value drifts.	40, 28, 36
16. High voltage reading drifts.	40, 136, 137, 28
17. DAV will not lock.	40, 36
18. DAV jumps out of lock.	40, 36
19. DAV will not indicate out-of-lock condition.	36
20. DAV displays incorrect frequency.	36

Table 4-4. Operational Failures (Continued)

SYMPTOM	STEP
21. DAV will not select proper range when autoranging is selected.	40, 108, 109
22. DAV will not indicate overload at the proper voltage levels.	40, 108, 109
23. One or more dim or inoperative front panel numeric displays.	49
24. One or more dim or inoperative front panel annunciator displays.	49
25. One or more dim or inoperative keyboard LEDs.	50
26. Incorrect annunciator display activated.	49
27. Incorrect numeric display activated.	49
28. Incorrect keyboard LED activated.	50
29. Inaccurate measurement of square wave phase angle.	40, 30, 31
30. Poor common mode rejection.	1, 3, 10, 11, 12, 13, 14, 15
31. Measurement beats near 60 Hz.	1, 3, 10, 11, 12, 13, 14, 15
32. DAV will not respond to test mode switches on autocal board A8.	41
33. DAV will not respond to 225 mode default setup switches.	42
34. DAV will not respond to IEEE-488 address switch.	43
35. DAV will not respond to trigger input.	51
36. Incorrect in phase recorder output.	45
37. Incorrect quadrature recorder output.	46
38. DAV will not accept IEEE-488 commands in native 2250 mode.	42, 44
39. DAV will not accept IEEE-488 commands in 225 compatible mode.	42, 44
40. Setup and calibration information not retained when power is removed.	48

Table 4-5. Calibration Step and Error Code Indication Failures

SYMPTOM	STEP
1. Calibration stops at CAL step 1 (CAL-1) and does not proceed.	29c
2. Calibration sequence is interrupted and main display reads Err 31.	29c
3. Calibration stops at CAL step 2 (CAL-2) and does not proceed.	29d
4. Calibration sequence is interrupted and main display reads Err 32.	29d
5. Calibration stops at CAL step 3 (CAL-3) and does not proceed.	29e
6. Calibration sequence is interrupted and main display reads Err 33.	29e
7. Calibration stops at CAL step 4 (CAL-4) and does not proceed.	29f
8. Calibration sequence is interrupted and main display reads Err 34.	29f
9. Calibration stops at CAL step 5 (CAL-5) and does not proceed.	29g
10. Calibration sequence is interrupted and main display reads Err 35.	29g
11. Calibration stops at CAL step 6 (CAL-6) and does not proceed.	29h
12. Calibration sequence is interrupted and main displa yreads Err 36.	29h
13. Calibration stops at CAL step 7 (CAL-7) and does not proceed.	29i
14. Calibration sequence is interrupted and main display reads Err 37.	29i
15. Calibration stops at CAL step 8 (CAL-8) and does not proceed.	29j
16. Calibration sequence is interrupted and main display reads Err 38.	29j
17. Calibration stops at CAL step 9 (CAL-9) and does not proceed.	29k
18. Calibration sequence is interrupted and main display reads Err 39.	29k
19. Calibration stops at CAL step 10 (CAL-10) and does not proceed.	29l
20. Calibration sequence is interrupted and main display reads Err 40.	29l
21. Calibration stops at CAL step 11 (CAL-11) and does not proceed.	29m
22. Calibration sequence is interrupted and main display reads Err 41.	29m
23. Calibration stops at CAL step 12 (CAL-12) and does not proceed.	29n

Table 4-5. Calibration Step and Error Code Indication Failures (Continued)

SYMPTOM	STEP
24. Calibration sequence is interrupted and main display reads Err 42.	29n
25. Calibration stops at CAL step 13 (CAL-13) and does not proceed.	29o
26. Calibration sequence is interrupted and main display reads Err 43.	29o
27. Calibration stops at CAL step 14 (CAL-14) and does not proceed.	29p
28. Calibration sequence is interrupted and main display reads Err 44.	29p
29. Calibration stops at CAL step 15 (CAL-15) and does not proceed.	29q
30. Calibration sequence is interrupted and main display reads Err 45.	29q
31. Calibration sequence is interrupted and main display reads Err 46.	29q
32. Calibration sequence is interrupted and main display reads Err 47.	29q
33. Calibration sequence is interrupted and main display reads Err 48.	29q
34. Calibration sequence is interrupted and main display reads Err 49.	29q
35. Calibration sequence is interrupted and main display reads Err 55.	29q, 29v
36. Calibration stops at CAL step 16 (CAL-16) and does not proceed.	29r
37. Calibration stops at CAL step 17 (CAL-17) and does not proceed.	29t
38. Calibration sequence is interrupted and main display reads Err 50.	29t
39. Calibration stops at CAL step 18 (CAL-18) and does not proceed.	29t

Table 4-6. DAV Troubleshooting Procedure

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
1	Turn on DAV. Remove protective cover from connector connected to A16A1J23 and use an ohmmeter to verify continuity as follows:		
	FROM / TO		
	a. A16A1P23-1 — Front Panel SIG HI	1b	52
	b. A16A1P23-1 — Rear Panel J1-A	1c	53
	c. A16A1P23-3 — Front Panel SIG LO	1d	52
	d. A16A1P23-3 — Rear Panel J1-B	1e	53
	e. A16A1P23-5 — Front Panel SIG GRD	1f	52
	f. A16A1P23-5 — Rear Panel J1-C	1g	53
	g. Front panel — Rear panel J1-D CASE ground	2	53
2	Turn on DAV. Remove protective cover from connector connected to A16A1J20 and use an ohmmeter to verify continuity as follows:		
	FROM / TO		
	a. A16A1P20-1 — Front Panel REF HI	2b	54
	b. A16A1P20-1 — Rear Panel J2-A	2c	55
	c. A16A1P20-3 — Front Panel REF LO	2d	54
	d. A16A1P20-3 — Rear Panel J2-B	2e	55
	e. A16A1P20-5 — Front Panel REF GRD	2f	54
	f. A16A1P20-5 — Rear Panel J2-C	2g	55
	g. Front panel — Rear Panel J2-D CASE ground	3	55
3	Turn off DAV and disconnect from ac line. Verify good mechanical and electrical connection to front panel CASE ground wire at both ends.	4	56
4	Turn off DAV and disconnect from ac line. Verify good mechanical and electrical connection to rear panel CHASSIS GND binding post.	5	57
5	Turn off DAV and disconnect from ac line. Verify good mechanical and electrical connection to rear panel chassis ground screw.	59	58

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
6	Turn off DAV and disconnect from ac line. Disconnect rear panel shorting link. Disconnect main power supply output connectors A17PS1P16, P17 from motherboard connectors A16A1J16, J17 and verify open circuit between rear panel CHASSIS GND and CIRCUIT GND binding posts.	60	7
7	Turn off DAV and disconnect from ac line. Disconnect main power supply output connector A17PS1P5 from display driver board connector A15A2J5 and verify open circuit between rear panel CHASSIS GND and CIRCUIT GND binding posts.	61	62
8	Turn on DAV. Disconnect front panel shorting links.		
	a. Disconnect signal channel input connector from A16A1J23 and verify open circuit between front panel SIG LO and SIG GRD.	8b	52
	b. Reconnect signal channel input connector to A16A1J23; remove A/D A12 and verify open circuit between front panel SIG LO and SIG GRD.	63	8c
	c. Remove filter A13 and verify open circuit between front panel SIG LO and SIG GRD.	64	8d
	d. Remove front end A14 and verify open circuit between front panel SIG LO and SIG GRD.	65	8e
	e. Reinstall front end A14 and disconnect isolated power supply connector from motherboard connector A16A1J21. Verify open circuit between front panel SIG LO and SIG GRD.	66	179
9	Turn on DAV. Disconnect front panel shorting links.		
	a. Disconnect reference channel input connector from A16A1J20 and verify open circuit between front panel REF LO and REF GRD.	9b	54
	b. Reconnect reference channel input connector to A16A1J20; remove A/D A9 and verify open circuit between front panel REF LO and REF GRD.	67	9c

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
9 (Cont.)	c. Remove filter A10 and verify open circuit between front panel REF LO and REF GRD.	68	9d
	d. Remove front end A11 and verify open circuit between front panel REF LO and REF GRD.	69	9e
	e. Reinstall front end A11 and disconnect isolated power supply connector from motherboard connector A16A1J18. Verify open circuit between front panel REF LO and REF GRD.	70	179
10	Turn off DAV and disconnect from ac line. Install front panel links. Install a jumper between front panel SIG HI and SIG LO. Install another jumper between front panel REF HI and REF LO.		
	a. Remove circuit card assemblies A9, A10, A11, A12, A13, and A14. Hipot at 300 V rms between SIG LO and REF LO and verify no leakage or breakdown indication.	8,9	10b
	b. Disconnect isolated power supply connectors from A16A1J18, J21. Hipot at 300 V rms between SIG LO and REF LO and verify no leakage or breakdown indication.	71	10c
	c. Disconnect signal and reference input connectors from motherboard A16A1J20, J23. Hipot at 300 V rms between SIG LO and REF LO and verify no leakage or breakdown.	72	10d
	d. Disconnect signal and reference rear input cables from isolation assemblies at A15A4J2 and A15A5J2. Hipot at 300 V rms between SIG LO and REF LO and verify no leakage or breakdown.	73	74
11	Turn on DAV. Remove front panel shorting links.		
	a. With an ohmmeter, verify continuity between front panel SIG GRD and signal front end A14 shield cover.	11c	11b
	b. Remove front end circuit card assembly A14. With an ohmmeter, verify continuity between front end A14 shield cover and front end A14 edge card connector P1-1, 51, 74.	13	75

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
11 (Cont.)	c. Be sure signal front end A14 is installed. With an ohmmeter, verify continuity between front panel SIG GRD and signal A/D A12 shield cover.	11e	11d
	d. Remove A/D circuit card assembly A12. With an ohmmeter, verify continuity between A/D A12 shield cover and A/D A12 edge connector P1-1, 51.	13	76
	e. With an ohmmeter, verify continuity between front panel SIG GRD and signal filter A13 shield cover.	11g	11f
	f. Remove filter circuit card assembly A13. With an ohmmeter, verify continuity between filter A13 shield cover and filter A13 edge connector P1-1, 51.	13	77
	g. With an ohmmeter, verify continuity between front panel SIG GRD and signal isolated power supply A17PS3 heatsink mounting screw.	177	11h
	h. Disconnect isolated power supply from motherboard connector A16A1J21. With an ohmmeter, verify continuity between power supply connector pin 1 (white wire) and heatsink mounting screw.	13	78
12	Turn on DAV. Remove front panel shorting links.		
	a. With an ohmmeter, verify continuity between front panel REF GRD and reference front end A11 shield cover.	12c	12b
	b. Remove front end circuit card assembly A11. With an ohmmeter, verify continuity between front end A11 shield cover and front end A11 edge card connector P1-1, 51, 74.	13	79
	c. Be sure reference front end A11 is installed. With an ohmmeter, verify continuity between front panel REF GRD and reference A/D A9 shield cover.	12e	12d
	d. Remove A/D circuit card assembly A9. With an ohmmeter, verify continuity between A/D A9 shield cover and A/D A9 edge connector P1-1, 51.	13	80

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
12 (Cont.)	e. With an ohmmeter, verify continuity between front panel REF GRD and reference filter A10 shield cover.	12g	12f
	f. Remove filter circuit card assembly A10. With an ohmmeter, verify continuity between filter A10 shield cover and filter A10 edge connector P1-1, 51.	13	81
	g. With an ohmmeter, verify continuity between front panel REF GRD and reference isolated power supply A17PS2 heatsink mounting screw.	177	12h
	h. Disconnect isolated power supply from motherboard connector A16A1J18. With an ohmmeter, verify continuity between power supply connector pin 1 (white wire) and heatsink mounting screw.	13	82
13	Turn off DAV and disconnect from ac line. Remove circuit card assemblies A9, A10, A11, A12, A13, and A14. With an ohmmeter, verify continuity between all of the following points: From A16A1J15-74 to A16A1J23-3 From A16A1J12-74 to A16A1J20-3		
	From A16A1J15-1 to A16A1J15-51, A16A1J14-1, -51, A16A1J13-1, -51. From A16A1J12-1 to A16A1J12-51, A16A1J11-1, -51, A16A1J10-1, -51.	1	83
14	Turn off DAV and disconnect from ac line. With an ohmmeter verify continuity between signal front end A14TP10 and screw head on small black shield.	177	75
15	Turn off DAV and disconnect from ac line. With an ohmmeter verify continuity between reference front end A11TP10 and screw head on small black shield.	177	79

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
	POWER SUPPLY CHECKS		
16	a. Disconnect main power supply cable from A16A1J17. With a DMM verify the following voltages on this connector (A17PS1P17):		
	GROUND PIN: 3, 4 — SUPPLY PIN: 1, 2 — VOLTAGE (+/- 5%): +5.1 V	16b	17
	b. Disconnect main power supply cable from A16A1J16. With a DMM verify the following voltages on this connector (A17PS1P16):		
	GROUND PIN: 1 — SUPPLY PIN: 2 — VOLTAGE (+/- 5%): +15 V GROUND PIN: 1 — SUPPLY PIN: 3 — VOLTAGE (+/- 5%): -15 V GROUND PIN: A17PS1P17-4 — SUPPLY PIN: A17PS1P16-4 — VOLTAGE (+/- 5%): +5 V	16c	17
	c. Disconnect main power supply cable from A15A2J5. With a DMM verify the following voltages on this connector (A17PS1P5):		
	GROUND PIN: 1 — SUPPLY PIN: 2 — VOLTAGE (+/- 5%): +5.1 V	83	17
17	Measure the following points on main power supply A17PS1 with a DMM:		
	GROUND PIN: GND. D — SUPPLY: +5 D — VOLTAGE (+/- 5%): +5.1 V GROUND PIN: GND. D — SUPPLY: +5 A — VOLTAGE (+/- 5%): +5 V GROUND PIN: GND. A — SUPPLY: +15 — VOLTAGE (+/- 5%): +15 V GROUND PIN: GND. A — SUPPLY: -15 — VOLTAGE (+/- 5%): -15 V	84	18
18	With a DMM verify the following voltages on A17PS1J1 (loaded):		
	LOW: 6 — HIGH: 3 — VOLTS AC (+/- 10%): 13.5 LOW: 6 — HIGH: 4 — VOLTS AC (+/- 10%): 13.5 LOW: 5 — HIGH: 1 — VOLTS AC (+/- 10%): 29 LOW: 5 — HIGH: 2 — VOLTS AC (+/- 10%): 29	85 86	19 19

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
19	Carefully measure main power supply transformer primary leads with a DMM. Verify voltages between points as follows: BLK to BLK/WHT 115 Vac BRN to BRN/WHT 115 Vac	87	88
20	Disconnect signal isolated power supply cable from motherboard connector A16A1J21. With a DMM verify the following voltages on this connector (A17PS3P21): GROUND PIN / SUPPLY PIN / VOLTAGE (+/- 5%) 4 / 2 / +15 V 4 / 3 / -15 V 5 / 6 / +5 V	83	21
21	Measure the following points on signal isolated supply A17PS3 with a DMM: GROUND / SUPPLY / VOLTAGE (+/- 5%) GND. D / +5 / +5 V GND. A / +15 / +15 V GND. A / -15 / -15 V	89	22
22	With a DMM verify the following voltages on A17PS3 (loaded): LOW / HIGH / VOLTS AC (+/- 10%) E2 / E1 / 13.4 E2 / E3 / 13.4 E5 / E4 / 30.5 E5 / E6 / 30.5	90 91	23 23
23	Carefully measure signal isolated power transformer primary leads with a DMM. Verify voltages between points as shown: BLK to BLK/WHT 115 Vac BRN to BRN/WHT 115 Vac	92	88

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
24	Disconnect reference isolated power supply A17PS2 cable from motherboard connector A16A1J18. With a DMM verify the following voltages on this connector (A17PS2P18): GROUND PIN / SUPPLY PIN / VOLTAGE (+/- 5%) 4 / 2 / +15 V 4 / 3 / -15 V 5 / 6 / +5 V	83	25
25	Measure the following points on reference isolated supply A17PS2 with a DMM: GROUND / SUPPLY / VOLTAGE (+/- 5%) GND D / +5 / +5 V GND A / +15 / +15 V GND A / -15 / -15 V	93	26
26	With a DMM verify the following voltages on A17PS2 (loaded): LOW / HIGH / VOLTS AC E2 / E1 / 13.4 E2 / E3 / 13.4 E5 / E4 / 30.5 E5 / E6 / 30.5	94 95	27 27
27	Carefully measure reference isolated power transformer primary leads with a DMM. Verify voltages between points as shown: BLK to BLK/WHT 115 Vac BRN to BRN/WHT 115 Vac	96	88
	CALIBRATION INTEGRITY CHECK		
28	Apply a signal source to the front panel signal and reference inputs and adjust to the amplitude and frequency where the error was encountered. Clear calibration factors at this frequency as follows: a. Set DIP switch A8SW1-8 to the closed position.		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
28 (Cont.)	b. Wait 5 seconds. c. Set DIP switch A8SW1-8 to the open position. d. Turn DAV off and back on again. Is the DAV reading now closer to the correct value?	29	32
29	Set the DAV to the SLO-CAL test mode by moving the actuator of autocal A8 test mode switch A8SW1-1 to the closed position. On the DAV front panel, press CAL key. Verify the conditions of DAV display readings, and monitor A/D A9 and A12 test points (TP2 is ground) and front end A11 and A14 test points (TP10 is ground) as outlined in steps 29a through 29aa. Probe test points momentarily only. Refer to figure 4-1 for a synopsis of the auto-calibration sequence and the mode control parameters imposed on the signal and reference channels. The frequency of the signal measured at these test points will be the same as the input frequency provided the input frequency is greater than 350 Hz. If the input frequency is less than 350 Hz, the frequency at these test points will be 350 Hz through step 29q. For steps 29r through 29t the frequency of the signal at these test points will be the same as the DAV input frequency. NOTE: For access to some of the test points indicated it may be necessary to use an extender card. a. DAV display reads CAL-, CF1-, CF2-, CF3-, or CF4-, and sequence does not proceed.	29v	29b
	b. DAV display momentarily reads CAL-L and then proceeds.	29c	29v

CAL STEP	ERR CODE	CONTROL SETTINGS				AUTOCAL AMPLITUDE	SECTION TESTED
		SIG F.E. (A14)	SIG A/D (A12)	REF F.E. (A11)	REF A/D (A9)		
L	30	BYPASS	D1	BYPASS	D1	-	AUTOCAL SQ WAVE PLL
1	31	BYPASS	D1	BYPASS	D1	.80V	REF. D1
2	32	BYPASS	D1	BYPASS	D2	.80V	REF. D2
3	33	BYPASS	D2	BYPASS	D1	.80V	SIG. D2
4	34	BYPASS	D2	BYPASS	D4	1.6V	REF. D4
5	35	BYPASS	D4	BYPASS	D2	1.6V	SIG. D4
6	36	BYPASS	D4	BYPASS	D8	3.2V	REF. D8
7	37	BYPASS	D8	BYPASS	D4	3.2V	SIG. D8
8	38	BYPASS	D8	20V	D2	4.6V	REF. 20V
9	39	20V	D2	BYPASS	D8	4.6V	SIG. 20V
10	40	BYPASS	D1	2V	D4	.80V	REF. 2V
11	41	2V	D4	BYPASS	D1	.80V	SIG. 2V
12	42	2V	D1	200mV	D8	.21V	REF. 200mV
13	43	200mV	D8	2V	D1	.21V	SIG. 200mV
14	44	200mV	D1	20mV	D8	.018V	REF. 20mV
15	45	20mV	D8	200mV	D1	.018V	SIG. 20mV
15	46	CALCULATED VALUE					REF. 200V
15	47	CALCULATED VALUE					SIG. 200V
15	48	CALCULATED VALUE					REF. 500V
15	49	CALCULATED VALUE					SIG. 500V
15	-	SET-UP FOR FILTER CAL					-
15	55	ACQUIRE LOCK FOR FILTER CAL					AUTOCAL, PLL, FILTER
16	-	2V	D4	2V	D4	.80V	FILTER OUT
17	50	2V	D4	2V	D4	.80V	FILTER IN
18	32	2V	*D4	2V	*D4	1.00V	TOTAL MODE RECTIFIER

*Total mode rectifier turned on.

Figure 4-1. Calibration Sequence and Signal/Reference Channel Mode Control Parameters

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	c. DAV main display reads a phase angle and harmonic display reads 1. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: TEST / TEST / BYPASS/D1 / BYPASS/D1		
	VERIFY: (1) A11TP1 reads 0.80 V rms	29c.2	29w
	(2) A14TP1 reads 0.80 V rms	29c.3	29w
	(3) A9TP1 reads 3.26 V rms	29c.4	29c.5
	(4) A12TP1 reads 3.26 V rms	29d	29c.7
	(5) Voltage at A9TP6 is 0.80 V rms.	29x	29c.6
	(6) Voltage at A9K1-8 is 0.80 V rms.	29x	29w
	(7) Voltage at A12TP6 is 0.80 V rms.	29y	29c.8
	(8) Voltage at A12K1-8 is 0.80 V rms.	29y	29w
	d. DAV main display reads a phase angle and harmonic display reads 2. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: TEST / TEST / BYPASS/D1 / BYPASS/D2		
	VERIFY: (1) A9TP1 reads 1.63 V rms	29d.2	29d.3
	(2) A12TP1 reads 3.26 V rms	29e	29d.5
	(3) Voltage at A9TP6 is 0.80 V rms.	29x	29d.4
	(4) Voltage at A9 K1-8 is 0.80 V rms.	29x	29w
	(5) Voltage at A12TP6 is 0.80 V rms.	29y	29d.6
	(6) Voltage at A12 K1-8 is 0.80 V rms.	29y	29w
	e. DAV main display reads a phase angle and harmonic display reads 3. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: TEST / TEST / BYPASS/D2 / BYPASS/D1		
	VERIFY: (1) A9TP1 reads 3.26 V rms	29e.2	29e.3
	(2) A12TP1 reads 1.63 V rms	29f	29e.5
	(3) Voltage at A9TP6 is 0.80 V rms.	29x	29e.4
	(4) Voltage at A9K1-8 is 0.80 V rms.	29x	29w
	(5) Voltage at A12TP6 is 0.80 V rms.	29y	29e.6
	(6) Voltage at A12K1-8 is 0.80 V rms.	29y	29w

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	f. DAV main display reads a phase angle and harmonic display reads 4. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: TEST / TEST / BYPASS/D2 / BYPASS/D4		
	VERIFY: (1) A9TP1 reads 1.63 V rms	29f.2	29f.3
	(2) A12TP1 reads 3.26 V rms	29g	29f.5
	(3) Voltage at A9TP6 is 1.60 V rms.	29x	29f.4
	(4) Voltage at A9K1-8 is 1.60 V rms.	29x	29w
	(5) Voltage at A12TP6 is 1.60 V rms.	29y	29f.6
	(6) Voltage at A12K1-8 is 1.60 V rms.	29y	29w
	g. DAV main display reads a phase angle and harmonic display reads 5. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: TEST / TEST / BYPASS/D4 / BYPASS/D2		
	VERIFY: (1) A9TP1 reads 3.26 V rms	29g.2	29g.3
	(2) A12TP1 reads 1.63 V rms	29h	29g.5
	(3) Voltage at A9TP6 is 1.60 V rms.	29x	29g.4
	(4) Voltage at A9K1-8 is 1.60 V rms.	29x	29w
	(5) Voltage at A12TP6 is 1.60 V rms.	29y	29g.6
	(6) Voltage at A12K1-8 is 1.60 V rms.	29y	29w
	h. DAV main display reads a phase angle and harmonic display reads 6. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: TEST / TEST / BYPASS/D4 / BYPASS/D8		
	VERIFY: (1) A9TP1 reads 1.63 V rms	29h.2	29h.3
	(2) A12TP1 reads 3.26 V rms	29i	29h.5
	(3) Voltage at A9TP6 is 3.20 V rms.	29x	29h.4
	(4) Voltage at A9K1-8 is 3.20 V rms.	29x	29w
	(5) Voltage at A12TP6 is 3.20 V rms.	29y	29h.6
	(6) Voltage at A12K1-8 is 3.20 V rms.	29y	29w

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	i. DAV main display reads a phase angle and harmonic display reads 7. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: TEST / TEST / BYPASS/D8 / BYPASS/D4		
	VERIFY: (1) A9TP1 reads 3.26 V rms	29i.1	29i.3
	(2) A12TP1 reads 1.63 V rms	29j	29i.5
	(3) Voltage at A9TP6 is 3.20 V rms	29x	29i.4
	(4) Voltage at A9K1-8 is 3.20 V rms	29x	29w
	(5) Voltage at A12TP6 is 3.20 V rms	29y	29i.6
	(6) Voltage at A12K1-8 is 3.20 V rms	29y	29w
	j. DAV main display reads a phase angle and harmonic display reads 8. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: TEST / 20 V / BYPASS/D8 / NORM/D2		
	VERIFY: (1) A11TP1 reads 4.60 V rms	29j.2	29w
	(2) A14TP1 reads 4.60 V rms	29j.3	29w
	(3) A11TP6 reads 1.38 V rms	29j.4	29aa
	(4) A14TP6 reads 0.00 V rms	29j.5	29z
	(5) A9TP1 reads 2.81 V rms	29j.6	29j.7
	(6) A12TP1 reads 2.34 V rms	29k	29j.9
	(7) Voltage at A9TP6 is 1.38 V rms	29x	29j.8
	(8) Voltage at A9K1-8 is 1.38 V rms	29x	29w
	(9) Voltage at A12TP6 is 4.60 V rms	29y	29j.10
	(10) Voltage at A12K1-8 is 4.60 V rms	29y	29w
	k. DAV main display reads a phase angle and harmonic display reads 9. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: 20 V / TEST / NORM/D2 / BYPASS/D8		
	VERIFY: (1) A11TP1 reads 4.60 V rms	29k.2	29w
	(2) A14TP1 reads 4.60 V rms	29k.3	29w
	(3) A11TP6 reads 0.00 V rms	29k.4	29aa

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	(4) A14TP6 reads 1.38 V rms	29k.5	29z
	(5) A9TP1 reads 2.34 V rms	29k.6	29k.7
	(6) A12TP1 reads 2.81 V rms	291	29k.9
	(7) Voltage at A9TP6 is 4.60 V rms	29x	29k.8
	(8) Voltage at A9K1-8 is 4.60 V rms	29x	29w
	(9) Voltage at A12TP6 is 1.38 V rms	29y	29k.10
	(10) Voltage at A12K1-8 is 1.38 V rms	29y	29w
	1. DAV main display reads a phase angle and harmonic display reads 10. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: TEST / 2 V / BYPASS/D1 / NORM/D4		
	VERIFY: (1) A11TP1 reads 0.80 V rms	291.2	29w
	(2) A14TP1 reads 0.80 V rms	291.3	29w
	(3) A11TP6 reads 2.40 V rms	291.4	29aa
	(4) A14TP6 reads 0.00 V rms	291.5	29z
	(5) A9TP1 reads 2.44 V rms	291.6	291.7
	(6) A12TP1 reads 3.26 V rms	29m	291.9
	(7) Voltage at A9TP6 is 2.40 V rms	29x	291.8
	(8) Voltage at A9K1-8 is 2.40 V rms	29x	29w
	(9) Voltage at A12TP6 is 0.80 V rms	29y	291.10
	(10) Voltage at A12K1-8 is 0.80 V rms	29y	29w
	m. DAV main display reads a phase angle and harmonic display reads 11. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: 2 V / TEST / NORM/D4 / BYPASS/D1		
	VERIFY: (1) A11TP1 reads 0.80 V rms	29m.2	29w
	(2) A14TP1 reads 0.80 V rms	29m.3	29w
	(3) A11TP6 reads 0.00 V rms	29m.4	29aa
	(4) A14TP6 reads 2.40 V rms	29m.5	29z
	(5) A9TP1 reads 3.26 V rms	29m.6	29m.7
	(6) A12TP1 reads 2.44 V rms	29n	29m.9
	(7) Voltage at A9TP6 is 0.80 V rms	29x	29m.8
	(8) Voltage at A9K1-8 is 0.80 V rms	29x	29w
	(9) Voltage at A12TP6 is 2.40 V rms	29y	29m.10
	(10) Voltage at A12K1-8 is 2.40 V rms	29y	29w

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	n. DAV main display reads a phase angle and harmonic display reads 12. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: 2 V / TEST / NORM/D1 / NORM/D8		
	VERIFY: (1) A11TP1 reads 0.21 V rms	29n.2	29w
	(2) A14TP1 reads 0.21 V rms	29n.3	29w
	(3) A11TP6 reads 6.30 V rms	29n.4	29aa
	(4) A14TP6 reads 0.63 V rms	29n.5	29z
	(5) A9TP1 reads 3.20 V rms	29n.6	29n.7
	(6) A12TP1 reads 2.56 V rms	29o	29n.9
	(7) Voltage at A9TP6 is 6.30 V rms	29x	29n.8
	(8) Voltage at A9K1-8 is 6.30 V rms	29x	29w
	(9) Voltage at A12TP6 is 0.63 V rms	29y	29n.10
	(10) Voltage at A12K1-8 is 0.63 V rms	29y	29w
	o. DAV main display reads a phase angle and harmonic display reads 13. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: 200 mV / 2 V / NORM/D8 / NORM/D1		
	VERIFY: (1) A11TP1 reads 0.21 V rms	29o.2	29w
	(2) A14TP1 reads 0.21 V rms	29o.3	29w
	(3) A11TP6 reads 0.63 V rms	29o.4	29aa
	(4) A14TP6 reads 0.63 V rms	29o.5	29z
	(5) A9TP1 reads 2.56 V rms	29o.6	29o.7
	(6) A12TP1 reads 3.20 V rms	29p	29o.9
	(7) Voltage at A9TP6 is 0.63 V rms	29x	29o.8
	(8) Voltage at A9K1-8 is 0.63 V rms	29x	29w
	(9) Voltage at A12TP6 is 6.30 V rms	29y	29o.10
	(10) Voltage at A12K1-8 is 6.30 V rms	29y	29w

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	p. DAV main display reads a phase angle and harmonic display reads 14. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: 200 mV / 20 mV / NORM/D1 / NORM/D8		
	VERIFY: (1) A11TP1 reads .018 V rms	29p.2	29w
	(2) A14TP1 reads .018 V rms	29p.3	29w
	(3) A11TP6 reads 5.40 V rms	29p.4	29aa
	(4) A14TP6 reads 0.54 V rms	29p.5	29z
	(5) A9TP1 reads 2.75 V rms	29p.6	29p.7
	(6) A12TP1 reads 2.20 V rms	29q	29p.9
	(7) Voltage at A9TP6 is 5.40 V rms	29x	29p.8
	(8) Voltage at A9K1-8 is 5.40 V rms	29x	29w
	(9) Voltage at A12TP6 is 0.54 V rms	29y	29p.10
	(10) Voltage at A12K1-8 is 0.54 V rms	29y	29w
	q. DAV main display reads a phase angle and harmonic display reads 15. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: 20 mV / 200 mV / NORM/D8 / NORM/D1		
	VERIFY: (1) A11TP1 reads .018 V rms	29q.2	29w
	(2) A14TP1 reads .018 V rms	29q.3	29w
	(3) A11TP6 reads 0.54 V rms	29q.4	29aa
	(4) A14TP6 reads 5.40 V rms	29q.5	29z
	(5) A9TP1 reads 2.20 V rms	29q.6	29q.7
	(6) A12TP1 reads 2.75 V rms	29r	29q.9
	(7) Voltage at A9TP6 is 0.54 V rms	29x	29q.8
	(8) Voltage at A9K1-8 is 0.54 V rms	29x	29w
	(9) Voltage at A12TP6 is 5.40 V rms	29y	29q.10
	(10) Voltage at A12K1-8 is 5.40 V rms	29y	29w

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	r. DAV main display reads a phase angle and harmonic display reads 16. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: 2 V / 2 V / NORM/D4 / NORM/D4		
	VERIFY: (1) A11TP1 reads 0.80 V rms	29r.2	29w
	(2) A14TP1 reads 0.80 V rms	29r.3	29w
	(3) A11TP6 reads 2.40 V rms	29r.4	29aa
	(4) A14TP6 reads 2.40 V rms	29r.5	29z
	(5) A9TP1 reads 2.44 V rms	29r.6	29r.9
	(6) A12TP1 reads 2.44 V rms	29r.7	29r.11
	(7) A11TP5 reads LOW (TTL)	29r.8	29aa
	(8) A14TP5 reads LOW (TTL)	29s	29z
	(9) Voltage at A9TP6 is 2.40 V rms	29x	29r.10
	(10) Voltage at A9K1-8 is 2.40 V rms	29x	29w
	(11) Voltage at A12TP6 is 2.40 V rms	29y	29r.12
	(12) Voltage at A12K1-8 is 2.40 V rms	29y	29w
	s. DAV main display reads a phase angle and harmonic display reads 17. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9		
	CAL MODE: 2 V / 2 V / NORM/D4 / NORM/D4		
	VERIFY: (1) A11TP1 reads 0.80 V rms	29s.2	29w
	(2) A14TP1 reads 0.80 V rms	29s.3	29w
	(3) A11TP6 reads 2.40 V rms	29s.4	29aa
	(4) A14TP6 reads 2.40 V rms	29s.5	29z
	(5) A9TP1 reads 2.44 V rms	29s.6	29s.9
	(6) A12TP1 reads 2.44 V rms	29s.7	29s.11
	(7) A11TP5 reads HIGH (TTL)	29s.8	29aa
	(8) A14TP5 reads HIGH (TTL)	29t	29z
	(9) Voltage at A9TP6 is 2.40 V rms	29x	29s.10
	(10) Voltage at A9K1-8 is 2.40 V rms	29x	29w
	(11) Voltage at A12TP6 is 2.40 V rms	29y	29s.12
	(12) Voltage at A12K1-8 is 2.40 V rms	29y	29w

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	t. DAV main display reads a phase angle and harmonic display reads 18. Verify the following calibration mode conditions:	29t.1	32
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: 2 V / 2 V / NORM/D4 / NORM/D4		
	VERIFY: (1) A11TP1 reads 1.00 V rms	29t.2	29w
	(2) A14TP1 reads 1.00 V rms	29t.3	29w
	(3) A11TP6 reads 3.00 V rms	29t.4	29aa
	(4) A14TP6 reads 3.00 V rms	29t.5	29z
	(5) A9TP1 reads 3.05 V rms	29t.6	29t.9
	(6) A12TP1 reads 3.05 V rms	29t.7	29t.11
	(7) A11TP5 reads HIGH (TTL)	29t.8	29aa
	(8) A14TP5 reads HIGH (TTL)	29u	29z
	(9) Voltage at A9TP6 is 3.00 V rms	29x	29t.10
	(10) Voltage at A9K1-8 is 3.00 V rms	29x	29w
	(11) Voltage at A12TP6 is 3.00 V rms	29y	29t.12
	(12) Voltage at A12K1-8 is 3.00 V rms	29y	29w
	u. DAV main display reads a phase angle and harmonic display reads 18 for several seconds only. Verify the following calibration mode conditions:		
	CCA: SIG F.E. A14 / REF F.E. A11 / SIG A/D A12 / REF A/D A9 CAL MODE: 2 V / 2 V / NORM/D4 / NORM/D4		
	VERIFY: (1) A11TP1 reads 1.00 V rms	29u.2	29w
	(2) A14TP1 reads 1.00 V rms	29u.3	29w
	(3) A11TP6 reads 3.00 V rms	29u.4	29aa
	(4) A14TP6 reads 3.00 V rms	29u.5	29z
	(5) A9TP2 reads 2.75 V dc	29u.6	29u.9
	(6) A12TP2 reads 2.75 V dc	29u.7	29u.11
	(7) A11TP5 reads HIGH (TTL)	29u.8	29aa
	(8) A14TP5 reads HIGH (TTL)	32	29z
	(9) Voltage at A9TP6 is 3.00 V rms	29x	29u.10
	(10) Voltage at A9K1-8 is 3.00 V rms	29x	29w
	(11) Voltage at A12TP6 is 3.00 V rms	29y	29u.12
	(12) Voltage at A12K1-8 is 3.00 V rms	29y	29w

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	v. Verify autocalibration phase lock function as follows:		
	(1) Connect an oscilloscope to A5TP3 (A5TP7 is ground). Verify a 15 V square wave, 50% duty cycle, at the present calibration frequency.	29v.2	29v.3
	(2) Connect an oscilloscope to A5TP5 (A5TP7 is ground). Verify a TTL low (this indicates a phase locked condition).	177	32
	(3) Connect an oscilloscope to A8TP5 (A8J2-2 is ground). Verify a TTL square wave at the present calibration frequency.	83	101
	w. Verify autocalibration signal output as follows:		
	(1) Connect DMM and oscilloscope to A8TP2 (A8J2-2 is ground). Verify correct test voltage of approximately 3.2 V rms at 10 kHz.	29w.2	102
	(2) Turn off the DAV and remove circuit card assemblies A9, A11, A12, and A14. With an ohmmeter, verify continuity from A8TP2 to all of the following points: A16A1J10-10,60 A16A1J12-10,60 A16A1J13-10,60 A16A1J15-10,60	29w.3	83
	(3) With an ohmmeter, verify continuity from A8-J2-2 to all of the following points: A16A1J10-11,61 A16A1J12-11,61 A16A1J13-11,61 A16A1J15-11,61 A16A1J24-3 A16A1J25-3	177	83

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	x. Apply power to DAV. Verify SIG A/D MSR/AC, BYPASS, and attenuator controls as follows:		
	(1) Use an oscilloscope to verify proper NORM/ BYPASS control conditions as indicated by calibration step where failure was encountered. Use A12TP2 as ground. (Reference steps 29c through 29t for control settings.)		
	MODE / MSR/AC A12U12-6 / BYPASS A12U12-7 NORM: TTL LOW / TTL LOW BYPASS: TTL LOW / TTL HIGH	29x.3	29x.2
	(2) Use an oscilloscope to verify proper NORM/ BYPASS control conditions as indicated by calibration step where failure was encountered. Use A12P1-50 as ground. (Reference steps 29c through 29t for control settings.)		
	MODE / MSR/AC A12U12-3 / BYPASS A12U12-2 NORM: TTL LOW / TTL LOW BYPASS: TTL LOW / TTL HIGH	97	103
	(3) Use an oscilloscope to verify proper inter-range control conditions as indicated by calibration step where failure was encountered. Use A12TP2 as ground. (Reference steps 29c through 29s for control settings.)		
	INTER-RANGE / DS1 A12U11-6 / DS0 A12U11-7 D1: TTL HIGH / TTL HIGH D2: TTL HIGH / TTL LOW D4: TTL LOW / TTL HIGH D8: TTL LOW / TTL LOW	97	29x.4

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	(4) Use an oscilloscope to verify proper inter-range control conditions as indicated by calibration step where failure was encountered. Use A12P1-50 as ground. (Reference steps 29c through 29t for control settings.)		
		97	103

INTER-RANGE	DS1 A12U11-3	DS0 A12U11-2
D1	TTL HIGH	TTL HIGH
D2	TTL HIGH	TTL LOW
D4	TTL LOW	TTL HIGH
D8	TTL LOW	TTL LOW

y. Verify REF A/D MSR/AC, BYPASS, and attenuator controls as follows:

(1) Use an oscilloscope to verify proper NORM/BYPASS control conditions as indicated by calibration step where failure was encountered. Use A9TP2 as ground. (Reference steps 29c through 29t for control settings.)

MODE	MSR/AC A9U12-6	BYPASS A9U12-7
NORM	TTL LOW	TTL LOW
BYPASS	TTL LOW	TTL HIGH

		29y.3	29y.2

(2) Use an oscilloscope to verify proper NORM/BYPASS control conditions as indicated by calibration step where failure was encountered. Use A9P1-50 as ground. (Reference steps 29c through 29t for control settings.)

MODE	MSR/AC A9U12-3	BYPASS A9U12-2
NORM	TTL LOW	TTL LOW
BYPASS	TTL LOW	TTL HIGH

		98	103

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	(3) Use an oscilloscope to verify proper inter-range control conditions as indicated by calibration step where failure was encountered. Use A9TP2 as ground. (Reference steps 29c through 29t for control settings.)		
	INTER-RANGE / DS1 A9U11-6 / DS0 A9U11-7 D1 / TTL HIGH / TTL HIGH D2 / TTL HIGH / TTL LOW D4 / TTL LOW / TTL HIGH D8 / TTL LOW / TTL LOW	98	29y.4
	(4) Use an oscilloscope to verify proper inter-range control conditions as indicated by calibration step where failure was encountered. Use A9P1-50 as ground. (Reference steps 29c through 29t for control settings.)		
	INTER-RANGE / DS1 A9U11-3 / DS0 A9U11-2 D1 / TTL HIGH / TTL HIGH D2 / TTL HIGH / TTL LOW D4 / TTL LOW / TTL HIGH D8 / TTL LOW / TTL LOW	98	103
	z. Verify SIG front end MSR/AC and attenuator controls as follows:		
	(1) Use an oscilloscope to verify proper MSR/AC control conditions as indicated by calibration step where failure was encountered. Use A14TP10 as ground. (Reference steps 29c through 29t for control settings.)		
	MSR/AC (A14U10-8) TTL HIGH	29z.3	29z.2

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)	(2) Use an oscilloscope to verify proper MSR/AC control conditions as indicated by calibration step where failure was encountered. Use A14P1-50 as ground. (Reference steps 29c through 29t for control settings.)		
	MSR/AC (A14U10-2) TTL LOW	99	103
	(3) Use an oscilloscope to verify proper range control conditions as indicated by calibration step where failure was encountered. Use A14TP10 as ground. These are TTL logic levels. (Reference steps 29c through 29t for control settings.)		
	RANGE / 1000/1 A14U8-6 / RS0 A14U9-6 / RS1 A14U9-7	30	29z.4
	20 mV HIGH HIGH HIGH		
	200 mV HIGH HIGH LOW		
	2 V HIGH LOW HIGH		
	20 V LOW HIGH HIGH		
	200 V LOW HIGH LOW		
	500 V LOW LOW HIGH		
	TEST X LOW LOW		
	(4) Use an oscilloscope to verify proper range control conditions as indicated by calibration step where failure was encountered. Use A14P1-50 as ground. These are TTL logic levels. (Reference steps 29c through 29t for control settings.)		
	RANGE / 1000/1 A14U8-3 / RS0 A14U9-3 / RS1 A14U9-2		
	20 mV HIGH HIGH HIGH		
	200 mV HIGH HIGH LOW		
	2 V HIGH LOW HIGH		
	20 V LOW HIGH HIGH		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)		99	103

RANGE	1000/1 A14U8-3	RS0 A14U9-3	RS1 A14U9-2
200 V	LOW	HIGH	LOW
500 V	LOW	LOW	HIGH
TEST	X	LOW	LOW

aa. Verify REF front end MSR/AC and attenuator controls as follows:

(1) Use an oscilloscope to verify proper MSR/AC control conditions as indicated by calibration step where failure was encountered. Use A11TP10 as ground. (Reference steps 29c through 29t for control settings.)

MSR/AC (A11U10-8)	TTL HIGH	29aa.3	29aa.2

(2) Use an oscilloscope to verify proper MSR/AC control conditions as indicated by calibration step where failure was encountered. Use A11P1-50 as ground. (Reference steps 29c through 29t for control settings.)

MSR/AC (A11U10-2)	TTL LOW	100	103

(3) Use an oscilloscope to verify proper range control conditions as indicated by calibration step where failure was encountered. Use A11TP10 as ground. These are TTL logic levels. (Reference steps 29c through 29t for control settings.)

RANGE	1000/1 A11U8-6	RS0 A11U9-6	RS1 A11U9-7
20 mV	HIGH	HIGH	HIGH
200 mV	HIGH	HIGH	LOW
2 V	HIGH	LOW	HIGH
20 V	LOW	HIGH	HIGH
200 V	LOW	HIGH	LOW

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
29 (Cont.)		31	29aa.4

RANGE	1000/1 A11U8-6	RS0 A11U9-6	RS1 A11U9-7
500 V	LOW	LOW	HIGH
TEST	X	LOW	LOW

(4) Use an oscilloscope to verify proper range control conditions as indicated by calibration step where failure was encountered. Use A11P1-50 as ground. These are TTL logic levels. (Reference steps 29c through 29t for control settings.)

RANGE	1000/1 A11U8-3	RS0 A11U9-3	RS1 A11U9-2
20 mV	HIGH	HIGH	HIGH
200 mV	HIGH	HIGH	LOW
2 V	HIGH	LOW	HIGH
20 V	LOW	HIGH	HIGH
200 V	LOW	HIGH	LOW
500 V	LOW	LOW	HIGH
TEST	X	LOW	LOW

		100	103
30	Determine the integrity of the signal front end and signal filter combination as follows:		
	a. Determine the integrity of the filter. Use a dual channel oscilloscope in the chop mode to compare signals at front end A14 test points TP8 and TP4. Verify that the signal at TP4 shows a phase lag of about 67 degrees and less high frequency noise. Use A14TP10 as ground.	30b	104
	b. Verify that the signals at front end A14 test points TP8 and TP4 have the same amplitude.	30c	104
	c. Determine if the filter should be in circuit at this time.		
	Is the DAV in the FUND, INPH, QUAD or PHASE ANGLE mode. . .	30d	30g
	OR		
	Is the DAV in autocalibration step 1 through 16?		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
30 (Cont.)	d. Determine if filter is in circuit. Use a dual channel oscilloscope in chop mode. Verify that the signal at front end A14 test point TP6 shows a phase lag of about 67 degrees and gain of about 17.3 relative to TP8. Use A14TP10 as ground.	99	30e
	e. Determine if filter switch controls are correct. Verify with an oscilloscope (ground is TP10) that TP5 is a TTL logic HIGH.	99	30f
	f. Determine if filter switch control input is correct. Verify with an oscilloscope (ground is P1-50) that U8-2 is a TTL logic HIGH.	99	112
	g. Determine if filter is in circuit. Use a dual channel oscilloscope in chop mode. Verify that the signal at front end A14 test point TP6 shows a phase lag of about 0 degrees and gain of about 17.3 relative to TP8. Use A14TP10 as ground.	99	30h
	h. Determine if filter switch controls are correct. Verify with an oscilloscope (ground is TP10) that TP5 is a TTL logic LOW.	99	30i
	i. Determine if filter switch control input is correct. Verify with an oscilloscope (ground is P1-50) that U8-2 is a TTL logic LOW.	99	112
31	Determine the integrity of the reference front end and reference filter combination as follows:		
	a. Determine the integrity of the filter. Use a dual channel oscilloscope in the chop mode to compare signals at front end A11 test points TP8 and TP4. Verify that the signal at TP4 shows a phase lag of about 67 degrees and less high frequency noise. Use A11TP10 as ground.	31b	105
	b. Verify that the signals at front end A11 test points TP8 and TP4 have the same amplitude.	31c	105
	c. Determine if the filter should be in circuit at this time.		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
31 (Cont.)	Is the DAV in the FUND, INPH, QUAD or PHASE ANGLE mode. . . OR Is the DAV in autocalibration step 1 through 16?	31d	31g
	d. Determine if filter is in circuit. Use a dual channel oscilloscope in chop mode. Verify that the signal at front end A11 test point TP6 shows a phase lag of about 67 degrees and gain of about 17.3 relative to TP8. Use A11TP10 as ground.	100	31e
	e. Determine if filter switch controls are correct. Verify with an oscilloscope (ground is TP10) that TP5 is a TTL logic HIGH.	100	31f
	f. Determine if filter switch control input is correct. Verify with an oscilloscope (ground is P1-50) that U8-2 is a TTL logic HIGH.	100	112
	g. Determine if filter is in circuit. Use a dual channel oscilloscope in chop mode. Verify that the signal at front end A11 test point TP6 shows a phase lag of about 0 degrees and gain of about 17.3 relative to TP8. Use A11TP10 as ground.	100	31h
	h. Determine if filter switch controls are correct. Verify with an oscilloscope (ground is TP10) that TP5 is a TTL logic LOW.	100	31i
	i. Determine if filter switch control input is correct. Verify with an oscilloscope (ground is P1-50) that U8-2 is a TTL logic LOW.	100	112
32	Turn off DAV and assure that the step-by-step autocalibration mode is turned off by setting the actuator of A8SW1-1 to the open position. Turn DAV on and connect a signal generator to the front panel SIG and REF inputs. Set the signal generator to the same frequency and amplitude where the original symptom was encountered.		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
32 (Cont.)	Determine whether failures are due to analog signal path or due to data acquisition circuits as follows:		
	a. Connect an oscilloscope to A9TP4 (A9TP5 is ground). Verify a TTL square wave, 50% duty cycle, with no apparent jitter.	32b	32c
	b. Connect a dual channel oscilloscope, chop mode, to A9U9-3 and A9U10-7 (A9TP2 is ground). Trigger the oscilloscope on the signal from A9TP4. Verify that the signal at A9U10-7 is a TTL pulse, low for 1.0 microsecond, synchronized with A9TP4 and with 64 samples over 1 to 28 cycles of the signal at A9TP4 (depending on frequency of input).	36	33
	c. Connect an oscilloscope to reference front end A11TP9 (A11TP10 is ground). Verify a sine-wave signal, at least 600 mV rms, with less than 10 mV of dc offset.	83	32d
	d. Connect an oscilloscope to reference front end A11TP1 (A11TP10 is ground). Verify the same amplitude and frequency as that applied to the front panel SIG and REF inputs.	33	36
	EVALUATE ANALOG SIGNAL PATH		
33	Turn DAV on and connect a signal generator to the front panel SIG and REF inputs. Set the signal generator to the same frequency and amplitude where the original symptom was encountered.		
	Determine integrity of isolation boards as follows:		
	a. Connect an oscilloscope to signal front end A14P1-66 (A14TP2 is ground). Verify that the signal at A14P1-66 is the same as the signal at the front panel input terminals and free from 60 Hz pickup.	33d	33b
	b. Connect an oscilloscope to signal isolation board A15A4P1-1 (A15A4P1-6 is ground). Verify a TTL HIGH level.	52	33c

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
33 (Cont.)	c. Turn off DAV and verify continuity on motherboard A16A1 between A16A1J24-1 and A16A1J7-28.	36	83
	d. Turn DAV back on and set up as before. Connect an oscilloscope to reference front end A11P1-66 (A11TP2 is ground). Verify that the signal at A11P1-66 is the same as the signal at the front panel input terminals and free from 60 Hz pickup.	34	33e
	e. Connect an oscilloscope to reference isolation board A15A5P1-1 (A15A5P1-6 is ground). Verify a TTL HIGH level.	54	33g
	f. Turn off DAV and verify continuity on motherboard A16A1 between A16A1J25-1 and A16A1J7-28.	36	83
34	Turn DAV on and connect a signal generator to the front panel SIG and REF inputs. Set the signal generator to the same frequency and amplitude where the original symptom was encountered.		
	a. To verify the integrity of the signal front end circuitry, connect an oscilloscope and DMM to signal front end A14TP1. Record the voltage measurement here (which must be equal to the front panel input voltage).		
	Connect the oscilloscope and DMM to signal front end A14TP6. Verify that this point has a signal free of excessive noise and distortion and that the gain relative to A14TP1 is correct for this range (see below). (A14TP10 is ground.)		
	RANGE / NOMINAL GAIN 20 mV / 300 200 mV / 30 2 V / 3 20 V / 0.3 200 V / 0.03 500 V / 0.003 TEST / 0	34b	29x

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
34 (Cont.)	b. Connect a dual channel oscilloscope to signal front end A14TP4 and A14TP8 (A14TP10 is ground) and set to chop mode. Use the front panel FUND and TOTAL mode keys to verify proper filter switching as shown by the approximate phase lag of the signal at TP4 relative to TP8. MODE — NOMINAL PHASE LAG FUND — 67 DEG. TOTAL — 0 DEG.	34c	30
	c. Connect a dual channel oscilloscope in chop mode to signal front end A14TP6 and A14TP9. Press the DAV TOTAL key. Use A14TP10 as ground. Verify that the signal at TP9 has the same amplitude as the signal at TP6, and has a phase lag of about 67 degrees.	34d	30
	d. Connect an oscilloscope to A14U11-7 (overload signal) and verify a TTL HIGH level. Use A14U11-8 as ground.	34e	108
	e. Adjust the DAV input voltage level equal to about 15% of the present voltage range. Connect an oscilloscope to A14U11-6 (don't-down-range signal) and verify a TTL LOW level. Use A14U11-8 as ground.	34f	108
	f. To verify the integrity of the reference front end circuitry, turn DAV on and connect a signal generator to the front panel SIG and REF inputs. Set the signal generator to the same frequency and amplitude where the original symptom was encountered. Connect an oscilloscope and DMM to the reference front end A11TP1. Record the voltage measurement here (which must be equal to the front panel input voltage). Connect the oscilloscope and DMM to reference front end A11TP6. Verify that this point has a signal free of excessive noise and distortion and that the gain relative to A11TP1 is correct for this range (see below). (A11TP10 is ground.)		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
34 (Cont.)	RANGE / NOMINAL GAIN 20 mV — 300 200 mV — 30 2 V — 3 20 V — 0.3 200 V — 0.03 500 V — 0.003 TEST — 0	34g	29y
	g. Connect a dual channel oscilloscope to signal front end A11TP4 and A11TP8 (A11TP10 is ground) and set to chop mode. Use the front panel FUND and TOTAL mode keys to verify proper filter switching as shown by the approximate phase lag of the signal at TP4 relative to TP8. MODE / NOMINAL PHASE LAG FUND — 67 DEG. TOTAL — 0 DEG.	34h	31
	h. Connect a dual channel oscilloscope in chop mode to signal front end A11TP6 and A11TP9. Press the DAV TOTAL key. Use A11TP10 as ground. Verify that the signal at TP9 has the same amplitude as the signal at TP6, and has a phase lag of about 67 degrees.	34i	31
	i. Connect an oscilloscope to A11U11-7 (overload signal) and verify a TTL HIGH level. Use A11U11-8 as ground.	34j	109
	j. Adjust the DAV input voltage level equal to about 15% of the present voltage range. Connect an oscilloscope to A11U11-6 (don't-down-range signal) and verify a TTL LOW level.	35	109
35	Turn DAV on and connect a signal generator to the front panel SIG and REF inputs. Set the signal generator to the same frequency and amplitude where the original symptom was encountered.		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
35 (Cont.)	a. To verify the integrity of the signal A/D circuitry, connect an oscilloscope to reference A/D A9TP6 (A9TP2 is ground); verify that this signal is the same as the reference front end output at A11TP6.	35c	35b
	b. Connect an oscilloscope to reference A/D A9K1-7 (A9TP2 is ground). Verify a signal the same as the reference output at A11TP6.	29y	112
	c. Connect a dual channel oscilloscope and DMM to reference A/D A9TP6 and A9TP1 (A9TP2 is ground). Verify gain is appropriate for the present inter-range as shown below: INTER-RANGE — NOMINAL GAIN D1 — 4.070 D2 — 2.035 D4 — 1.018 D8 — 0.509		
	NOTE Inter-range is always automatically selected by the DAV operating system software. The inter-range selection is based on a four step binary division of the major (front end) voltage range selected. For example, on the 20 V range, inter-range switch points would be 2.5 V (D1/D2), 5.0 V (D2/D4), and 10 V (D4/D8). These values are influenced by ranging hysteresis of about 20%.	35d	29y
	d. Connect an oscilloscope to reference A/D A9TP4 (A9TP5 is ground). Verify a TTL square wave, the same frequency as the DAV input, with no apparent jitter.	35f	35e
	e. Connect an oscilloscope to reference A/D A9TP12 (A9TP2 is ground). Verify a sinewave signal of same amplitude as signal at reference front end A11TP9.	111	112
	f. Connect an oscilloscope to reference A/D A9U10-7 (A9TP2 is ground). Verify the presence of TTL pulses, LOW for 1.0 microsecond.	35g	112

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
35 (Cont.)	g. Connect an oscilloscope to reference A/D A9U10-8 (A9TP2 is ground). Verify the presence of TTL pulses.	35h	112
	h. To verify the integrity of the signal A/D circuitry, connect an oscilloscope to signal A/D A12TP6 (A12TP2 is ground); verify that this signal is the same as the signal front end output at A14TP6.	35j	35i
	i. Connect an oscilloscope to signal A/D A12K1-7 (A9TP2 is ground). Verify a signal the same as the signal output at A14TP6.	29x	112
	j. Connect a dual channel oscilloscope and DMM to signal A/D A12TP6 and A12TP1 (A12TP2 is ground). Verify gain is appropriate for the present inter-range as shown below: INTER-RANGE — NOMINAL GAIN D1 — 4.070 D2 — 2.035 D4 — 1.018 D8 — 0.509		
	NOTE Inter-range is always automatically selected by the DAV operating system software. The inter-range selection is based on a four step binary division of the major (front end) voltage range selected. For example, on the 2 V range, inter-range switch points would be 2.5 V (D1/D2), 5.0 V (D2/D4), and 10 V (D4/D8). These values are influenced by ranging hysteresis of about 20%.	35k	29x
	k. Connect an oscilloscope to signal A/D A12U10-7 (A12TP2 is ground). Verify the presence of TTL pulses, LOW for 1.0 microsecond.	351	112
	l. Connect an oscilloscope to signal A/D A12U10-8 (A12TP2 is ground). Verify the presence of TTL pulses.	113	112

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
	EVALUATE DATA ACQUISITION CIRCUITS		
36	Evaluate phase lock function as follows:		
	a. Turn on DAV and connect a signal source to the SIG and REF front panel input terminals. Adjust the signal source to the same amplitude and frequency at which the original failure occurred. Wait for unit to initialize. Verify that the DAV front panel main display does not indicate NO LOC.	37	36b
	b. Connect an oscilloscope to phase locked loop board A5TP3 (A5TP7 is ground). Verify a 15 V logic square wave, 50% duty cycle, of same frequency as DAV input, and free of apparent phase jitter.	36c	36d
	c. Connect an oscilloscope to phase locked loop A5 to monitor frequency control inputs PLLFS0-2 (A5P1-23, 72, 22). Use A5TP7 as ground. With a dual channel scope, it may be necessary to make use of the trigger input to enable monitoring all 3 of these signals simultaneously. Verify that, at least momentarily, these controls assume a state correct for the band which includes the DAV input frequency as shown below (15 V logic).	118	116
	PLL BAND / FREQ RANGE / FS2 U21-4 / FS1 U21-7 / FS0 U21-9 7 10 Hz-32 Hz HIGH HIGH HIGH 6 32 Hz-100Hz HIGH HIGH LOW 5 100Hz-316Hz HIGH LOW HIGH 4 316Hz-1KHz HIGH LOW LOW 3 1kHz-3.16kHz LOW HIGH HIGH 2 3.16kHz-10.6kHz LOW HIGH LOW 1 10.6kHz-28.5kHz LOW LOW HIGH 0 28.5kHz-100kHz LOW LOW LOW		
	d. Connect an oscilloscope to phase-locked loop A5U10-5 (A5TP7 is ground). Verify a TTL square wave, of same frequency as DAV front panel input.	36e	119

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
36 (Cont.)	e. Connect an oscilloscope to phase locked loop A5U10-2 (BSIGSL) and A5U10-14 (BREFSL). A5TP7 is ground. Verify that these lines assume, at least momentarily, the conditions shown below. BSIGSL A5U10-2 TTL HIGH BREFSL A5U10-14 TTL LOW	118	116
37	Determine integrity of sample generation circuits as follows: a. Turn on DAV and connect a signal source to the SIG and REF front panel input terminals. Adjust the signal source to the same amplitude and frequency at which the original failure occurred. Wait for unit to initialize. Connect an oscilloscope to phase locked loop A5TP9 (A5TP7 is ground). Verify a 15 V logic square wave, frequency as shown below: DAV INPUT FREQUENCY — A5TP9 FREQUENCY 10 Hz-28.5 kHz — 64 X DAV INPUT 28.5 kHz-100 kHz — 16 X DAV INPUT	37c	37b
	b. Turn off DAV and use an ohmmeter to verify continuity between motherboard A16A1 connectors A16A1J6-12 and A16A1J5-12.	138	83
	c. Connect an oscilloscope to timing and control board A4TP1 (A4TP10 is ground). Verify a TTL pulse train, frequency as shown below (this signal is called SAMPLE): DAV INPUT FREQUENCY — A4TP1 FREQUENCY 10 Hz-3.16 kHz — 64.00 X DAV INPUT 3.16 kHz-10.6 kHz — 21.33 X DAV INPUT 10.6 kHz-28.5 kHz — 7.111 X DAV INPUT 28.5 kHz-100 kHz — 2.286 X DAV INPUT	37d	139
	d. Connect an oscilloscope to reference A/D A9U10-2 (A9TP5 is ground). Verify a TTL pulse, active low, 1 microsecond wide, and of same frequency as SAMPLE. This signal is called T/H.	37h	37e

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
37 (Cont.)	e. Connect an oscilloscope to microprocessor board A1TP5 (A1TP11 is ground). Verify a TTL square wave at a frequency of 8 MHz, 50% duty cycle.	37f	140
	f. Turn off the DAV and use an ohmmeter to verify continuity on motherboard A16A1 between J2-21, J1-27, J3-21, J4-21, J5-21. Turn DAV back on.	37g	83
	g. Connect an oscilloscope first to signal A/D A12TP10 (A12TP2 is ground) and then to reference A/D A9TP10 (A9TP2 is ground). Verify in each case that this point assumes a TTL LOW condition at least once within 1.1 milliseconds.	141	37h
	h. Connect an oscilloscope to reference A/D A9U10-8 (A9TP5 is ground). Verify a TTL low-to-high transition occurring at the same frequency as SAMPLE. This signal is called START.	37i	141
	i. Connect an oscilloscope first to signal A/D A12TP10 (A12TP2 is ground) and then to reference A/D A9TP10 (A9TP2 is ground). Verify in each case that this point assumes a TTL LOW condition at least once within 1.1 milliseconds.	38	142,143
38	If a failure is encountered in the signal channel, proceed as follows:	38a	39
	a. Connect an oscilloscope to signal accumulator A6TP2 and A6TP3 (A6TP14 is ground). Verify that TP2 has bursts of 12 TTL pulses at about 10 MHz. Also verify that TP3 has a serial data stream in the same time frame as the 12 TTL (clock) pulses.	38c	38b
	b. Turn off the DAV and use an ohmmeter to verify continuity between A16A1J13-39 and A16A1J7-34 (clock) and A16A1J13-40 and A16A1J7-84 (data). Turn DAV back on.	144	83

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
38 (Cont.)	c. Connect an oscilloscope to signal accumulator A6TP1 (A6TP14 is ground). Verify positive going TTL pulse, 125 nS in duration and with the same repetition rate as the clock and data streams.	38e	38d
	d. Turn off the DAV and use an ohmmeter to verify continuity between A16A1J5-7 and A16A1J7-7 (latch A/D). Turn DAV back on.	141	831
	e. Connect an oscilloscope to signal accumulator A6TP10 (A6TP14 is ground). Verify that there is not a continuous TTL LOW condition.	38f	146
	f. Connect an oscilloscope to timing and control board A4TP3 (A4TP10 is ground). Verify a TTL HIGH pulse with the same repetition rate as SAMPLE. This signal is called MEMREQ.	177	147
39	If a failure is encountered in the reference channel, proceed as follows:		
	a. Connect an oscilloscope to reference accumulator A7TP2 and A7TP3 (A7TP14 is ground). Verify that TP2 has bursts of 12 TTL pulses at about 10 MHz. Also verify that TP3 has a serial data stream in the same time frame as the 12 TTL (clock) pulses.	39c	39b
	b. Turn off the DAV and use an ohmmeter to verify continuity between A16A1J10-39 and A16A1J8-34 (clock) and A16A1J10-40 and A16A1J8-84 (data). Turn DAV back on.	145	83
	c. Connect an oscilloscope to reference accumulator A7TP1 (A7TP14 is ground). Verify positive going TTL pulse, 125 nS in duration and with the same repetition rate as the clock and data streams.	39e	39d
	d. Turn off the DAV and use an ohmmeter to verify continuity between A16A1J5-7 and A16A1J8-7 (latch A/D). Turn DAV back on.	141	83

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
39 (Cont.)	e. Connect an oscilloscope to reference accumulator A7TP10 (A7TP14 is ground). Verify that there is not a continuous TTL LOW condition.	39f	146
	f. Connect an oscilloscope to timing and control board A4TP3 (A4TP10 is ground). Verify a TTL HIGH pulse with the same repetition rate as SAMPLE. This signal is called MEMREQ.	177	147
40	To isolate a defective signal or reference section board proceed as follows:		
	a. Turn on the DAV and connect a signal source to the front panel SIG and REF input terminals. Adjust the signal source to the same frequency and amplitude where the original failure was encountered.		
	Verify that the failure is apparent in either the signal channel or the reference channel (use READ REF key), but not both. Make note of which channel shows the failure.	40b	177
	b. Turn off the DAV and exchange the positions of the signal and reference front end boards A14 and A11. Turn on the DAV and verify that the failure now appears in the other channel.	40c	40d
	c. Is the failure now in the signal channel?	148	149
	d. Turn off the DAV and exchange the positions of the signal and reference A/D boards A9 and A12. Turn on the DAV and verify that the failure now appears in the other channel.	40e	40f
	e. Is the failure now in the signal channel?	150	151
	f. Turn off the DAV and exchange the positions of the signal and reference filter boards A10 and A13. Turn on the DAV and verify that the failure now appears in the other channel.	40g	40h
	g. Is the failure now in the signal channel?	152	153

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
40 (Cont.)	h. Turn off the DAV and exchange the positions of the signal and reference accumulator boards A6 and A7. Turn on the DAV and verify that the failure now appears in the other channel.	40i	177
	i. Is the failure now in the signal channel?	154	155
41	Verify operation of autocal A8 test mode switches as follows:		
	a. Use an oscilloscope to monitor the test mode switch buffer inputs at A8U10-2, 17, 4, 15, 6, 13, 8, 11. Operate the actuators of each section of DIP switch A8SW1 and verify that the corresponding buffer input follows the switch. Use A8U10-10 as ground.	41b	156
	b. Use an oscilloscope to monitor data bus lines D8 through D15 on the outputs of buffer A8U10-18, 3, 16, 5, 14, 7, 12, 9. Verify that these outputs assume the correct state when A8U10-1 (ACLSTAT) is low. (State outputs are the same as A8SW1 inputs.)	41c	156
	c. Use an ohmmeter to verify continuity of each data bus line (D8 through D15) to microprocessor A1 connector P1 pins 45, 95, 46, 96, 47, 97, 48, 98, respectively.	156	83
42	Verify operation of IEEE-488 mode and 225 emulation device clear switches as follows:		
	a. Use an oscilloscope to monitor inputs to A3SW1 latch at A3U8-18, 17, 14, 13, 8, 7, 4, 3. Operate the actuators of A3SW1 and verify that the corresponding latch input follows the switch.	42b	157
	b. Use an oscilloscope to monitor inputs to A3SW2 latch at A3U11-18, 17, 14, 13, 8, 7, 4, 3. Operate the actuators of A3SW2 and verify that the corresponding latch input follows the switch.	42c	157

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
	c. Use an oscilloscope to monitor outputs of A3SW1 latch at A3U8-19, 16, 15, 12, 9, 6, 5, 2. Verify that each output assumes a level equal to that at the corresponding input at the time when enable input at A3U8-1 is low.	42d	157
	d. Use an oscilloscope to monitor outputs of A3SW2 latch at A3U11-19, 16, 15, 12, 9, 6, 5, 2. Verify that each output assumes a level equal to that at the corresponding input at the time when enable input at A3U11-1 is low.	42e	157
	e. Use an ohmmeter to verify continuity to the microprocessor board A1 for each of the data bus lines D0 through D7 (A1 connector P1 pins 41, 91, 42, 92, 43, 93, 44, 94).	177	83
43	Verify operation of IEEE-488 address switch as follows:		
	a. Use an oscilloscope to monitor inputs to A3 address latch at A3U7-18, 17, 14, 13, 8, 7, 4, 3. Operate the actuators of rear panel IEEE-488 address switch and verify that the corresponding latch input follows the switch.	43b	158
	b. Use an oscilloscope to monitor outputs of A3 address latch at A3U7-19, 16, 15, 12, 9, 6, 5, 2. Verify that each output assumes a level equal to that at the corresponding input at the time when enable input at A3U7-1 is low.	43c	157
	c. Use an ohmmeter to verify continuity to the microprocessor board A1 for each of the data bus lines D0 through D7 (A1 connector P1 pins 41, 91, 42, 92, 43, 93, 44, 94).	177	83
44	Verify operation of IEEE-488 interface as follows:		
	Connect an IEEE-488 controller to the DAV IEEE-488 port. Request a serial poll and verify that the DAV transmits the serial poll byte.	159	43

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
45	Verify operation of inphase recorder output as follows:		
	Connect an oscilloscope to I/O board A3TP5 (A3TP12 is ground). Verify that the output dc voltage is correct for the present front panel in phase reading and that the output is stable and free of excessive noise.	158	160
46	Verify operation of quadrature recorder output as follows:		
	Connect an oscilloscope to I/O board A3TP6 (A3TP12 is ground). Verify that the output dc voltage is correct for the present front panel quadrature reading and that the output is stable and free of excessive noise.	158	160
47	Determine the cause of DAV initialization failure as follows:		
	a. Connect an oscilloscope to microprocessor A1TP5 (A1TP11 is ground). Verify a TTL square wave at 8 MHz, 50% duty cycle.	47h	47b
	b. Turn off the DAV and use an ohmmeter to verify no continuity between A1TP5 (8 MHz) and A1TP2 (ground) and no continuity between A1TP5 (8 MHz) and A4TP9 (+5 V).	140	47c
	c. Remove memory board A2 and use an ohmmeter to verify no continuity between A1TP5 (8 MHz) and A1TP2 (ground), and no continuity between A1TP5 (8 MHz) and A4TP9 (+5 V).	47d	161
	d. Remove I/O board A3 and use an ohmmeter to verify no continuity between A1TP5 (8 MHz) and A1TP2 (ground) and no continuity between A1TP5 (8 MHz) and A4TP9 (+5 V).	47e	162

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
47 (Cont.)	e. Remove timing and control board A4 and use an ohmmeter to verify no continuity between A1TP5 (8 MHz) and A1TP2 (ground) and no continuity between A1TP5 (8 MHz) and motherboard connector A16A1J5-49 (+5 V).	47f	163
	f. Disconnect ribbon cable from display driver board at A15A2J3 and use an ohmmeter to verify no continuity between A1TP5 and A1TP2, and no continuity between A1TP5 and motherboard connector A16A1J5-49.	47h	164
	g. Remove mirocprocessor A1 and use an ohmmeter to verify no continuity between motherboard A16A1J2-21 and A16A1J2-50, and no continuity between A16A1J2-21 and A16A1J2-49.	140	179
	h. Reinstall all boards, connect ribbon cable and turn on DAV. Use an oscilloscope to monitor each of the microprocessor data bus lines A1P1-41, 91, 42, 92, 43, 93, 44, 94, 45, 95, 46, 96, 47, 97, 48, 98, respectively, and verify that no line is stuck in the high or low state.	47i	165
	i. Use an oscilloscope to monitor each of the microprocessor address bus lines AB1-23 at A1P1-79, 30, 80, 31, 81, 32, 82, 33, 83, 34, 84, 35, 85, 36, 86, 37, 87, 38, 88, 39, 89, 40, 90, respectively, and verify that no line is stuck in the high or low state.	47j	165
	j. Install all circuit cards back into the DAV and turn the DAV on. Connect an oscilloscope to memory board A2TP5 (BERR) (A1TP11 is ground) and verify a TTL HIGH level.	165	166
48	Verify operation of memory board A2 as follows:		
	a. Turn DAV on and verify that checksum which appears corresponds to one of those listed in table 1-1.	48b	167
	b. Connect a signal to the DAV front panel REF input terminals. When the DAV initializes and locks, press CAL. When the autocalibration sequence is completed, observe that the LED on the CAL key is not lit. Turn off the DAV for one minute and turn it back on. Verify that the CAL LED is not lit.	177	167

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
49	Determine cause of display failures as follows:		
	a. Is failure confined to a single display segment or section of one display?	168	49b
	b. Observe the displays or sections which exhibit the failure. Refer to the display driver schematic (figure 7-13) and determine which display driver outputs control those displays. Use an ohmmeter to verify continuity from the display driver board to the display board for these lines.	169	170
50	Determine cause of keyboard failures as follows:		
	a. Is there a failure of one or more of the keyboard keys?	50d	50b
	b. Is there a failure of only one keyboard LED?	171	50c
	c. Observe which LEDs exhibit failure and refer to the display driver schematic (figure 7-13) to determine which lines control these LEDs. Use an ohmmeter to verify continuity between the display driver board and the keyboard for these lines.	173	170
	d. Are all key failures in the same column or in the same row?	50e	50f
	e. Refer to the display driver schematic (figure 7-13) and determine which lines control the row or column which fails. Use an ohmmeter to verify continuity in the cable between the keyboard and the display driver A15A1J1 to A15A2J4) for these lines.	172	173
	f. Do any of the keyboard keys work?	174	172
51	Determine cause of trigger input failure as follows:		
	a. Connect an oscilloscope to A3TP1 (A3TP9 is ground). With a jumper, momentarily short the rear panel trigger input to ground and verify that TP1 assumes a TTL LOW state.	51b	175
	b. Use an ohmmeter to verify continuity on motherboard A16A1 from J4-24 to J2-24.	176	175

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
52	Replace or repair signal channel isolation board A15A4.		
53	Replace or repair signal rear input cable.		
54	Replace or repair reference channel isolation board A15A5.		
55	Replace or repair reference rear input cable.		
56	Replace or repair front panel chassis ground wire.		
57	Replace or repair wires to rear panel chassis ground binding post.		
58	Replace or repair wires to rear panel chassis ground screw.		
59	Replace or repair main harness A17W1.		
60	Repair short to chassis at motherboard A16A1.		
61	Repair short to chassis at front bezel assembly A15.		
62	Replace or repair main power supply A17PS1 (short to chassis).		
63	Replace or repair signal A/D board A12 (short between guard and ground).		
64	Replace signal filter A13 (short between guard and ground).		
65	Replace or repair signal front end A14 (short between guard to ground).		
66	Replace or repair signal isolated power supply A17PS3 (short between guard and ground).		
67	Replace or repair reference A/D board A9 (short between guard and ground).	178	
68	Replace reference filter A10 (short between guard and ground).		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
69	Replace or repair reference front end A11 (short between guard and ground).	178	
70	Replace or repair reference isolated power supply A17PS2 (short between guard and ground).		
71	Replace or repair both isolated power supplies (A17PS2, A17PS3) (isolation breakdown).		
72	Replace or repair motherboard A16A1 (isolation breakdown).		
73	Replace or repair signal rear panel input cable and reference rear panel input cable (isolation breakdown).		
74	Replace or repair signal isolation board A15A4 and reference isolation board A15A5 (isolation breakdown).		
75	Replace or repair signal front end A14 (defective shields).	178	
76	Replace or repair signal A/D A12 (defective shields).	178	
77	Replace signal filter A13 (defective shields).		
78	Replace or repair signal isolated power supply A17PS3 (defective shields).		
79	Replace or repair reference front end A11 (defective shields).	178	
80	Replace or repair reference A/D A9 (defective shields).	178	
81	Replace reference filter A10 (defective shields).		
82	Replace or repair reference isolated power supply A17PS2 (defective shields).		
83	Replace or repair motherboard A16A1 (open traces).		
84	Replace or repair main power supply A17PS1 (defective output cable).		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
85	Replace or repair main power supply A17PS1 (defective logic supply).		
86	Replace or repair main power supply A17PS1 (defective analog supply).		
87	Replace main power transformer A17T1.		
88	Replace main harness A17W1.		
89	Replace or repair signal isolated power supply A17PS3 (defective cable).		
90	Replace or repair signal isolated power supply A17PS3 (defective logic supply).		
91	Replace or repair signal isolated power supply A17PS3 (defective analog supply).		
92	Replace or repair signal isolated power supply A17PS3 (defective transformer).		
93	Replace or repair reference isolated power supply A17PS2 (defective cable).		
94	Replace or repair reference isolated power supply A17PS2 (defective logic supply).		
95	Replace or repair reference isolated power supply A17PS2 (defective analog supply).		
96	Replace or repair reference isolated power supply A17PS2 (defective transformer).		
97	Replace or repair signal A/D A12 (defective amplifier/attenuator circuits).	178	
98	Replace or repair reference A/D A9 (defective amplifier/attenuator circuits).	178	
99	Replace or repair signal front end A14 (defective amplifier/attenuator circuits).	178	
100	Replace or repair reference front end A11 (defective amplifier/attenuator circuits).	178	
101	Replace or repair autocal board A8 (defective square wave output circuit).	178	

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
102	Replace or repair autocal board A8 (defective calibration signal output circuit).	178	
103	Verify continuity of printed circuit traces on motherboard A16A1 as referenced by previous step.	32	83
104	Replace signal filter A13.		
105	Replace reference filter A10.		
106	Replace or repair signal front end A14 (defective filter controls).	178	
107	Replace or repair reference front end A11 (defective filter controls).	178	
108	Replace or repair signal front end A14 (defective overload/range-limit circuits).	178	
109	Replace or repair reference front end A11 (defective overload/range-limit circuits).	178	
110	Replace or repair signal A/D A12 (defective zero crossing detector circuits).	178	
111	Replace or repair reference A/D A9 (defective zero crossing detector circuits).	178	
112	Verify continuity of printed circuit traces on motherboard A16A1 as referenced by previous step.	36	83
113	Perform alignments for A/D boards A9 and A12, and front end boards A11 and A14.		
114	With an ohmmeter, verify continuity on motherboard A16A1 to points connected to A16A1J8 pins 2, 5, 6, 9, 12, 15, 16, 19.	115	83
115	Replace or repair reference accumulator A7 (defective front end-A/D control circuits).		
116	With an ohmmeter, verify continuity on motherboard A16A1 to points connected to A16A1J6 pins 24, 74, 22, 72, 23, 18, 27, 32 and 82.	117	83
117	Replace or repair timing and control board A4 (defective control port circuits).		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
118	Replace or repair phase locked loop A5 (defective lock or lock detection circuits).	178	
119	With an ohmmeter, verify continuity on motherboard A16A1 to the points referenced in the previous step.	177	83
120	Replace or repair memory board A2 (faulty PROMs).		
121	Replace or repair autocal board A8 (cannot adjust distortion, amplitude, or symmetry).	178	
122	Replace or repair autocal board A8 (defective square wave output circuits).	178	
123	Replace or repair autocal board A8 (defective external test signal input circuits).	178	
124	Replace or repair signal front end A14 (cannot adjust dc offsets).	178	
125	Replace or repair reference front end A11 (cannot adjust dc offsets).	178	
126	Replace or repair signal front end A14 (cannot adjust attenuator frequency response).	178	
127	Replace or repair reference front end A11 (cannot adjust attenuator frequency response).	178	
128	Replace or repair phase locked loop board A5 (defective VCO circuits for upper 4 bands).	178	
129	Replace or repair phase locked loop board A5 (defective VCO circuits for lower 4 bands).	178	
130	Replace or repair phase locked loop board A5 (defective filter circuits for upper 4 bands).	178	
131	Replace or repair phase locked loop board A5 (defective filter circuits for lower 4 bands).	178	
132	Replace or repair signal A/D A12 (cannot adjust conversion rate).	178	
133	Replace or repair reference A/D A9 (cannot adjust conversion rate).	178	

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
134	Replace or repair signal A/D A12 (cannot adjust offset or gain).	178	
135	Replace or repair reference A/D A9 (cannot adjust offset or gain).	178	
136	Replace or repair signal front end A14 (high voltage failure).	178	
137	Replace or repair reference front end A11 (high voltage failure).	178	
138	Replace or repair phase locked loop A5 (defective CLKIN output circuits).	178	
139	Replace or repair timing and control board A4 (defective SAMPLE generator circuits).		
140	Replace or repair microprocessor board A1 (defective 8 MHz clock circuit).		
141	Replace or repair timing and control A4 (defective state machine circuit).		
142	Replace or repair signal A/D A9 (defective DONE output).	178	
143	Replace or repair reference A/D A12 (defective DONE output).	178	
144	Replace or repair signal A/D A12 (defective clock and data outputs).	178	
145	Replace or repair reference A/D A9 (defective clock and data outputs).	178	
146	Replace or repair timing and control A4 (defective preloads circuits).		
147	Replace or repair timing and control A4 (microprocessor access to accumulator not possible).		
148	Replace or repair signal front end A14.	178	
149	Replace or repair reference front end A11.	178	
150	Replace or repair signal A/D A12.	178	

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
151	Replace or repair reference A/D A9.	178	
152	Replace signal filter A13.		
153	Replace reference filter A10.		
154	Replace or repair signal accumulator A6.		
155	Replace or repair reference accumulator A7.		
156	Replace or repair autocal board A8 (defective test mode DIP switch circuits).	178	
157	Replace or repair I/O A3 (defective DIP switch circuits).	178	
158	Replace I/O cable assembly.		
159	Replace or repair I/O A3 (defective IEEE-488 interface circuits).	178	
160	Replace or repair I/O A3 (defective recorder output circuits).	178	
161	Replace or repair memory board A2 (short on 8 MHz line).		
162	Replace or repair I/O A3 (short on 8 MHz line).		
163	Replace or repair timing and control A4 (short on 8 MHz line).		
164	Replace or repair display driver A15A2 (short on 8 MHz line).		
165	Replace or repair microprocessor A1 (defective address or data bus).		
166	Replace or repair memory A2 (produces bus error (BERR)).		
167	Replace or repair memory A2.		
168	Replace or repair display A15A3.		
169	Replace or repair display driver A15A2.		

Table 4-6. DAV Troubleshooting Procedure (Continued)

STEP #	PROCEDURE	IF YES STEP	IF NO STEP
170	Replace ribbon cables between display A15A3 and display driver A15A2.		
171	Replace or repair keyboard A15A1 (defective LED).		
172	Replace or repair display driver A15A2 (defective keyboard interface circuits).		
173	Replace ribbon cable between keyboard A15A1 and display driver A15A2.		
174	Replace keyboard A15A1 (defective switch).		
175	Replace or repair I/O A3 (defective trigger input circuits).	178	
176	Replace or repair microprocessor A1 (defective interrupt circuits).		
177	Inconclusive result (recheck symptom in tables 4-1 through 4-5).		
178	Perform an alignment on the circuit card which was replaced (see section 3).		
179	Replace or repair motherboard A16A1 (shorted).		

MODEL 2250

SECTION 5

REPAIR

5-1. INTRODUCTION.

This section provides procedures for the removal and replacement of assemblies and parts found to be defective. Use the following list of removals and replacements to help select the best procedure needed to effect a repair after troubleshooting.

Procedure	Paragraph
Circuit Card Assemblies (CCAs) A1 to A14 Removal	5-2a
CCAs A4, A5, A8, A9, A12 Shield Removal	5-2b
CCAs A10, A13 Shield Removal	5-2c
CCAs A11, A14 Shield Replacement	5-2d
Circuit Card Assemblies A1 to A14 Replacement	5-3
CCAs A4, A5, A8, A9, A12 Shield Replacement	5-3a
CCAs A10, A13 Shield Replacement	5-3b
CCAs A11, A14 Shield Replacement	5-3c
Circuit Card Assemblies A1 to A14 Replacement	5-3d
Front Bezel Assembly A15 Removal and Disassembly	5-4
Front Bezel Assembly A15 Removal	5-4a
Isolation Assemblies A15A4, A15A5 Removal	5-4b
Display Driver CCA A15A2, Keyboard A15A1, and Display CCA A15A3 Removal	5-4c
Front Bezel Assembly A15 Reassembly and Replacement	5-5
Display Driver CCA A15A2, Keyboard A15A1, and Display CCA A15A3 Replacement	5-5a
Isolation Assemblies A15A4, A15A5, and Shield Replacement	5-5b
Front Bezel Assembly A15 Replacement	5-5c
Rear Panel Assembly A17 Removal and Disassembly	5-6
Rear Panel Assembly A17 Removal	5-6a

Procedure	Paragraph
Isolated Power Supplies A17PS2 and A17PS3 Removal	5-6b
Main Power Supply Assembly A17PS1 Removal	5-6c
Main Power Transformer A17T1 Removal	5-6d
Fan Assembly A17B1 Removal	5-6e
Main Harness Assembly A17W1 Removal	5-6f
Address Switch A17S1 Removal	5-6g
I/O Cable Assembly A17W5 Removal	5-6h
Rear Panel Assembly A17 Reassembly and Replacement	5-7
I/O Cable Assembly A17W5 Replacement	5-7a
Address Switch A17S1 Replacement	5-7b
Main Harness Assembly A17W1 Replacement	5-7c
Fan Assembly A17B1 Replacement	5-7d
Main Transformer A17T1 Replacement	5-7e
Main Power Supply Assembly A17PS1 Replacement	5-7f
Isolated Power Supplies A17PS2 and A17PS3 Replacement	5-7g
Rear Panel Assembly A17 Replacement	5-7h
Motherboard A16A1 Removal	5-8
Motherboard A16A1 Replacement	5-9

Use standard shop practices and refer to the exploded view in figure 5-1 when doing removal and replacement.

WARNING

Disconnect DAV from ac power and disconnect signal and reference inputs at front and rear panel connectors before attempting any removal and replacement.

5-2. CIRCUIT CARD ASSEMBLIES (CCAs) A1 TO A14 REMOVAL.

a. CCA REMOVAL. (See figure 5-1, sheet 1.)

1. Remove four screws (1) and remove DAV top cover (2).

2. Before removing CCAs A3 to A8, disconnect I/O cable connector A17W5J2 (3) from connector A15A3P2 (4).

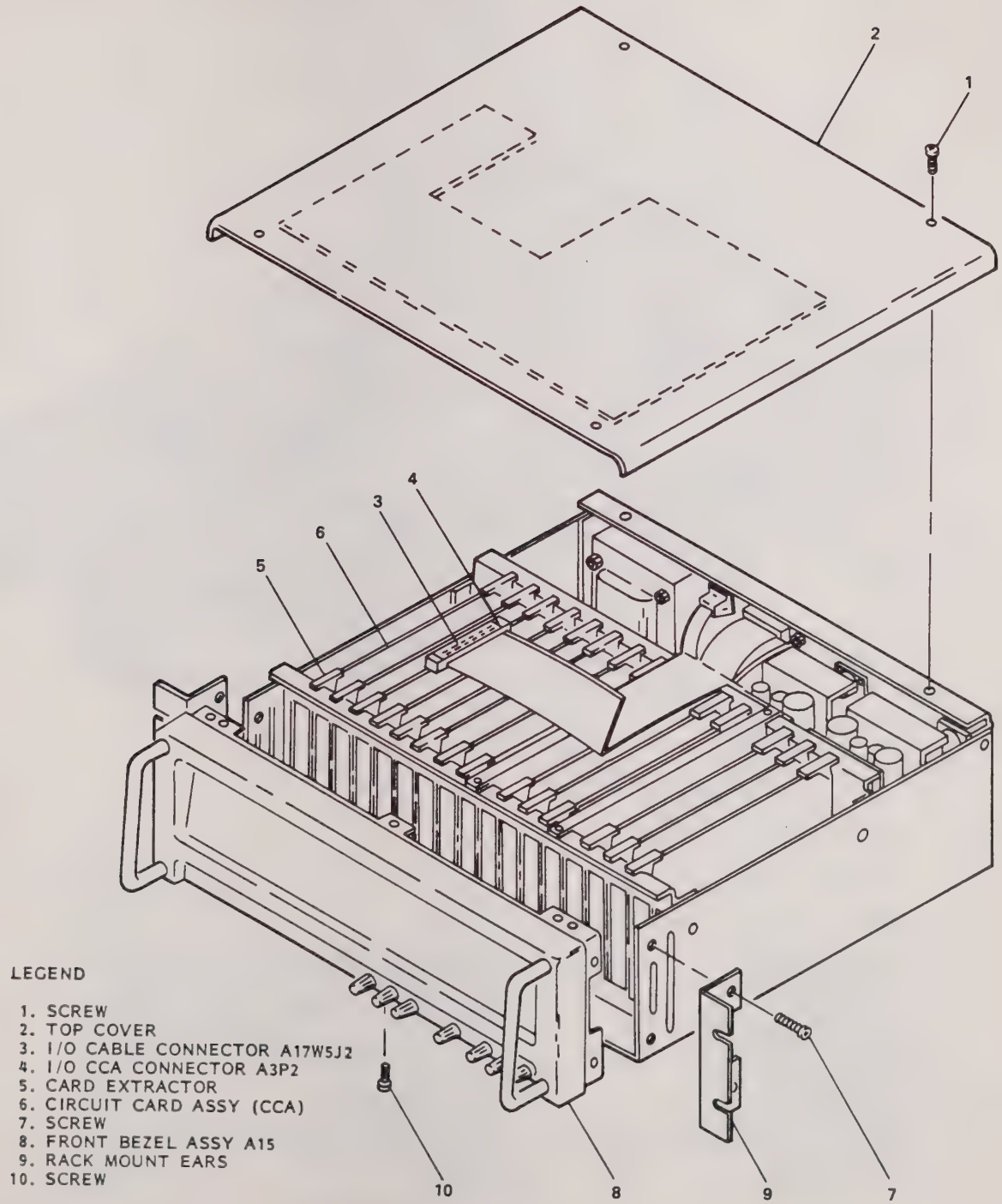
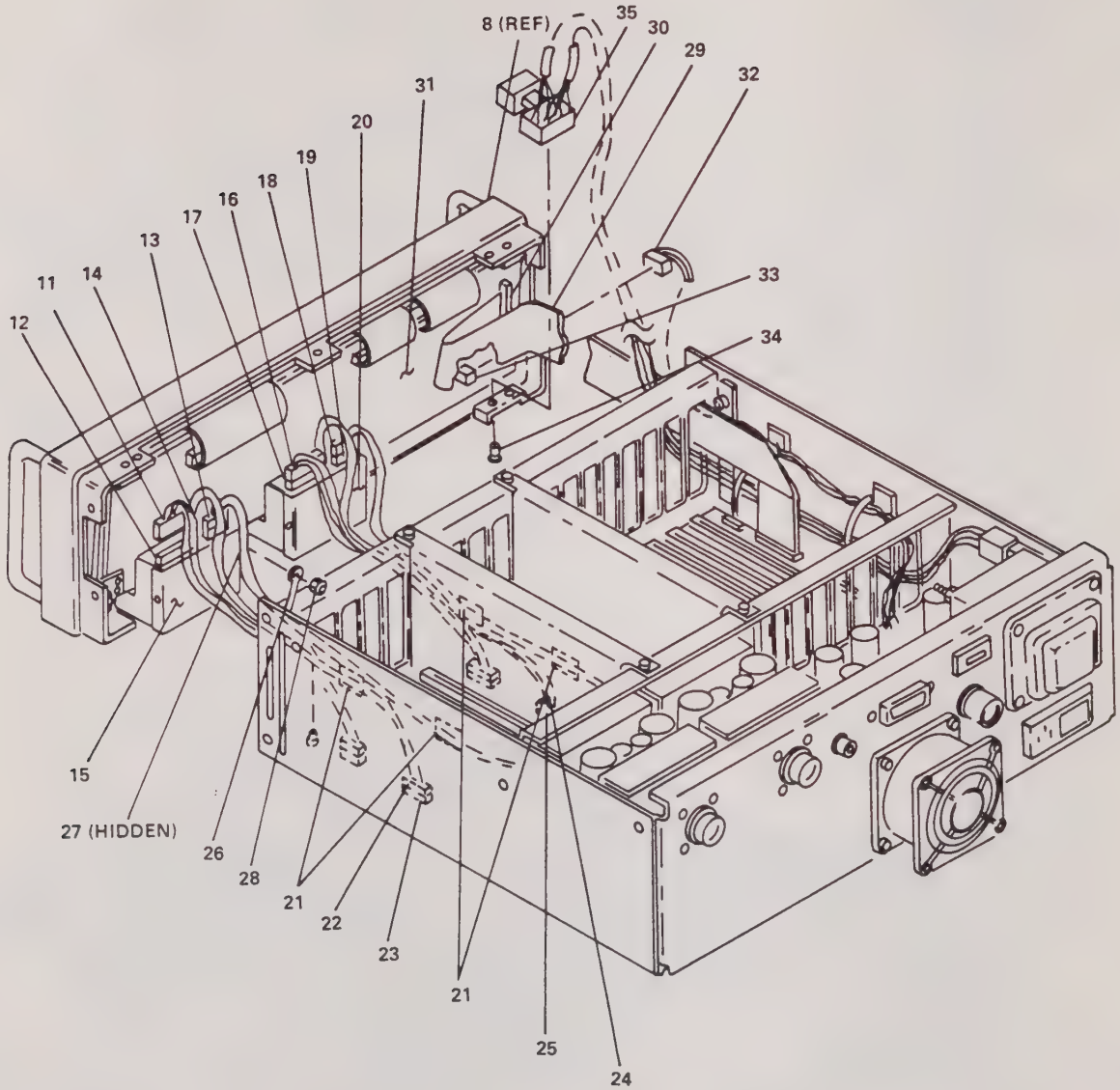


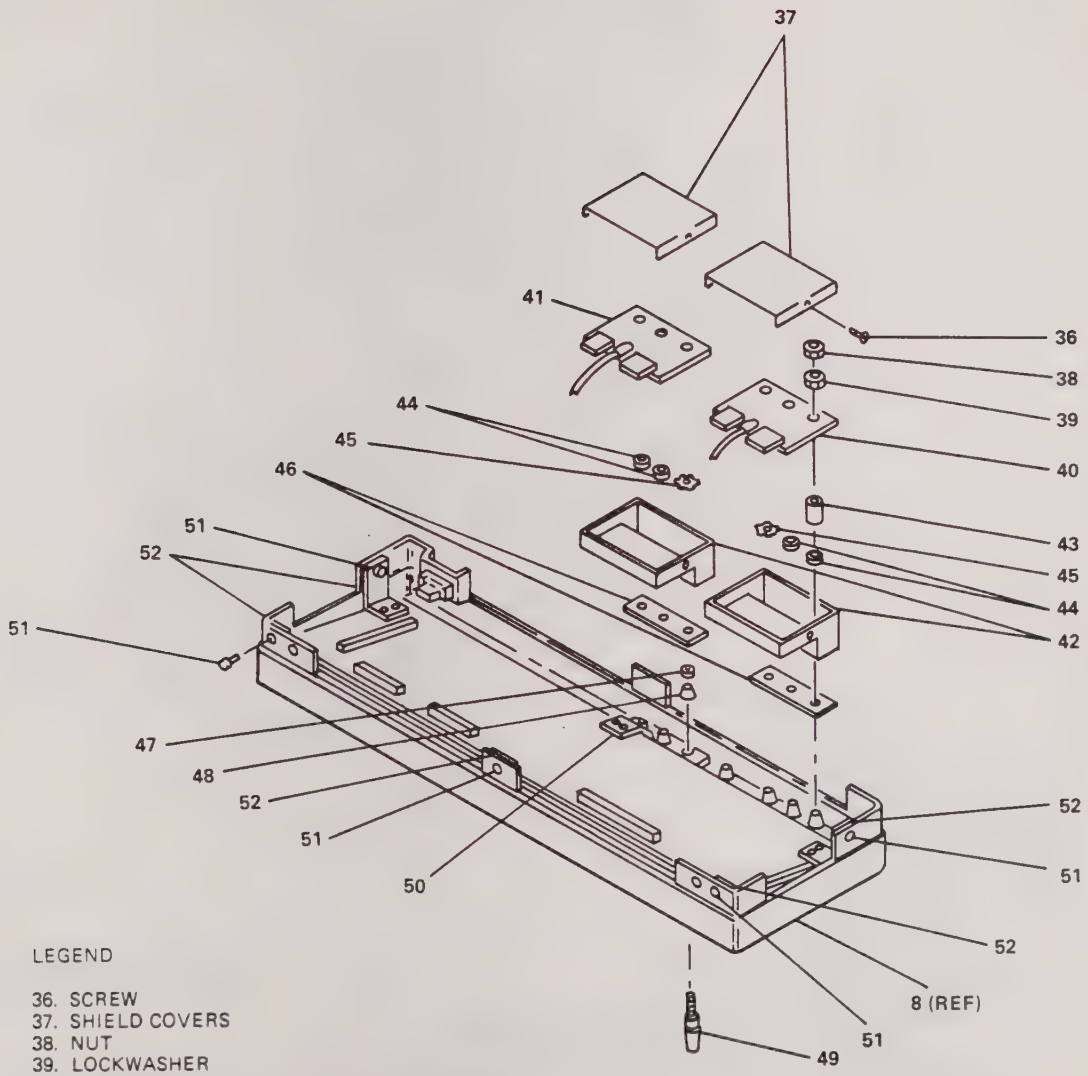
Figure 5-1. DAV, Exploded View (Sheet 1 of 7)



LEGEND

11. HARNESS JACK
12. CONNECTOR A15A4J1
13. HARNESS JACK
14. CONNECTOR A15A4J2
15. SIGNAL ISOLATION ASSY A15A4
16. HARNESS JACK
17. CONNECTOR A15A5J1
18. HARNESS JACK
19. CONNECTOR A15A5J2
20. REFERENCE ISOLATION ASSY A15A5
21. CABLE TIES
22. HARNESS JACK
23. CONNECTOR A16A1J23
24. HARNESS JACK
25. CONNECTOR A16A1J20
26. GROUND WIRE
27. CIRCUIT GROUND BINDING POST
28. NUT
29. 34-PIN RIBBON CABLE
30. CONNECTOR A15A2J3
31. DISPLAY DRIVER CCA A15A2
32. MAIN POWER HARNESS JACK A15A2J5
33. CONNECTOR A16A18J5
34. SCREW
35. POWER SWITCH A15SW1

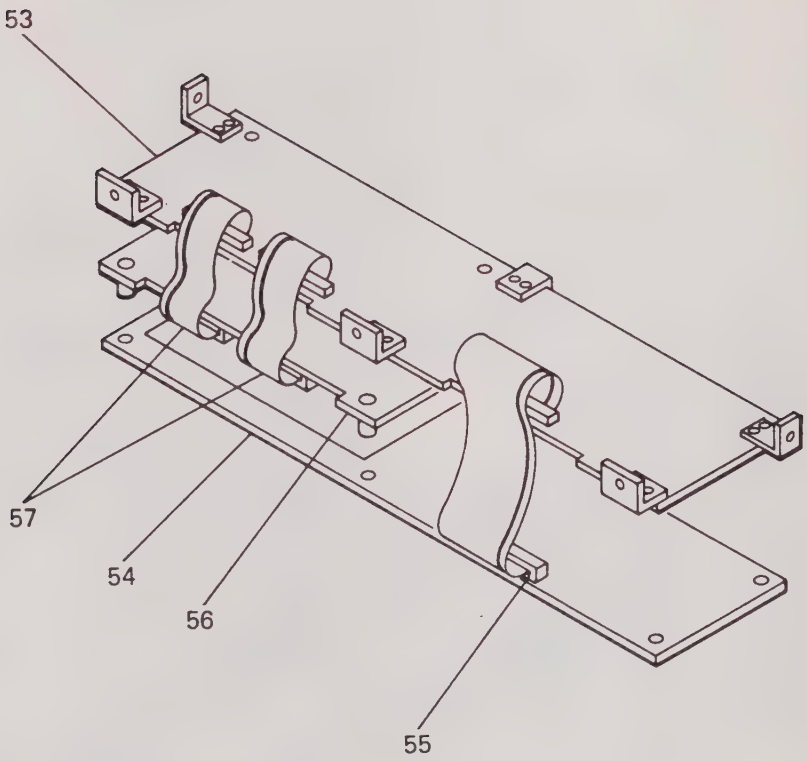
Figure 5-1. DAV, Exploded View (Sheet 2 of 7)



LEGEND

36. SCREW
37. SHIELD COVERS
38. NUT
39. LOCKWASHER
40. SIGNAL ISOLATION ASSY A15A4 P/N 787448-1
41. REFERENCE ISOLATION ASSY A15A5 P/N 787448-2
42. ASSEMBLY SHIELDS
43. MALE-FEMALE STANDOFFS
44. NYLON INSULATORS
45. EXTERNNAL TOOTH LOCKWASHER
46. INSULATORS
47. NUT
48. INSULATOR
49. REFERENCE CHANNEL BINDING POST
50. BRACKET
51. SCREW
52. BRACKET

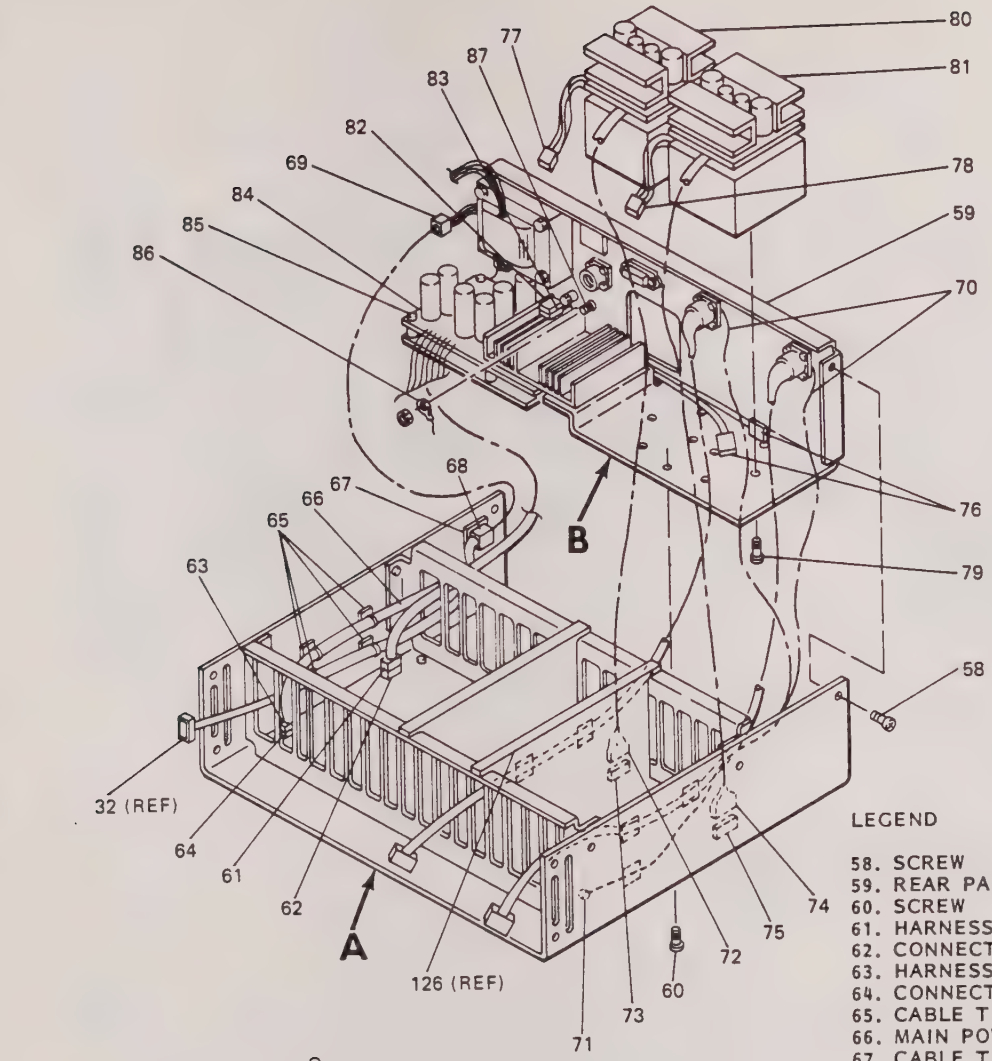
Figure 5-1. DAV, Exploded View (Sheet 3 of 7)

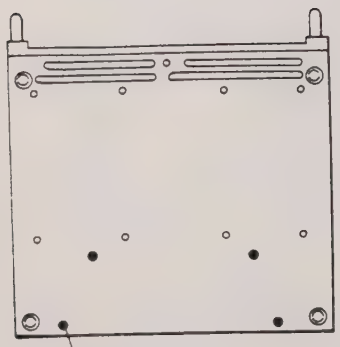


LEGEND

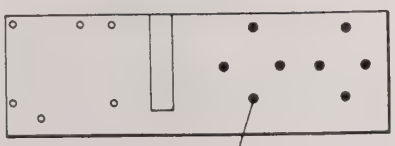
53. DISPLAY DRIVER CCA A15A2
54. KEYBOARD A15A1
55. 50-PIN CONNECTOR
56. DISPLAY CCA A15A3
57. 40-PIN CONNECTORS

Figure 5-1. DAV, Exploded View (Sheet 4 of 7)





A
BOTTOM MAIN CHASSIS

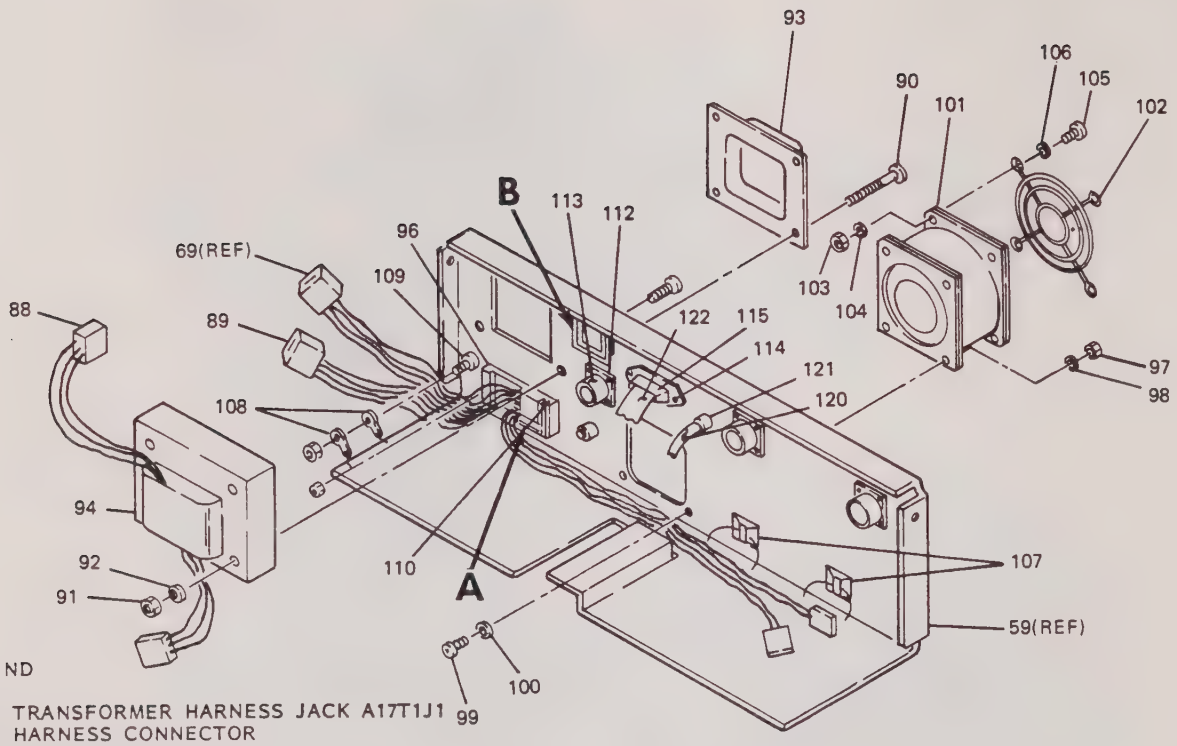


B
BOTTOM REAR PANEL ASSY

LEGEND

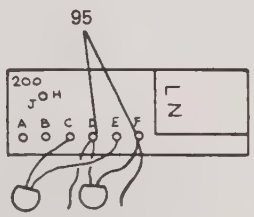
58. SCREW
59. REAR PANEL ASSY A17
60. SCREW
61. HARNESS JACK A17PS1P16
62. CONNECTOR A16A1J16
63. HARNESS JACK A17PS1P17
64. CONNECTOR A16A1J17
65. CABLE TIES
66. MAIN POWER SUPPLY CABLE
67. CABLE TIE
68. HARNESS JACK
69. CONNECTOR A17W1P1
70. GROUND WIRES
71. STANDOFF
72. HARNESS JACK
73. CONNECTOR A16A1J18
74. HARNESS JACK
75. CONNECTOR A16A1J21
76. HARNESS ASSEMBLY JACKS
77. CONNECTOR A17PS2J1
78. CONNECTOR A17PS3J1
79. SCREW
80. ISOLATED POWER SUPPLY A17PS2
81. ISOLATED POWER SUPPLY A17PS3
82. HARNESS JACK
83. CONNECTOR A17PS1J1
84. MAIN POWER SUPPLY A17PS1
85. SCREW
86. GROUND WIRE
87. CIRCUIT GROUND BINDING POST

Figure 5-1. DAV, Exploded View (Sheet 5 of 7)

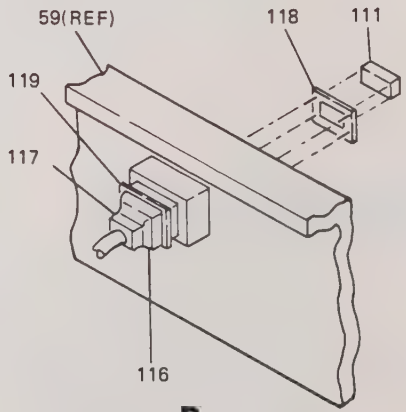


LEGEND

88. TRANSFORMER HARNESS JACK A17T1J1
89. HARNESS CONNECTOR
90. SCREW
91. NUT
92. LOCKWASHER
93. END BELL
94. TRANSFORMER ASSY A17T1
95. SOLDER POINTS
96. LINE ENTRY MODULE
97. NUT
98. LOCKWASHER
99. SCREW
100. FLATWASHER
101. FAN A17B1
102. FAN GUARD
103. NUT
104. LOCKWASHER
105. SCREW
106. FLATWASHER
107. CABLE TIES
108. WIRES
109. GROUND SCREW
110. CLIP
111. ADDRESS SWITCH A17W5S1
112. SCREW
113. MS CONNECTOR A17W5J5
114. SCREW
115. IEEE CONNECTOR A17W5J4
116. TABS
117. SOCKET
118. BEZEL
119. SHIM
120. CABLE
121. BNC CONNECTOR A17W5J3
122. I/O CABLE ASSY A17W5

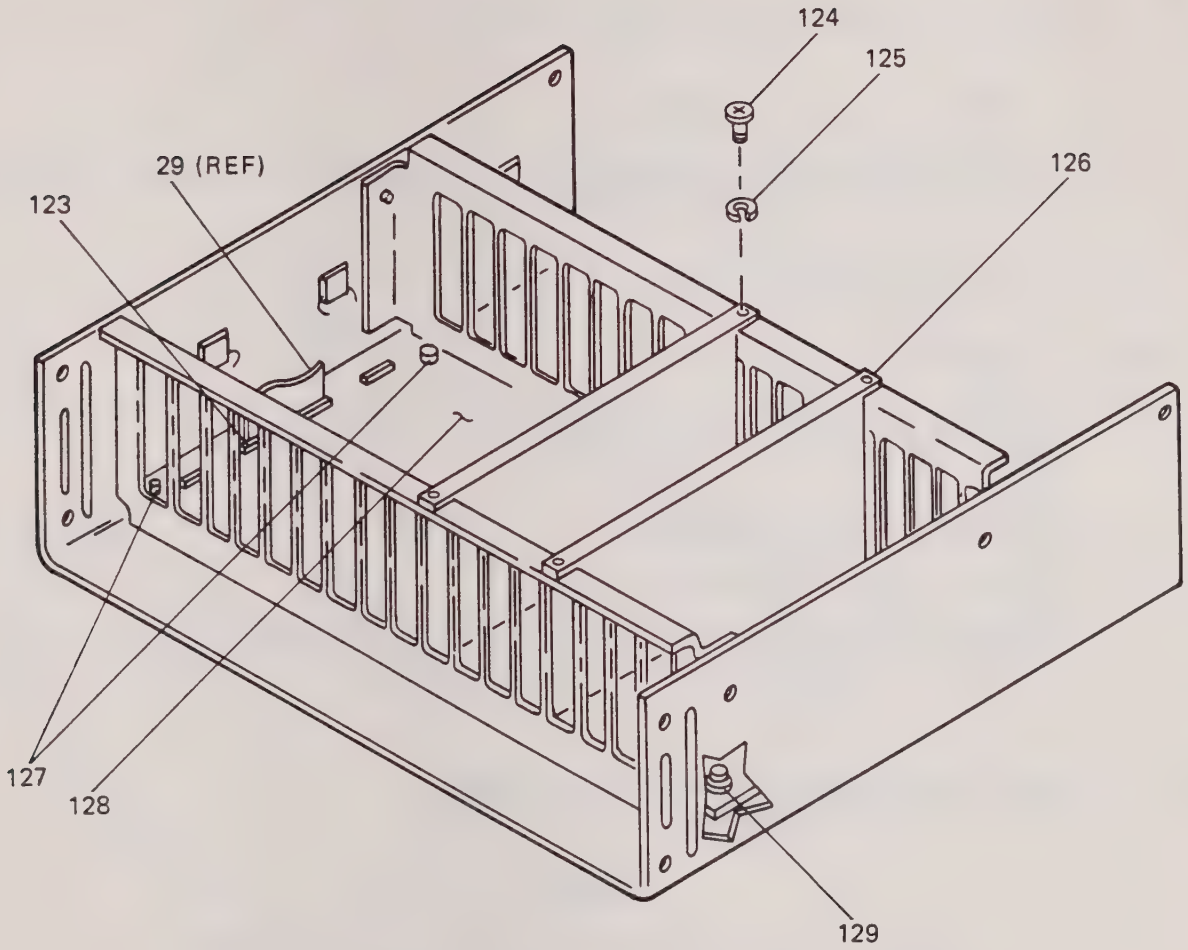


A
LINE ENTRY MODULE ASSY



B
ADDRESS SWITCH

Figure 5-1. DAV, Exploded View (Sheet 6 of 7)



LEGEND

123. MOTHERBOARD CONNECTOR A16A1J1
124. SCREW
125. LOCKWASHER
126. BULKHEAD
127. SELF-LOCKING NUT
128. MOTHERBOARD A16A1
129. STANDOFF

Figure 5-1. DAV, Exploded View (Sheet 7 of 7)

3. Pull up on card extractors (5) and carefully pull CCA (6) out of mother-board connector.

b. CCAs A4, A5, A8, A9, A12, SHIELD REMOVAL.

1. Remove CCA as per paragraph a.

2. Remove four screws and lockwashers (1, figure 5-2) from panel (2) side of CCA (3) and remove shield (4). Remove CCA.

c. CCAs A10 AND A13 SHIELD REMOVAL.

1. Remove CCA as per paragraph a.

2. Remove four screws and lockwashers (1, figure 5-3) from shield side of CCA and remove shield (2). Remove CCA (3) from panel (4).

d. CCAs A11 AND A14 SHIELD REMOVAL.

1. Remove CCA as per paragraph a.

2. Remove four screws and lockwashers (1, figure 5-4) from panel (2) side of CCA (3) and remove shield (4). Remove CCA.

5-3. CIRCUIT CARD ASSEMBLIES A1 TO A14 REPLACEMENT.

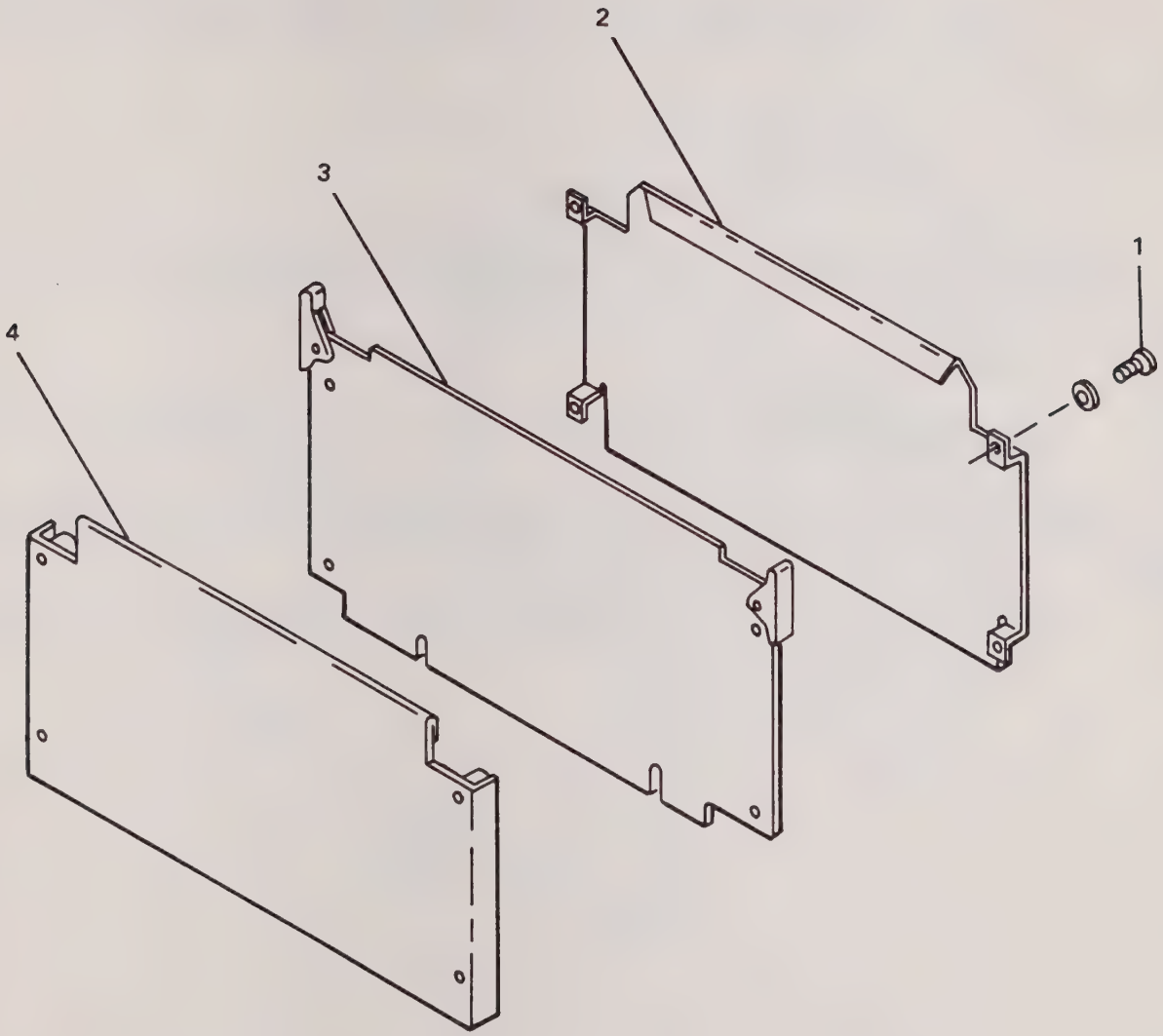
CAUTION

CCAs are keyed to matching connectors in mother-board. Do not force any CCA that meets resistance to insertion. Check for insertion in proper slot.

a. CCAs A4, A5, A8, A9, A12 SHIELD REPLACEMENT.

1. Place CCA (3, figure 5-2) component side against shield (4). Place panel (2) against back of CCA (3). Align screw holes and secure with four screws and lockwashers (1).

2. Replace CCA as per paragraph c.



LEGEND

1. SCREW AND LOCKWASHER
2. PANEL
3. CCA
4. SHIELD

Figure 5-2. CCAs A4, A5, A8, A9, A12 Shield Removal or Replacement

b. CCAs A10, A13, SHIELD REPLACEMENT.

1. Place CCA (3, figure 5-3) wiring side against panel (4). Place shield (2) against component side of CCA. Align screw holes and secure with four screws and lockwashers (1).

2. Replace CCA as per paragraph d.

c. CCAs A11 AND A14 SHIELD REPLACEMENT.

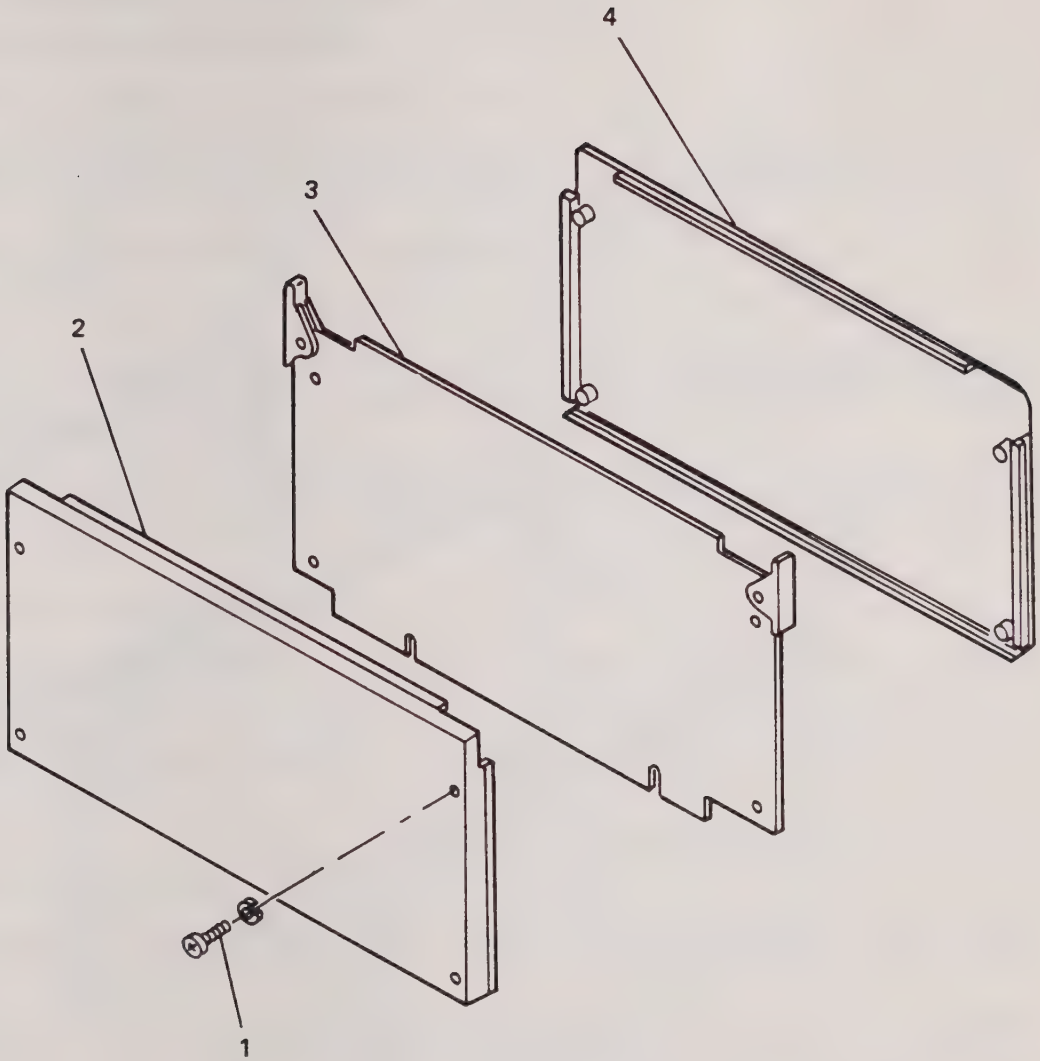
Place CCA (3, figure 5-4) component side against shield (4). Place panel (2) against back of CCA (3). Align screw holes and secure with four screws and lockwashers (1).

d. CCAs REPLACEMENT.

1. Align correct CCA (6, figure 5-1, sheet 1) in slot and carefully push in until inserted into connector.

2. After replacing CCAs A3 to A8, connect I/O cable connector A17W1J2 (3) to I/O CCA plug A15A3P2 (4) being careful to fold cable to face polarizing stripe toward rear of chassis.

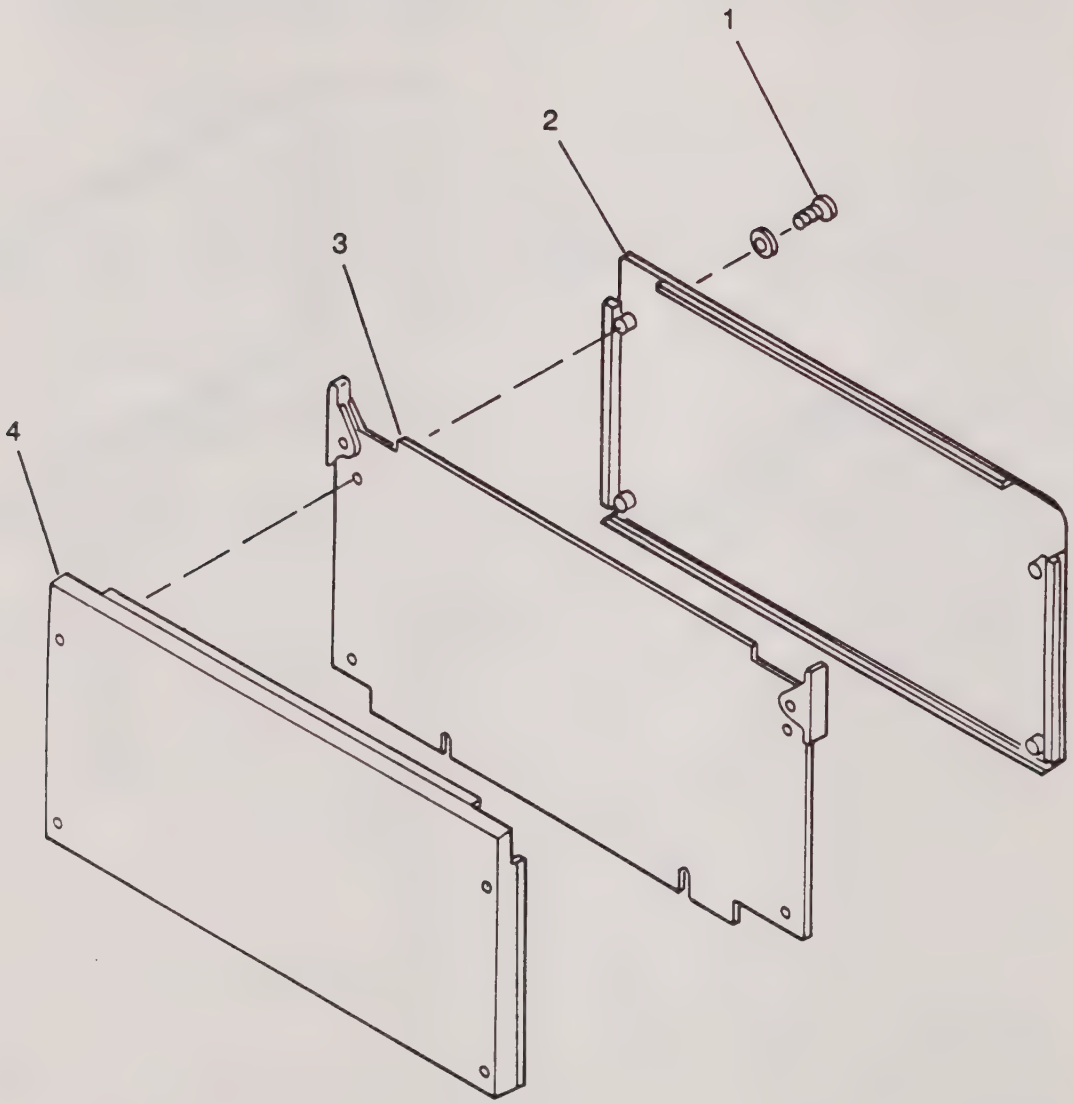
3. Replace top cover (2) with foam pad notch facing rear and secure with four screws (1).



LEGEND

1. SCREW AND LOCKWASHER
2. SHIELD
3. CCA
4. PANEL

Figure 5-3. CCAs A10 and A13 Shield Removal or Replacement



LEGEND

1. SCREW AND LOCKWASHER
2. PANEL
3. CCA
4. SHIELD

Figure 5-4. CCAs A11 and A14 Shield Removal or Replacement

5-4. FRONT BEZEL ASSEMBLY A15 REMOVAL AND DISASSEMBLY.

a. FRONT BEZEL ASSEMBLY A15 REMOVAL.

1. Remove all CCAs as per paragraph 5-2.a.

2. Remove screws (7, figure 5-1, sheet 1) on each side securing front bezel assembly A15 (8) (and rack mount ears (9), if installed) to chassis.

3. Remove center screw (10) on bottom of chassis.

4. Carefully pull out front bezel assembly A15 (8) about an inch.

5. Remove harness jack (11, sheet 2) from connector A15A4J1 (12) and remove harness jack (13) from connector A15A4J2 (14) on signal isolation assembly A15A4 (15).

6. Remove harness jack (16) from connector A15A5J1 (17) and remove harness jack (18) from connector A15A5J2 (19) on reference isolation assembly A15A5 (20).

7. Cut four cable ties (21).

8. Unplug signal isolation assembly harness jack (22) from connector A16A1J23 (23).

9. Unplug reference isolation assembly harness jack (24) from connector A16A1J20 (25).

10. Remove ground wire (26) secured to circuit ground binding post (27) with 5/6-inch nut (28).

11. Remove 34-pin ribbon cable (29) from connector A15A2J3 (30) left side of display driver CCA A15A2 (31).

12. Unplug main power harness jack (32) (red/black wire) from connector A15A2J5 (33) on display driver CCA A15A2 (31).

13. Remove two screws (34) that secure power switch A15SW1 (35) to front bezel assembly A15 (8).

14. Remove front bezel assembly A15 (8).

b. ISOLATION ASSEMBLIES A15A4, A15A5 REMOVAL.

1. Remove front bezel assembly as per paragraph 5-4.a.

2. Remove two screws (36, figure 5-1, sheet 3) on either side of each isolation assembly. Remove shield covers (37).

CAUTION

Use caution not to damage relays.

3. Remove three hex nuts (38) and external tooth lockwasher (39) on each isolation assembly with 1/4-inch thin wall nut driver.

4. Remove signal isolation assembly A15A4 (40) right side and reference isolation assembly A15A5 (41) left side.

5. From inside assembly shields (42), remove three male-female standoffs (43).

NOTE

Before lifting out shields, note position of loose hardware as indicated on sheet 3: nylon insulators (44), external tooth lockwashers (45).

6. Lift out shields (42).

7. Remove insulators (46).

c. DISPLAY DRIVER CCA A15A2, KEYBOARD A15A1, AND DISPLAY CCA A15A3 REMOVAL.

1. Remove front bezel assembly and isolation assemblies as per paragraph 5-4.a and b.

NOTE

Bracket connecting display driver CCA A15A2 to front bezel assembly is secured underneath binding posts of reference channel.

2. Remove nut (47, figure 5-1, sheet 3), insulator (48), and remove reference channel binding post (49), for three posts securing bracket (50).

3. Remove five screws (51) from display driver CCA A15A2 brackets (52) mounted to front bezel assembly A15 (8). This frees the three assemblies.

NOTE

Keyboard A15A1, display driver CCA A15A2, and display CCA A15A3 can be separated for replacement of any one, but the three are kept electrically connected for troubleshooting. (See sheet 4.)

4. To separate display driver CCA A15A2 (53) from keyboard A15A1 (54), disconnect 50-pin connector (55).

5. To separate display CCA A15A3 (56) from display driver CCA A15A2 (53), remove two 40-pin connectors (57).

5-5. FRONT BEZEL ASSEMBLY A15 REASSEMBLY AND REPLACEMENT.

a. DISPLAY DRIVER CCA A15A2, KEYBOARD A15A1, AND DISPLAY CCA A15A3 REPLACEMENT.

1. Electrically connect display driver CCA A15A2 (53, figure 5-1, sheet 4) with keyboard A15A1 (54) using 50-pin connector (55) making sure polarizing stripe faces right edge of boards.

2. Electrically connect display driver CCA A15A2 (53) to display CCA A15A3 (56) using two 40-pin connectors (57) making sure polarizing stripes face left edge of boards.

3. Carefully adjust A15A1, A2, and A3 assemblies and align display driver CCA A15A2 brackets (52, sheet 3) over front bezel assembly A15 (8), screw hole and secure with five screws (51).

4. Replace reference channel binding posts (49), and secure display driver bracket (50) to front bezel assembly A15 (8), with insulator (48), and nut (47).

5. Replace isolation assemblies and front bezel assembly A15 as per paragraph 5-5.b and c.

b. ISOLATION ASSEMBLIES A15A4, A15A5, AND SHIELD REPLACEMENT.

1. Place insulators (46, figure 5-1, sheet 3) over binding posts (49).

2. Place assembly shields (42) over binding posts (49).

3. Place nylon insulators (44) and external tooth lockwashers (45) inside assembly shields (42) as indicated on sheet 3.

4. Replace three male-female standoffs (43) over binding posts (49) to secure each assembly shield (42).

NOTE

While securing the isolation assembly shields, maintain 1/8-inch clearance between shield and bezel assembly and 1/8-inch clearance between display driver CCA A15A2 and shield.

5. Place signal isolation assembly A15A4 (40) into right shield (42) and reference isolation assembly A15A5 (41) into left shield (42).

6. With 1/4-inch thin wall nut driver, secure each isolation assembly using three hex nuts (38) and three external tooth lockwashers (39).

7. Place a shield cover (37) over each isolation board assembly. Secure with two screws (36) on each shield.

8. Replace front bezel assembly A15 (8) as per paragraph 5-5.c.

c. FRONT BEZEL ASSEMBLY A15 REPLACEMENT.

1. Position power switch A15SW1 (35, figure 5-1, sheet 2) against bezel and secure with two screws (34).

2. Connect main power harness jack (32) to connector A15A2J5 (33) on display driver CCA A15A2 (31).

3. Connect 34-pin ribbon cable (29) to connector A15A2J3 (30) left side of display driver CCA A15A2 (31). Dress cable as shown in illustration.

4. Secure ground wire (26) to circuit ground binding post (27) with 5/6-inch nut (28).

5. Plug reference isolation harness jack (24) into motherboard connector A16A1J20 (25).

6. Plug signal isolation assembly harness jack (22) into motherboard connector A16A1J23 (23).

7. Plug harness jack (18) into connector A15A5J2 (19) and harness jack (16) into connector A15A5J1 (17) on reference isolation assembly A15A5 (20).

8. Plug harness jack (13) into connector A15A4J2 (14) and harness jack (11) into connector A15A4J1 (12) on signal isolation assembly A15A4 (15).

9. Secure cables to chassis with four cable ties (21).

10. Push front bezel assembly A15 (8) carefully against chassis.

11. Secure front bezel assembly A15 (8) [and rack mount ears (9, sheet 1), if required] with two screws (7) on each side.

12. Secure front bezel assembly A15 (8) with one screw (10) on bottom of chassis.

13. Replace all CCAs as per paragraph 5-3.c.

5-6. REAR PANEL ASSEMBLY A17 REMOVAL AND DISASSEMBLY.

a. REAR PANEL ASSEMBLY A17 REMOVAL.

1. Remove front bezel assembly A15 as per paragraph 5-4.a.

2. Remove one screw (58, figure 5-1, sheet 5) from each side securing rear panel assembly A17 (59) to chassis.

3. Remove four screws (60) from bottom of chassis.

4. Pull rear panel assembly A17 (59) away an inch.

5. Unplug main power supply harness jack A17PS1P16 (61) from motherboard connector A16A1J16 (62) and harness jack A17PS1P17 (63) from motherboard connector A16A1J17 (64).

6. Cut four cable ties (65).

7. Pull disconnected main power supply cables (red/black wire) (66) through back of chassis.

8. Cut cable ties (67) securing main ac power harness jack (68) on chassis and disconnect from main harness connector A17W1P1 (69).

9. Disconnect two ground wires (70) secured to signal and reference input connectors from standoff (71).

10. Unplug isolated power supply A17PS2 harness jack (72) from motherboard connector A16A1J18 (73) and isolated power supply A17PS3 harness jack (74) from motherboard connector A16A1J21 (75). Pull both harnesses through back of chassis.

b. ISOLATED POWER SUPPLIES A17PS2 AND A17PS3 REMOVAL.

1. Remove rear panel assembly A17 as per paragraph 5-6.a.

2. Unplug (and tag) two 4-pin jacks (76, figure 5-1, sheet 5) on harness assembly from isolated power supply connectors A17PS2J1 (77) and A17PS3J1 (78).

3. Remove eight screws (79) from bottom of rear panel assembly (four per isolated power supply assembly).

4. Remove isolated power supplies A17PS2 (80) and A17PS3 (81).

c. MAIN POWER SUPPLY ASSEMBLY A17PS1 REMOVAL.

1. Remove rear panel assembly A17 as per paragraph 5-6.a.

2. Unplug transformer harness jack (82, figure 5-1, sheet 5) from connector A17PS1J1 (83) on main power supply A17PS1 (84).

3. Remove six pan-head screws (85) that secure main power supply A17PS1 (84) to rear panel assembly A17 (59). Lift away main power supply A17PS1 (84).

4. Remove ground wire (86) from black circuit ground binding post (87).

d. MAIN POWER TRANSFORMER A17T1 REMOVAL.

1. Remove rear panel assembly A17 and main power supply assembly A17PS1 as per paragraph 5-6.a and c.

2. Unplug transformer harness jack A17T1J1 (88, figure 5-1, sheet 6) from harness connector (89).

3. Remove four screws (90), four nuts (91) and four lockwashers (92) securing end bell (93) and transformer assembly A17T1 (94) to rear panel assembly A17 (59). Lift away transformer assembly and end bell.

e. FAN ASSEMBLY A17B1 REMOVAL.

1. Remove rear panel assembly A17 and main power supply A17PS1 as per paragraph 5-6.a and c.
2. Unsolder wires D and F (95, figure 5-1, sheet 6) from line entry module (96).
3. Remove four nuts (97) and lockwashers (98) from outside panel and four screws (99) and flatwashers (100) from inside rear panel assembly.
4. Pull fan A17B1 (101) away from outside rear panel assembly.

NOTE

Fan guards are riveted to fans on some units and are not removable.

f. MAIN HARNESS ASSEMBLY A17W1 REMOVAL.

1. Remove rear panel assembly A17, isolated power supplies A17PS2 and A17PS3, main power supply A17PS1, main power transformer A17T1, and fan assembly A17B1 as per paragraph 5-6.a, b, c, d, and e.
2. Cut cable ties (107, figure 5-1, sheet 6) on rear panel assembly.
3. Disconnect wires (108) from ground screw (109).
4. Press in tongs on 2 clips (110) on sides of line entry module (96) and push whole assembly with attached harness out of rear panel assembly.

g. ADDRESS SWITCH A17W5S1 REMOVAL.

1. Using long nose pliers with serrated jaws, grasp address switch A17S1 (111, figure 5-1, sheet 6), and pull straight out from outside of rear panel assembly A17 (59).

h. I/O CABLE ASSEMBLY A17W5 REMOVAL.

1. Remove rear panel assembly A17 and address switch A17W5S1 as per paragraph 5-6.a and g.
2. Remove four screws (112, figure 5-1, sheet 6) securing MS connector A17A1J5 (113) to rear panel assembly (59).
3. Remove two screws (114) securing IEEE connector A17W5J4 (115) to rear panel assembly.
4. Press two tabs (116) on each side of address switch socket (117) and remove bezel (118).
5. Remove shim (119).
6. Tag and cut or unsolder wire from cable (120) connected to BNC connector A17W5J3 (121).
7. Remove I/O cable assembly A17W5 (122).

5-7. REAR PANEL ASSEMBLY A17 REASSEMBLY AND REPLACEMENT.

a. I/O CABLE ASSEMBLY A17W5 REPLACEMENT.

1. Solder wire from cable (120, figure 5-1, sheet 6) to BNC connector A17J3 (121).

2. Place shim (119) over address switch socket (117).

3. Insert address switch socket (117) into hole in rear panel assembly A17 (59).

4. Snap bezel (118) into position on outside of rear panel assembly A17 (59).

5. Secure IEEE connector A17W5J4 (115) with two screws (114).

6. Secure MS connector A17W5J5 (113) with four screws (112).

7. Replace rear panel assembly A17 and address switch A17W5S1 as per paragraph 5-7.b, c, d, e, f, g, and h.

b. ADDRESS SWITCH A17W5S1 REPLACEMENT.

1. Push address switch A17W5S1 (111, figure 5-1, sheet 6) into address switch socket (117) from outside of rear panel assembly A17 (59).

c. MAIN HARNESS ASSEMBLY A17W1 REPLACEMENT.

1. Push harness assembly A17W1 through line entry module assembly rear panel opening and snap line entry module assembly (96, figure 5-1, sheet 6) into place so that tongs on clip (110) are not depressed.

2. Secure lugs on wires (108) to ground screw (109).

3. Secure cable to ties (107) on rear panel assembly A17 (59).

4. Replace fan assembly A17B1, main power supply assembly A17PS1, isolated power supplies, and rear panel assembly A17 as per paragraph 5-7.d, e, f, g, and h.

d. FAN ASSEMBLY A17B1 REPLACEMENT.

1. Place fan assembly A17B1 (101, figure 5-1, sheet 6) against rear panel assembly A17 (59) and align screw holes. Check to ensure that air flow direction arrow on fan A17B1 (101) is pointing away from rear panel.

2. Secure fan A17B1 (101) with four screws (99) and flatwashers (100) from inside rear panel assembly and four nuts (97) and lockwashers (98) from outside of rear panel.

3. Attach fan guard (102) to fan A17B1 (101) using four 6-32 hex nuts (103), #6 lockwashers (104), 6-32 panhead screws (105), and #6 split flatwashers (106).

NOTE

Fan guards are riveted to fans on some units and are not removable.

4. Replace main power supply assembly A17PS1 and rear panel assembly A17 as per paragraph 5-7.f and h.

e. MAIN TRANSFORMER A17T1 REPLACEMENT.

1. Place transformer assembly A17T1 (94, figure 5-1, sheet 6) on inside of rear panel assembly and end bell (93) on outside of rear panel assembly and align screw holes.

2. Secure transformer assembly A17T1 (94) to inside of rear panel assembly A17 (59) and end bell (93) to outside of rear panel assembly with four screws (90) through end bell with four lockwashers (92) and four nuts (91) on transformer.

3. Connect transformer harness jack A17T1J1 (88) to harness connector (89).

4. Replace main power supply assembly A17PS1 and rear panel assembly A17 as per paragraph 5-7.f and h.

f. MAIN POWER SUPPLY ASSEMBLY A17PS1 REPLACEMENT.

1. Secure ground wire (86, figure 5-1, sheet 5) to circuit ground binding post (87).

2. Place main power supply A17PS1 (84) inside of rear panel assembly and align screw holes. Secure main power supply A17PS1 (84) with six screws (85).

3. Replace rear panel assembly as per paragraph 5-7.h.

g. ISOLATED POWER SUPPLIES A17PS2 AND A17PS3 REPLACEMENT.

1. Connect two 4-pin harness jacks (76, figure 5-1, sheet 5) on harness to isolated power supply connectors A17PS2J1 (77) and A17PS3J1 (78).

2. Place isolated power supplies A17PS2 (80) and A17PS3 (81) on inside of rear panel assembly (59) and align screw holes.

3. Secure isolated power supplies A17PS2 (80) and A17PS3 (81) to bottom of rear panel assembly with four screws (79) on each isolated power supply.

4. Replace rear panel assembly A17 as per paragraph 5-7.h.

h. REAR PANEL ASSEMBLY A17 REPLACEMENT.

1. Place rear panel assembly A17 (59, figure 5-1, sheet 5) an inch away from chassis.

2. Pull two ground wires (70) from signal and reference input connectors through first rear right opening in chassis, through chassis and secure to circuit ground binding post (71).

3. Pull isolated power supply A17PS3 harness jack (74) through first rear right opening in chassis and connect to motherboard connector A16A1J21 (75).

4. Pull isolated power supply A17PS2 harness jack (72) through first rear right opening in chassis to the left of bulkhead (126) and connect to motherboard connector A16A1J18 (73).

5. Connect main ac power harness jack (68) on chassis to main harness connector A17W1P1 (69).

6. Secure cable with tie (67).

7. Pull main power supply cables (red/black wire) (66) through first rear left opening in chassis, through chassis, and pull main power harness jack (32) through first left front opening of chassis. Two harness jacks from main power supply cable hang free in chassis.

8. Plug main power supply harness jack A17PS1P17 (63) into motherboard connector A16A1J17 (64) and plug harness jack A17PS1P16 (61) into motherboard connector A16A1J16 (62).

9. Secure cables with four ties (65).

10. Push rear panel assembly A17 (59) against chassis.

11. Secure rear panel assembly A17 (59) to chassis on each side with one screw (58).

12. Secure rear panel assembly A17 (59) to bottom of chassis with four screws (60).

13. Replace front bezel assembly A15 as per paragraph 5-4.c.

14. Replace CCAs A1 to A14 as per paragraph 5-3.c.

5-8. MOTHERBOARD A16A1 REMOVAL.

a. Remove circuit card assemblies A1 to A14 as per paragraph 5-2.a.

b. Remove front bezel assembly A15 as per paragraph 5-4.a.

c. Remove rear panel assembly A17 as per paragraph 5-6.a.

d. Disconnect 34-pin ribbon cable (29, figure 5-1, sheet 7) from motherboard connector A16A1J1 (123).

e. Remove two screws (124) and lockwashers (125) securing two bulkheads (126).

f. Remove seven self-locking nuts (127) securing motherboard (128) to chassis.

g. Remove standoff (129) from front right corner. Remove motherboard A16A1 (128).

5-9. MOTHERBOARD A16A1 REPLACEMENT.

a. Position motherboard A16A1 (128, figure 5-1, sheet 7) in chassis and align screw holes.

b. Secure motherboard A16A1 (128) to chassis with seven self-locking nuts (127).

c. Replace standoff (129) on front right-hand corner.

d. Align two bulkheads (126) over screw holes and secure with two lockwashers (125) and screws (124).

e. Connect ribbon cable (29) to motherboard connector A16A1J1 (123).

f. Replace rear panel assembly A17 as per paragraph 5-7.h.

g. Replace front bezel assembly A15 as per paragraph 5-5.c.

h. Replace circuit card assemblies A1 to A14 as per paragraph 5-3.c.

SECTION 6

PARTS LIST

6-1. INTRODUCTION.

This section contains replaceable parts lists, federal supply codes of manufacturers (FSCM), parts location diagrams, and a list of manufacturers of parts used for the Model 2250 Digital Analyzing Voltmeter.

6-2. PARTS LIST.

The parts list contains only replaceable parts for the DAV. It is prepared in tabular form and divided into five columns as follows:

a. Column 1 - REF DES./Figure and Index No.

1. Reference designations. Lists alphanumerical reference designations for circuit card assembly replaceable parts shown on schematic and parts location diagrams.

2. Figure and Index Number. Lists index numbers for top assembly parts breakdown illustrations, if applicable.

b. Column 2 - Description. Contains descriptions which identify replaceable parts.

c. Column 3 - NAI P/N. Lists North Atlantic Industries part numbers assigned to replaceable parts.

d. Column 4 - FSCM. Lists Federal Supply Code for Manufacturers. The FSCM identifies manufacturer or government agency whose number is listed in the manufacturer's part number column. If a FSCM is not assigned to a manufacturer, a five letter code is given and alphabetically referenced (AAAAA, BBBBB, etc.) to the List of Manufacturer's table within this manual.

e. Column 5 - MFR P/N. Lists manufacturer's part numbers of replaceable parts or data to aid in determining parts substitution.

6-3. LIST OF MANUFACTURERS.

This list contains the names, addresses, FSCMs, and other identifying codes of manufacturers referenced in the parts list. It is arranged numerically using the manufacturer's FSCMs provided in the Federal Supply Code for Manufacturers, Cataloging Handbooks H4-1, H4-2, and H4-3.

The list is prepared in tabular form as follows:

a. Column 1 contains FSCMs of all manufacturers referenced in the parts list.

b. Column 2 contains the names and addresses of manufacturers applicable to FSCMs listed in column 1.

6-4. PARTS LOCATION ILLUSTRATIONS.

Parts location illustrations are provided to give the user a quick and positive method for locating parts on specific assemblies being repaired. Each illustration provides corresponding location index numbers and each parts location diagram provides reference designations for circuit card components.

Table 6-1. Digital Analyzing Voltmeter Model 2250, Part Number 402250-FX Common Parts

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
A1	Microprocessor Circuit Card Assembly	787170	07342	787170
A2	Memory Circuit Card Assembly	787171-4	07342	787171-4
A3	I/O Circuit Card Assembly	787172-2	07342	787172-2
A4	Timing and Control Circuit Card Assembly	787173-1	07342	787173-1
A5	Phase Locked Loop Circuit Card Assembly	787192-1	07342	787192-1
A6,A7	Accumulator Circuit Card Assembly	787193-1	07342	787193-1
A8	Autocal Circuit Card Assembly	787274-2	07342	787274-2
A9	A/D Converter Circuit Card Assembly	787664	07342	787664
A10	Filter Circuit Card Assembly	787176-1	07342	787176-1
A11	Front End Circuit Card Assembly	787505-1	07342	787505-1
A12	Same as A9			
A13	Same as A10			
A14	Same as A11			
A15	Front Bezel Assembly	787198	07342	787198
A16	Chassis Assembly	787197-2	07342	787197-2
A16A1	Mother Board Circuit Card Assembly	787177	07342	787177
A16W1	Relay Isolation Cable Assembly (#4)	548516	07342	548516
A16W2	Same as A16W1			
A17	Rear Panel Assembly	787277	07342	787277
F1	Fuse, 2A, 250 V	883922	75915	312002
F1	Fuse, 1A, 250 V, 3AG (for 230 V operation only)	800118	75915	312001
W1	Line Cord, 3 Conductor, Detachable, Unshielded	870165	70903	17251

Table 6-2. Model 2250 DAV - F1 Feature 1, Option 1 - IEEE-488 Interface - Unique Parts

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U1	PROM, Programmed	888671-1	07342	888671-1
U2	PROM, Programmed	888671-2	07342	888671-2
U3,U4	Not used			

Table 6-3. Model 2250 DAV - F2 Feature 1, Option 2 - MATE-CIIL Interface - Unique Parts

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U1	PROM, Programmed	888672-1	07342	888672-1
U2	PROM, Programmed	888672-2	07342	888672-2
U3,U4	Not used			

Table 6-4. Model 2250 DAV - F3 Feature 1, Option 3 - Model 225 Emulation IEEE Interface - Unique Parts

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U1	PROM, Programmed	887989-1	07342	887989-1
U2	PROM, Programmed	887989-2	07342	887989-2
U3,U4	Not used			
U5	PROM, Programmed	887989-3	07342	887989-3
U6	PROM, Programmed	887989-4	07342	887989-4

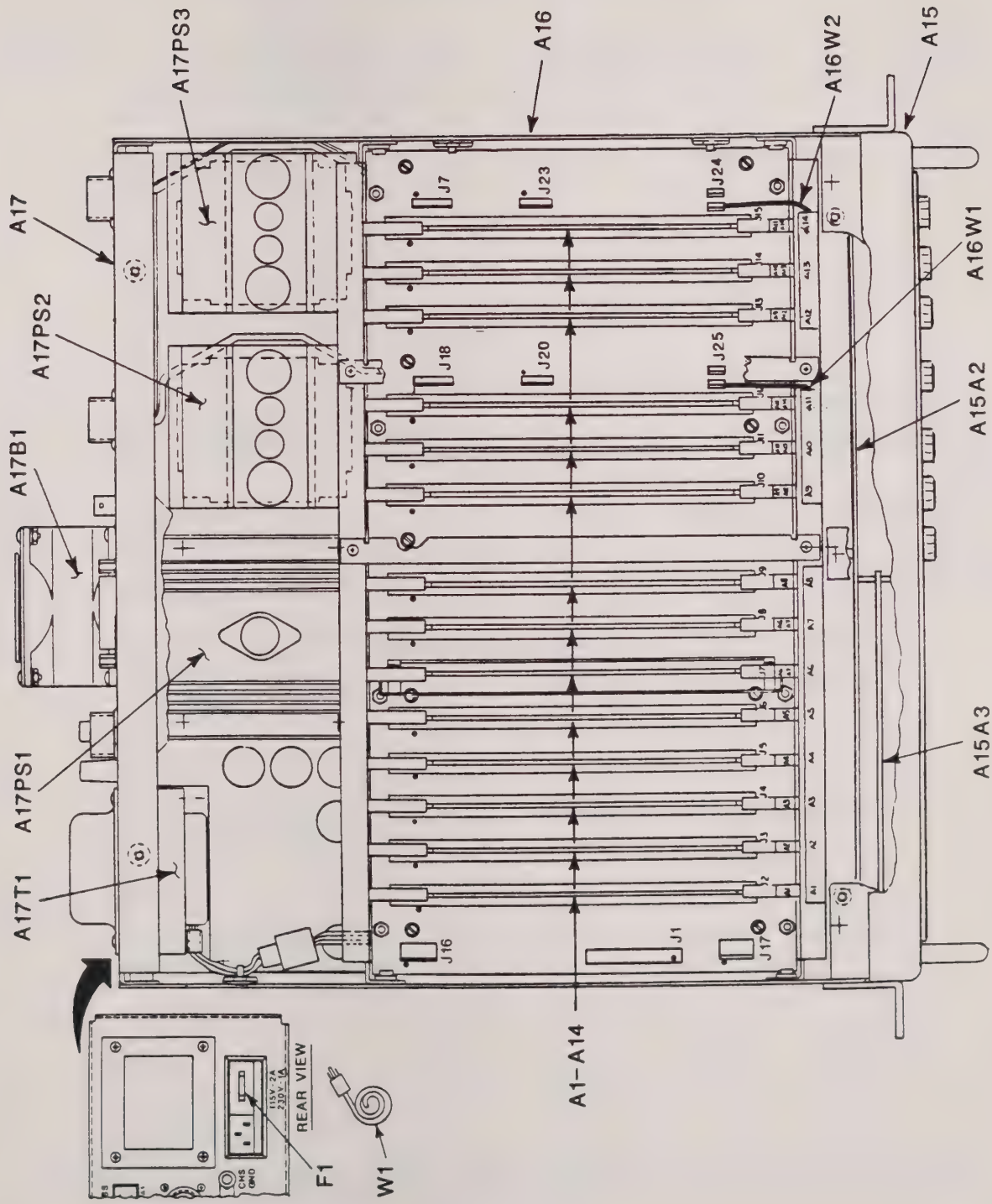


Figure 6-1. Model 2250 DAV Chassis Assembly, Parts Location

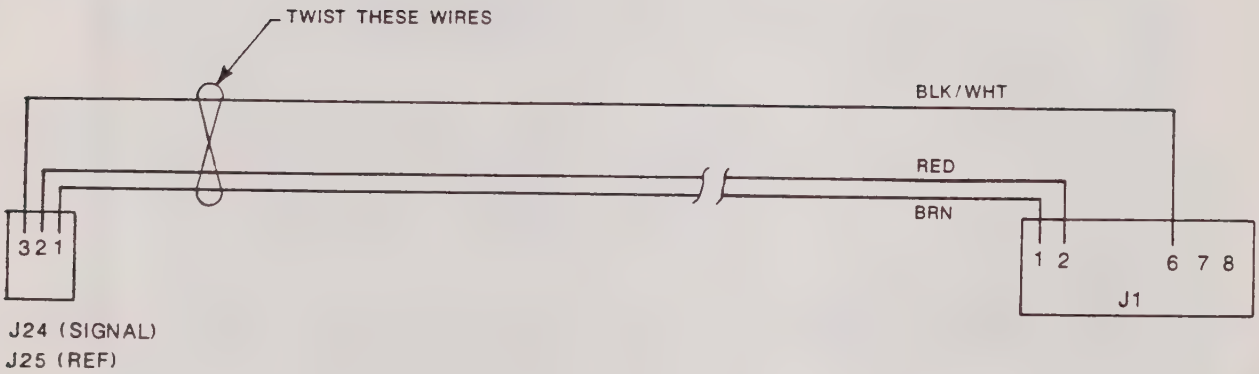


Figure 6-2. Relay Isolation Cable Assembly (#4) A16W1, A16W2 (P/N 548516), Parts Location

Table 6-5. Replacement Parts List: Microprocessor Circuit Card Assembly A1 - 787170 Revision F

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	886063	16299	SR215E104MAA
C2	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C3	Same as C1			
C4	Capacitor, Ceramic, 0.47 uf, 50 V, ±10%	882449	09182	CKR06BK474KP
C5,C6	Same as C1			
C7	Capacitor, Ceramic, 0.01 uf, 100 WVDC, ±10%	808487	56289	CKR06BX103KL
C8	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	885498	DDDDD	SA105E104MAA
C9-C27	Same as C8			
L1	Ferrite Wide Band Choke	886121	02114	VK20-09/3B
R1	Resistor, Composition, 1 M, 1/4 W, ±5%	880100	01121	CB1055
R2	Same as R1			
R3	Resistor, Composition, 3.3 k, 1/4 W, ±5%	803388	01121	CB3325
R4,R5	Same as R3			
TP1	Post, P and Cont., Mod II, Machine Applied	880007	00779	87022-9
TP2-TP11	Same as TP1			
U1	Timer	883803	18324	SE-555-FE
U2	IC, TTL, Hex Invertor Buffer/Driver	808971	01295	SN7406N
U3	IC, TTL, Quad 2-Input OR Gate	808898	01295	SN74LS32N

Table 6-5. Replacement Parts List: Microprocessor Circuit Card Assembly A1 - 787170 Revision F (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U4	IC, TTL, Dual 4-Input Positive AND Gate	883509	01295	74LS21N
U5	IC, Microcomputer	870338	04713	MC68000DL8
U6	IC, TTL, 8-Bit Encoder	883508	01295	74LS148N
U7	IC, TTL, Octal Line Buffer w/ TriState Outputs	808713	18324	74LS244
U8	IC, Octal Bus Driver	870340	34335	SN74S244F
U9-U11	Same as U7			
U12	IC, LV, TTL, 20-Pin, Bus Receiver, Plastic Case	886186	04713	SN74LS645
U13	Same as U12			
XU5	IC Socket, 64-pin, Low Profile	886122	71279	703-4364-01-06-00
Y1	Crystal, Clk, Oscillator, 8 MHz	886144	00815	HS-100 @8.000 MHz
Z1	Resistor, Network, 3.3 k, 15 Res	885964	32997	4116R-002-332

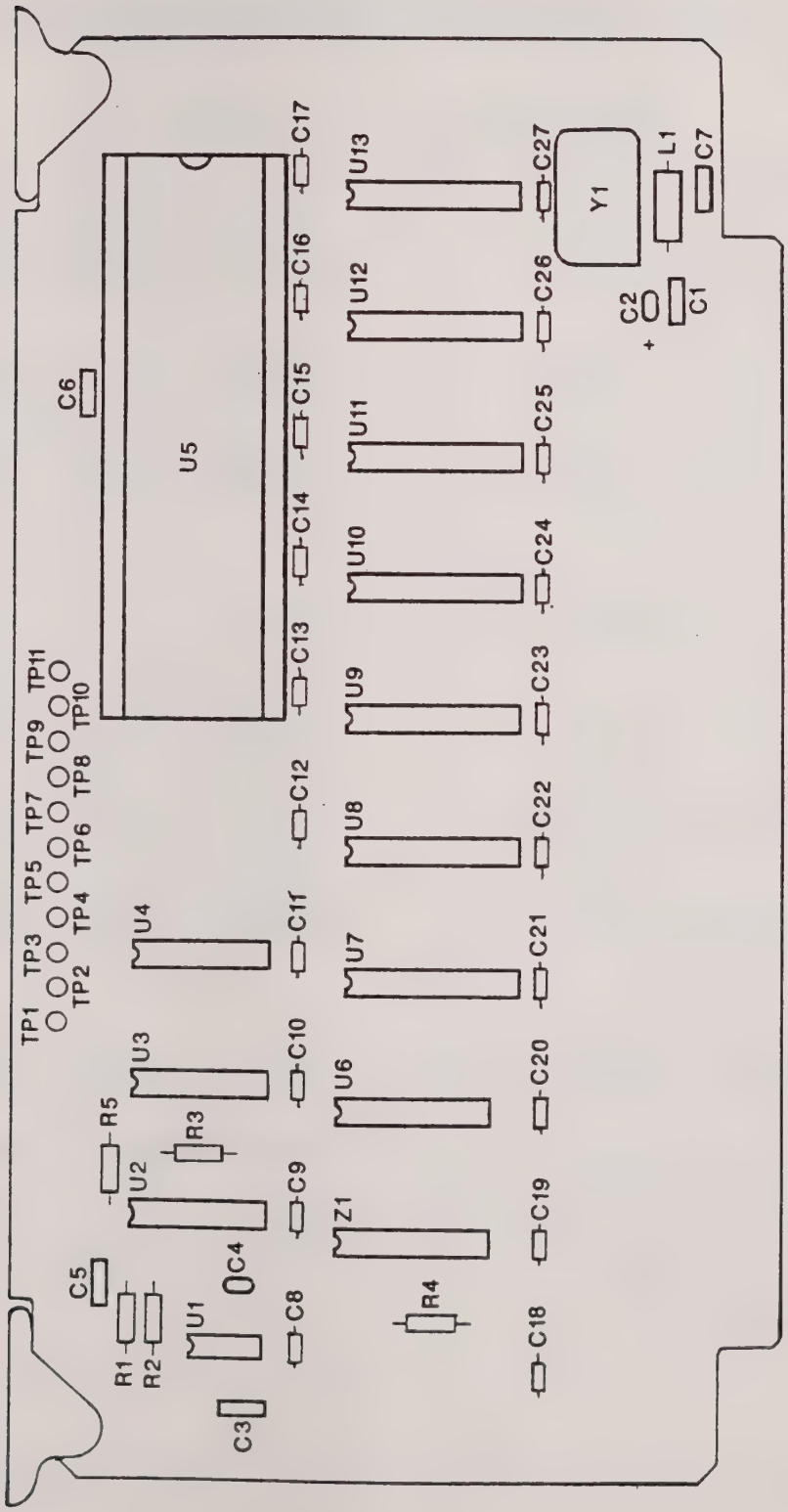


Figure 6-3. Microprocessor CCA A1 (P/N 787170 Revision F), Parts Location

Table 6-6. Replacement Parts List: Memory Circuit Card Assembly A2 - 787171-4 Revision A

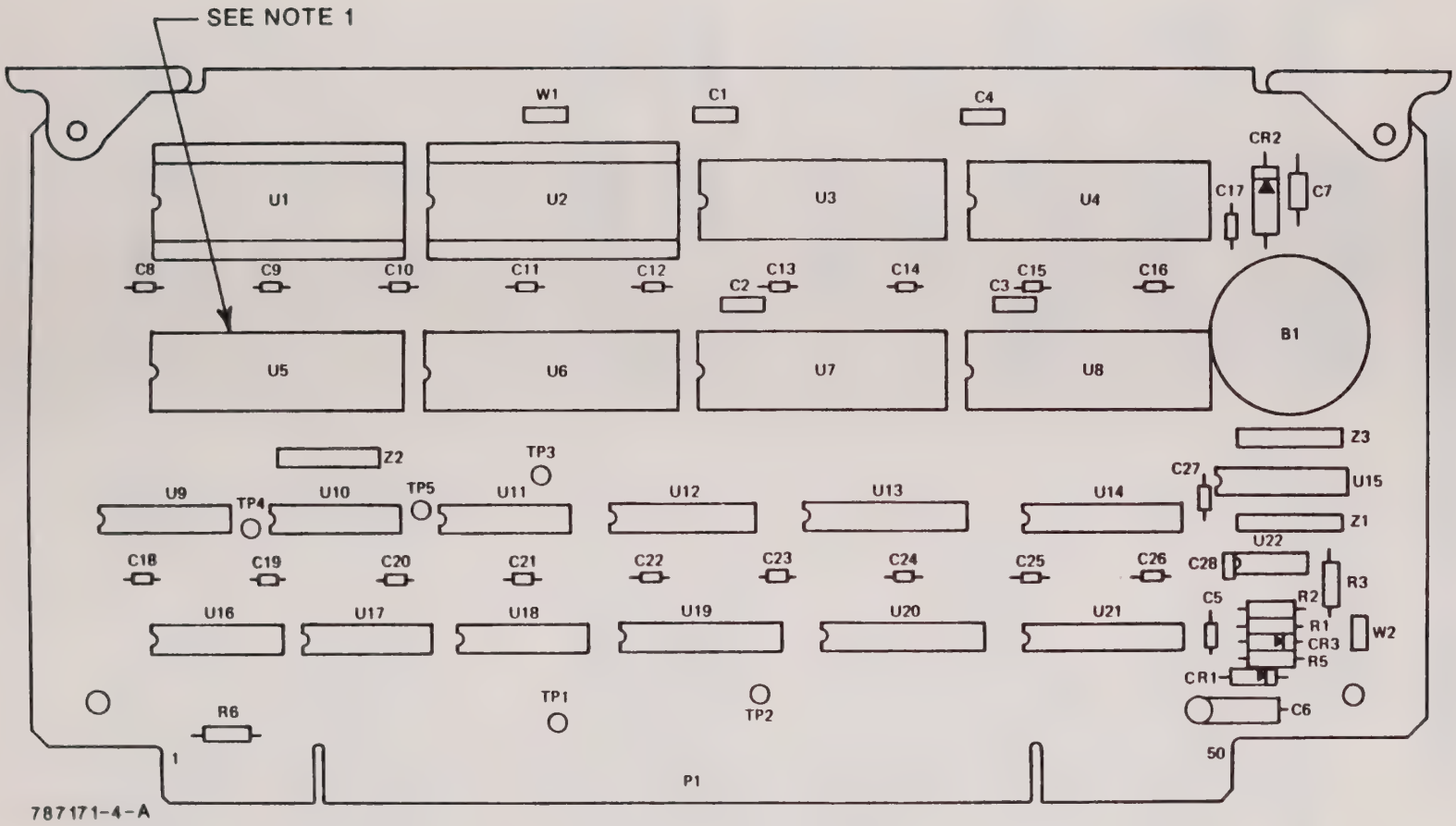
REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
B1	Battery, 2.4 V	886007	04713	MMB2.4B
C1	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	885498	DDDDD	SA105E104MAA
C2-C5	Same as C1			
C6	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C7	Capacitor, Tantalum, 1 uf, 35 V, +1%	883001	56289	150D105X9035A
C8-C28	Same as C1			
CR1	Diode, Schottky, 30 V	886005	81349	1N5818
CR2,CR3	Same as CR1			
R1	Resistor, Composition, 6.2 k, 1/4 W, ±5%	880566	01121	CB6225
R2	Resistor, Composition, 10 k, 1/4 W, ±5%	880092	01121	CB1035
R3	Resistor, Composition, 100 k, 1/4 W, ±5%	880846	01121	CB1045
R4	Not used			
R5	Resistor, Fixed, Comp., 2.7 k, 1/4 W, ±5%	880746	01121	CB2725
R6	Resistor, Composition, 3.3 k, 1/4 W, ±5%	803388	01121	CB3325
TP1	Post, P and Cont., Mod II, Machine Applied	880007	00779	87022-9
TP2-TP5	Same as TP1			

Table 6-6. Replacement Parts List: Memory Circuit Card Assembly A2 - 787171-4 Revision A (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U1	Not supplied as part of this assembly. Refer to Digital Analyzing Voltmeter Unique Parts tables 6-2 and 6-3 for proper replacement parts.			
U2	Not supplied as part of this assembly. Refer to Digital Analyzing Voltmeter Unique Parts tables 6-2 and 6-3 for proper replacement parts.			
U3	IC, RAM, 32k-8	888673	BBBBB	HM62256P-15
U4	Same as U3			
U5	Not supplied as part of this assembly. Refer to Digital Analyzing Voltmeter Unique Parts tables 6-2 and 6-3 for proper replacement parts.			
U6	Not supplied as part of this assembly. Refer to Digital Analyzing Voltmeter Unique Parts tables 6-2 and 6-3 for proper replacement parts.			
U7,U8	Not used			
U9	IC, TTL, Quad 2-Input NAND Gate	870321	26374	LS260P
U10	IC, TTL, Hex Inverter	885980	01295	74LS05N

Table 6-6. Replacement Parts List: Memory Circuit Card Assembly A2 - 787171-4 Revision A (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U11	IC, TTL, Quad 2-Input OR Gate	808898	01295	SN74LS32N
U12	IC, TTL, Dual 1 of 4 Decoder	880652	01295	SN74LS139
U13	IC, TTL, Octal Line Buffer w/Tristate Outputs	808713	18324	74LS244
U14	IC, LV, TTL, 20-Pin	886186	04713	SN74LS645
U15	IC, HC, CMOS	886352	27014	74HC126
U16	IC, TTL, Quad 2-Input NAND Buffer, w/Open Collector Output	883949	01295	SN74LS38N
U17	IC, TTL, Serial In-Parallel Out Shift Register	884560	01295	SN74LS164N
U18	IC, TTL, Dual Modulo-16 Counter	883463	07263	74LS393N
U19,U20	Same as U13			
U21	Same as U14			
U22	IC, CMOS, OP Amp	887258	32293	ICL7611DCPA
W10	Mini-Jumper	884691	22526	65474-001
W10-1, W10-2	Same as TP1			
XU1	IC Socket, DIP, 28-Pin	883951	00779	2-640362-3
XU2	Same as XU1			
XU3-XU6	Not used			
Z1	Resistor, Network, NML, 3.3 k, 6-Pin, SIP	884487	32997	4306R-101-332
Z2,Z3	Same as Z1			



NOTES: 1. U5 THROUGH U8 NOT USED.
2. U1 AND U2 ARE INSTALLED AT TOP ASSEMBLY.

Figure 6-4. Memory CCA A2 (P/N 787171-4 Revision A), Parts Location

Table 6-7. Replacement Parts List: I/O Circuit Card Assembly A3 - 787172-2 Revision D

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Ceramic, Axial Lead, 0.01 uf, 100 V, +80-20%	886812	96095	SA101E103ZAA
C2	Capacitor, Ceramic, 1 uf, 50 V, ±10%	805155	95750	CK06BX105K
C3	Same as C1			
C4	Same as C2			
C5	Capacitor, Ceramic, Axial Lead, 0.1 uf, 50 V, ±20%	885498	96095	SA105E104MAA
C6-C10	Same as C5			
C11	Same as C1			
C12	Same as C5			
C13,C14	Same as C1			
C15	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C16	Capacitor, Tantalum, 3.3 uf, 25 V, ±20%	886064	AAAAA	NDT3.3M-25VMZD
C17	Same as C16			
C18	Same as C5			
C19	Same as C1			
C20-C24	Same as C5			
C25-C28	Same as C2			
C29-C31	Same as C5			
C32	Not used			
C33-C35	Same as C5			
C36	Same as C1			

Table 6-7. Replacement Parts List: I/O Circuit Card Assembly A3 - 787172-2 Revision D (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R1	Resistor, Variable, 50 k, 1/2 W, 2k-1, Cermet	807251	32997	3299X50KOHM
R2-R4	Same as R1			
R5	Resistor, Metal Film, 127 k, 1/10 W, ±1%	808118	16299	NC4 127K
R6	Resistor, Metal Film, Special, 3.09 M, .1 W, ±1%	808905	01637	CMF-1/103.09K T1
R7	Same as R5			
R8	Resistor, Composition, 1 k, 1/4 W, ±5%	880084	01121	CB1025
R9	Resistor, Composition, 100 ohm, 1/4 W, ±5%	880077	01121	CB1015
R10	Same as R6			
SW1	Switch, DIP, 16-Pin	808582	00779	435802-9
SW2	Same as SW1			
TP1	Post, P and Cont., Mod II, Machine Applied	880007	00779	87022-9
TP2-TP12	Same as TP1			
U1	Not used			
U2	IC, Interface	885997	01295	SN75160A
U3	IC, Interface	885998	01295	SN75161A
U4	IC, DAC, 16-Bit	887896	13919	BAC1600JF
U5	Same as U4			
U6	IC, Interface	885996	01295	TMS9914A
U7	IC, TTL, Octal Transparent Latch	884513	07263	74LS373PC

Table 6-7. Replacement Parts List: I/O Circuit Card Assembly A3 - 787172-2 Revision D (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U8	Same as U7			
U9	IC, TTL, Dual JK Flip-Flop	883604	01295	SN74LS107N
U10	IC, TTL, Hex Inverter	808898	01295	SN74LS32N
U11	Same as U7			
U12	IC, TTL, 1-of-8 Decoder/ Demultiplexer	808135	01295	SN74LS138
U13	Same as U12			
U14	IC, TTL, Hex Inverter	885980	01295	74LS05N
U15	IC, LV, TTL, 20-Pin	886186	04713	SN74LS645
U16	IC, TTL, D-Type Flip-Flop w/Clear	883592	01295	ASN74LS273
U17-U19	Same as U16			
U20	IC, Amp, OP-27GZ	886028	06665	OP-27GZ
U21	Same as U20			
U22	IC, TTL, Octal Buffer/Line Driver	808713	18324	74LS244
W2,W4	Jumper, Mini, Shorting Strip	884691	22526	65474-001
W1-1,W1-2	Same as TP1			
W2-1,W2-2	Same as TP1			
W3-1,W3-2	Same as TP1			
W4-1,W4-2	Same as TP1			

Table 6-7. Replacement Parts List: I/O Circuit Card Assembly A3 - 787172-2 Revision D (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
Z1	Resistor, Network, 3.3 k, 15 Res	885964	32997	4116R-002-332
Z2	Same as Z1			
Z3	Resistor, Network, 4 Pin, 80 k, 20 k, 175 k	887897	07342	887897
Z4	Same as Z3			

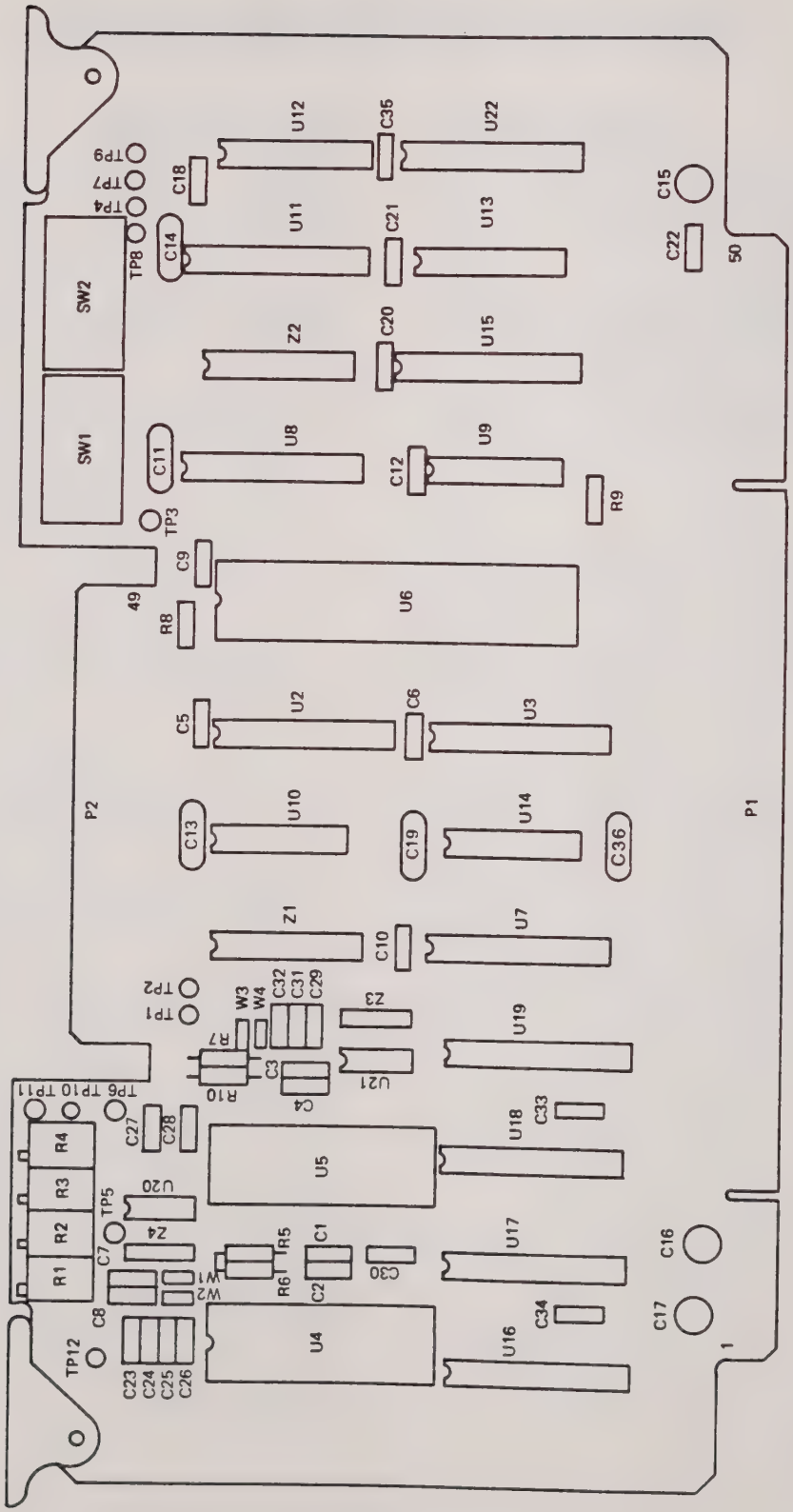


Figure 6-5. I/O CCA A3 (P/N 787172-2 Revision D), Parts Location

Table 6-8. Replacement Parts List: Timing and Control Circuit Card Assembly A4 - 787173-1 Revision E

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	886063	16299	SR215E104MAA
C2-C5	Same as C1			
C6	Capacitor, Ceramic, 0.1 uf, 50 V, +80-20%	886061	AAAAA	NCD-.01M50VZZ5V
C7-C14	Same as C6			
C15-C20	Same as C1			
C21	Capacitor, Tantalum, 1 uf, 35 V, ±10%	883001	56289	150D105X9035A
C22	Same as C6			
C23-C25	Same as C1			
C26	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25V-M-ZD
C27	Same as C6			
R1	Resistor, Composition, 11 k, 1/4 W, ±5%	802255	01121	CB6815
R2	Resistor, Composition, 18 k, 1/4 W, ±5%	802183	01121	CB1835
R3	Same as R2			
U1	IC, TTL, 1-of-16 Decoder/ Demultiplexer	884668	01295	SN74LS154N
U2	IC, TTL (ALS), Synchronous Presettable Binary Counter	886356	01295	74ALS161
U3	IC/D, TTL, Quad 2-Input AND Gate	883236	01295	SN74LS08N
U4	IC, TTL, Dual D-Type Positive Edge-Triggered Flip-Flop	883240	01295	SN74LS74N

Table 6-8. Replacement Parts List: Timing and Control Circuit Card Assembly A4 - 787173-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U5	IC, TTL, Dual Modulo-16 Counter	883463	07263	74LS393N
U6	Same as U1			
U7	IC, TTL, 13-Input NAND Gate	880842	01295	SN74S133N
U8	Same as U4			
U9	Same as U5			
U10	IC/D, MOS HT, Programmable Timer	884475	04713	MC6840CP
U11	Same as U5			
U12	Same as U4			
U13	IC, TTL, Quad 2-Input NAND Gate	808128	01295	SB74S00N
U14	IC/D, TTL, Quad Set-Reset Latch	880068	01295	SN74279
U15	IC, TTL, Quad D Flip-Flop	808889	01295	SN74S174N
U16	Same as U5			
U17	IC, XMOS, Hex Inverter	885985	01295	74HC14N
U18	IC, TTL, Hex Schmitt Trigger Inverter	883703	01295	SN74LS14N
U19	IC, TTL, 1-of-8 Decoder/ Demultiplexer	808135	01295	SN74LS138
U20	IC, TTL, Binary UP/DOWN Counter	808914	01295	SN74LS193N
U21	Same as U14			

Table 6-8. Replacement Parts List: Timing and Control Circuit Card Assembly A4 - 787173-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U22	IC, TTL, Quad 2-Input Multiplexer	880699	01295	SN745S157
U23,U24	Same as U22			
U25	IC, TTL, Quad 2-Input Schmitt Trigger NAND Gate	883982	01295	ASN74LS132N
U26	IC, TTL, Quad Bus Buffer Gate	808342	01295	SN74LS125N
U27	IC, TTL, Quad 2-Input NAND Gate	885981	01295	74LS03N
U28	IC/D, TTL, Quad Set-Reset Latch	883239	01295	SN74LS279N
U29	Same as U26			
U30-U32	IC, TTL, 8-Bit Register w/Clear	883634	01295	SN74LS273N
U33	IC, LV TTL, 20-Pin	886186	04713	SN74LS645
XU14	IC, Socket	808197	00779	2-640358-3

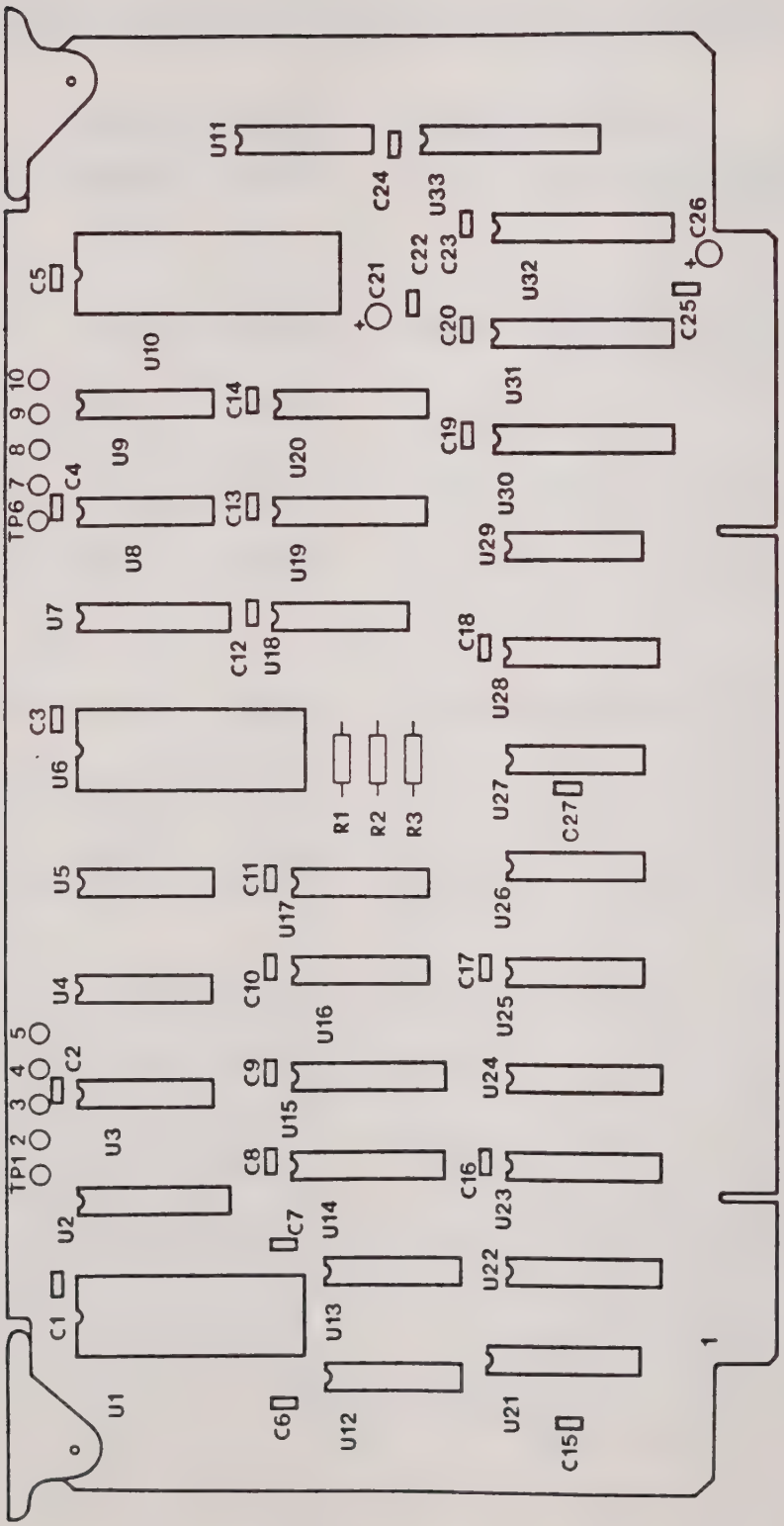


Figure 6-6. Timing and Control CCA A4 (P/N 787173-1 Revision E), Parts Location

Table 6-9. Replacement Parts List: Phase-Locked Loop Circuit Card Assembly A5 - 787192-1 Revision E

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
BB1	Buss Bar, 10-Pos	886004	19648	SU10.75.3.1
BB2,BB3	Same as BB1			
C1	Capacitor, Ceramic, 39 pf, 200 V, ±10%	808624	81349	CK05BX390K
C2	Capacitor, Ceramic, 24 pf, 200 V, ±10%	886394	51406	CK05BX240K
C3	Capacitor, Metal Film, 180 pf, 200 V, ±10%	808103	81349	CK05BX181K
C4	Capacitor, Ceramic, 820 pf, 200 V, ±10%	886395	51406	CK05BX821K
C5	Capacitor, Ceramic, 560 pf, 200 V, ±10%	805283	81349	CK05BX561K
C6	Capacitor, Ceramic, 1800 pf, 100 V, ±10%	886397	51406	CK06BX182K
C7	Capacitor, Ceramic, 0.0056 uf, 200 V, ±10%	805957	81349	CK06BX562K
C8	Capacitor, Ceramic, 0.018 uf, 100 V, ±10%	805281	95750	CK06BX183K
C9	Same as C7			
C10	Same as C8			
C11	Capacitor, Ceramic, 0.056 uf, 100 V, ±10%	805454	81349	CK06BX563K
C12	Capacitor, Ceramic, 0.18 uf, 100 V, ±10%	886402	51406	CK06BX184K
C13	Capacitor, Ceramic, 0.22 uf, 50 V, ±10%	882456	81349	CKR06BX224KP
C14	Capacitor, Ceramic, 1 uf, 50 V, ±10 %	882876	81349	CKR06BX105KP

Table 6-9. Replacement Parts List: Phase-Locked Loop
Circuit Card Assembly A5 - 787192-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C15	Capacitor, El, Tantalum, 2.2 uf, 20 V, ±20%	884160	25088	ST822A225M020N
C16	Capacitor, Tantalum, 4.7 uf, 25 V, ±20%	886059	AAAAA	NDT4.7M25VMZD
C17	Capacitor, Ceramic, 0.015 uf, 100 V, ±10%	806367	81349	CK06BX153K
C18	Same as C11			
C19	Capacitor, Ceramic, 3900 pf, 200 V, ±10%	886400	51406	CK06BX392K
C20	Capacitor, Ceramic, 22 pf, 200 V, ±10%	886399	51406	CK05BX220K
C21	Capacitor, Ceramic, 0.1 uf, 50 V, ±10%	807730	81349	CK05BX104K
C22	Capacitor, Ceramic, 0.47 uf, 50 V, ±10%	886398	54407	CP487
C23	Capacitor, Ceramic, 0.18 uf, 100 V, ±10%	886402	51406	CK06BX184K
C24	Same as C21			
C25	Same as C20			
C26	Same as C14			
C27,C28	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25V-MZD
C29,C30	Capacitor, Tantalum, 3.3 uf, 25 V, ±20%	886064	AAAAA	NDT3.3M-25V MZD
C31-C42	Capacitor, Ceramic, Axial Lead, 0.1 uf, 50 V, ±20%	885498	96095	SA105E104MAA
C43	Same as C27			
C44	Same as C31			
CR1	Not used			

Table 6-9. Replacement Parts List: Phase-Locked Loop
Circuit Card Assembly A5 - 787192-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
CR2	Diode, Sig. In	808974	01295	1N4148
CR3-CR8	Same as CR2			
CR9	Diode, Zener, 2.4 V	888287	04713	1N5221B
Q1	Transistor, MOSFET, TO-92 Case	886370	17896	VN10KM
Q2,Q3	Same as Q1			
R1	Resistor, Metal Film, 19.1 k, 1/10 W, ±1%	808370	01121	CC1912F
R2	Resistor, Metal Film, 5.90 k, 1/20 W, ±1%	886379	91637	EMF-50-100-5.90K
R3,R4	Not used			
R5	Resistor, Composition, 1 k, 1/8 W, ±5%	880694	01121	BB1025
R6	Resistor, Metal Film, 4.12 k, 1/20 W, ±1%	886373	91637	EFM-50-100-4.12K
R7	Resistor, Metal Film, 20 k, 1/10 W, ±0.5%	808226	91637	CMF-55,T-2
R8	Resistor, Composition, 82 ohm, 1/8 W, ±5%	887711	01121	RCR05G820JS
R9	Resistor, Metal Film, 10.0 k, 1/20 W, ±1%	886380	91637	EMF-50-100-10K
R10	Same as R6			
R11	Resistor, Metal Film, 3.01 k, 1/20 W, ±1%	886374	91637	EMF-50-100-3.01K
R12	Resistor, Metal Film, 6.98 k, 1/20 W, ±1%	886393	91637	EMF-50-100-6.98K
R13	Resistor, Metal Film, 24.3 k, 1/20 W, ±1%	886383	91637	EMF-50-100-24.3K
R14	Resistor, Composition, 510 ohm, 1/4 W, ±5%	880082	01121	CB5115

Table 6-9. Replacement Parts List: Phase-Locked Loop
Circuit Card Assembly A5 - 787192-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R15	Same as R9			
R16	Resistor, Metal Film, 3.16 k, 1/20 W, ±1%	886375	91637	EMF-50-100-3.16K
R17	Resistor, Metal Film, 1.00 k, 1/20 W, ±1%	886372	91637	EMF-50-100-1K
R18	Resistor, Metal Film, 316 ohm, 1/20 W, ±1%	886371	91637	EMF-50-100-316OHM
R19	Resistor, Metal Film, 316 k, 1/20 W, ±1%	808640	92637	EMF-50-100-316K
R20	Resistor, Metal Film, 100 k, 1/20 W, ±1%	808657	91637	EMF-50-100-100K
R21	Resistor, Metal Film, 31.6 k, 1/20 W, ±1%	886384	91637	EMF-50-100-31.6K
R22	Same as R9			
R23	Not used			
R24	Same as R19			
R25	Same as R20			
R26	Same as R21			
R27	Same as R19			
R28	Resistor, Metal Film, 158 k, 1/20 W, ±1%	808650	91637	EMF-50-100-158K
R29	Resistor, Metal Film, 49.9 k, 1/20 W, ±1%	886387	91637	EMF-50-100-49.9K
R30	Resistor, Metal Film, 15.8 k, 1/20 W, ±1%	886382	91637	EMF-50-100-15.8K
R31	Resistor, Metal Film, 4.99 k, 1/20 W, ±1%	886377	91637	EMF-50-100-4.99K
R32	Resistor, Metal Film, 475 k, 1/20 W, ±1%	886389	91637	EMF-50-100-475K

Table 6-9. Replacement Parts List: Phase-Locked Loop Circuit Card Assembly A5 - 787192-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R33	Resistor, Metal Film, 150 k, 1/20 W, ±1%	886388	91637	EMF-50-100-150K
R34	Resistor, Metal Film, 47.5 k, 1/20 W, ±1%	886386	91637	EMF-50-100-47.5K
R35	Resistor, Metal Film, 15.0 k, 1/20 W, ±1%	886381	91637	EMF-50-100-15.0K
R36	Same as R5			
R37	Resistor, Metal Film, 33.2 k, 1/20 W, ±1%	886385	91637	EMF-50-100-33.2K
R38	Same as R19			
R39	Resistor, Metal Film, 3.32 k, 1/20 W, ±1%	886376	91637	EMF-50-100-3.32K
R40	Same as R17			
R41	Resistor, Metal Film, 1.00 Meg, 1/20 W, ±1%	886391	91637	EMF-50-100 1.0M
R42	Same as R19			
R43	Same as R20			
R44	Same as R21			
R45	Same as R41			
R46	Same as R19			
R47	Same as R20			
R48	Same as R21			
R49	Resistor, Metal Film, 499 k, 1/20 W, ±1%	886390	91637	EMF-50-100-499K
R50	Same as R28			
R51	Same as R29			
R52	Same as R30			

Table 6-9. Replacement Parts List: Phase-Locked Loop Circuit Card Assembly A5 - 787192-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R53	Resistor, Metal Film, 1.5 Meg, 1/10 W, ±1%	886392	91637	EMF-55-100-1.5M
R54	Same as R32			
R55	Same as R33			
R56	Same as R34			
R57	Same as R5			
R58	Not used			
R59	Resistor, Composition, 10 k, 1/8 W, ±5%	880830	01121	BB1035
R60-R62	Same as R59			
R63	Resistor, Composition, 1 M, 1/8 W, ±5%	880833	01121	BB1055
R64	Resistor, Composition, 5.1 k, 1/8 W, ±5%	880576	01121	BB5125
R65	Same as R59			
R66	Resistor, Variable, 20 k, 1/2 W, ±10%	808241	32997	3299X203
R67	Resistor, Variable, 100 k, 1/2 W, 25-Turn	808428	32997	3299X-1-104
R68	Resistor, Composition, 3.3 k, 1/8 W, ±5%	805103	81349	RC05GF332J
U1	IC, TTL, Hex Buffer/Driver	808140	01295	SN7407N
U2	IC, Data Converter	808886	02735	CD4051BE
U3,U4	Same as U2			
U5	IC, Data Converter	808227	02735	CB4052BE
U6-U9	Same as U5			
U10	IC, TTL, Hex Buffer/Driver	883497	01295	SN74LS153N

Table 6-9. Replacement Parts List: Phase-Locked Loop Circuit Card Assembly A5 - 787192-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U11	IC, TTL, Quad Bus Buffer	808342	01295	SN74LS125N
U12	IC, CMOS, Phase-Locked Loop	888289	27014	MM74HC4046N
U13	IC, CMOS, 2-Channel Analog Multiplexer	808304	02735	CD4053BE
U14	IC, CMOS, Hex Inverter	888290	02735	CD74HC4049E
U15	IC, TTL, Dual D-Type Edge Triggered Flip-Flop	883240	01295	SN74LS74N
U16	IC, CMOS, 3-Input NOR Gate (Triple)	888292	02735	CD74HC27
U17	IC, CMOS, High Speed Presettable Down Counter	888291	02735	CD4MC40103E
U18	Same as U17			
U19	IC, OP Amp, 8-Pin, DIP	886495	06665	OP16-EZ
U20	Same as U19			
U21	IC, TTL, Quad 2-Input Multiplexer	883460	07263	74LS157N
U22	IC, -5 V Voltage Regulator	884919	27014	70L05ACZ
U23	IC, Amplifier	885026	01295	TL082ACP
Z1	Resistor, Network, NML, 1 k, 8-P, 7 Res., ±2%	808371	56289	420CH102X2PD

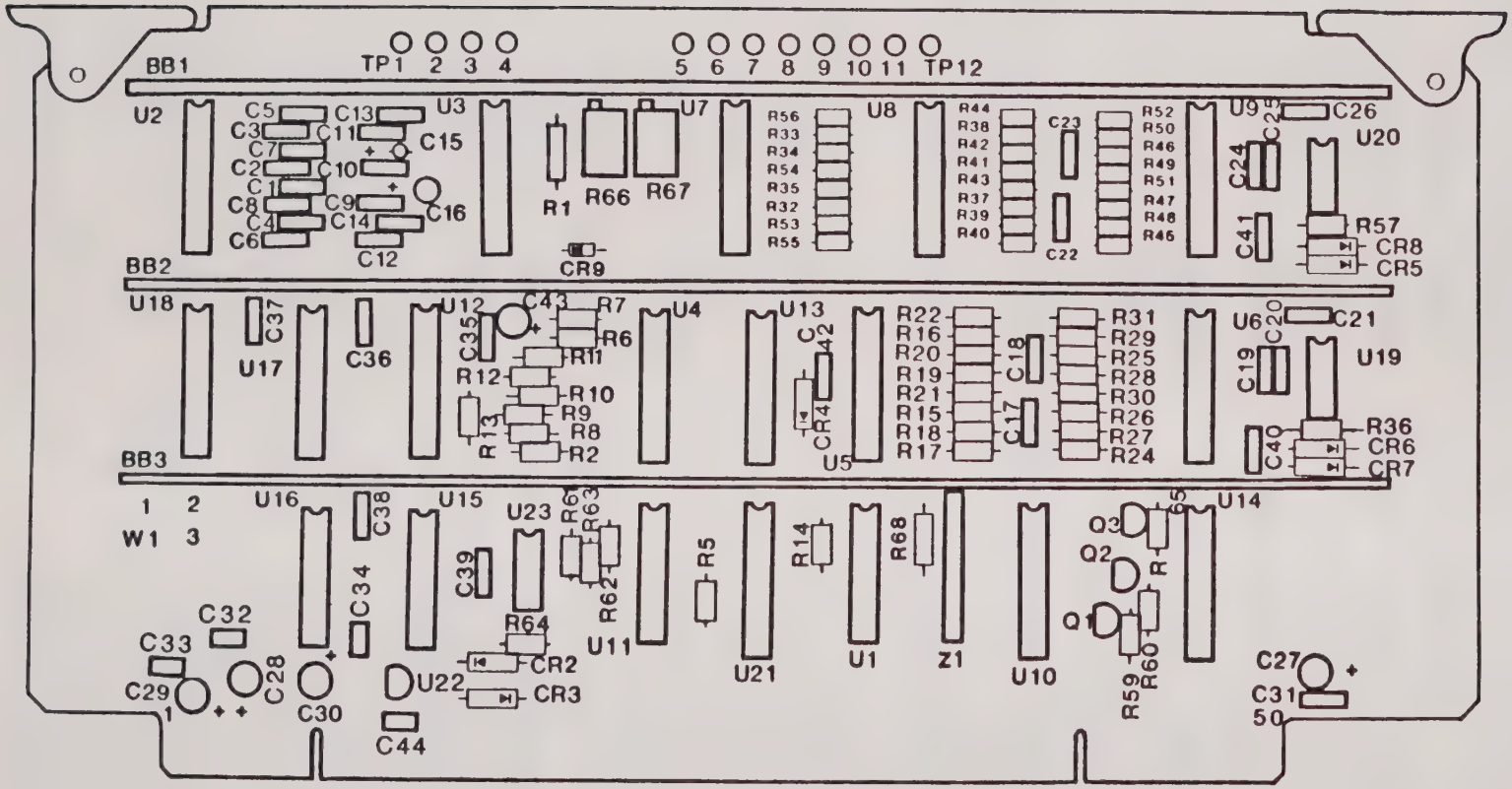


Figure 6-7. Phase-Locked Loop CCA A5 (P/N 787192-1 Revision E), Parts Location

Table 6-10. Replacement Parts List: Accumulator Circuit Card Assembly A6,A7 - 787193-1 Revision A

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C2	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	886063	16299	SR215E104MAA
C3-C15	Same as C2			
TP1	Post	880007	00779	87022-9
TP2-TP14	Same as TP1			
U1	IC, TTL, Quad 2-Input Multiplexer	883590	01295	SN74LS158
U2	IC, TTL, 4-Bit Binary Full Adder (w/fast carry)	883593	01295	SN74LS283
U3	Same as U1			
U4	Same as U2			
U5	Same as U1			
U6	Same as U2			
U7	Same as U1			
U8	Same as U2			
U9	Same as U1			
U10,U11	Same as U2			
U12	IC, TTL, Octal D-Type Flip-Flop	808576	01295	SN74LS374N
U13	IC, RAM, 2 k x 8, 120 ms	886097	52464	MSM5128RS-62
U14	PAL, Overload Indicator	887742	07342	887742
U15	IC, CMOS, 8-Bit Latched Shift Register	885986	04713	74HC595N
U16	IC, TTL, Octal Buffer/Line Driver	885098	01295	SN74LS240

Table 6-10. Replacement Parts List: Accumulator Circuit Card Assembly A6,A7 - 787193-1 Revision A (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U17	Same as U16			
U18	Resistor, Network, SIP, 1 k, 6 Pos, 5 Res, ±2%	885535	32997	430GR-101-102
U19	Same as U12			
U20	Same as U13			
U21	Same as U13			
U22	Same as U12			
U23	Same as U15			
U24	IC, XMOS, Hex Inverter	885985	01295	74HC14N
U25	IC, TTL, Octal Latch, Schottky	886738	01295	745273N
U26	IC, LV, TTL, 20-Pin	886186	04713	SN74LS645
U27	Same as U26			
XU14	Socket, Int Ckt, DIP, 20-Pin	808408	00779	2-640464-3

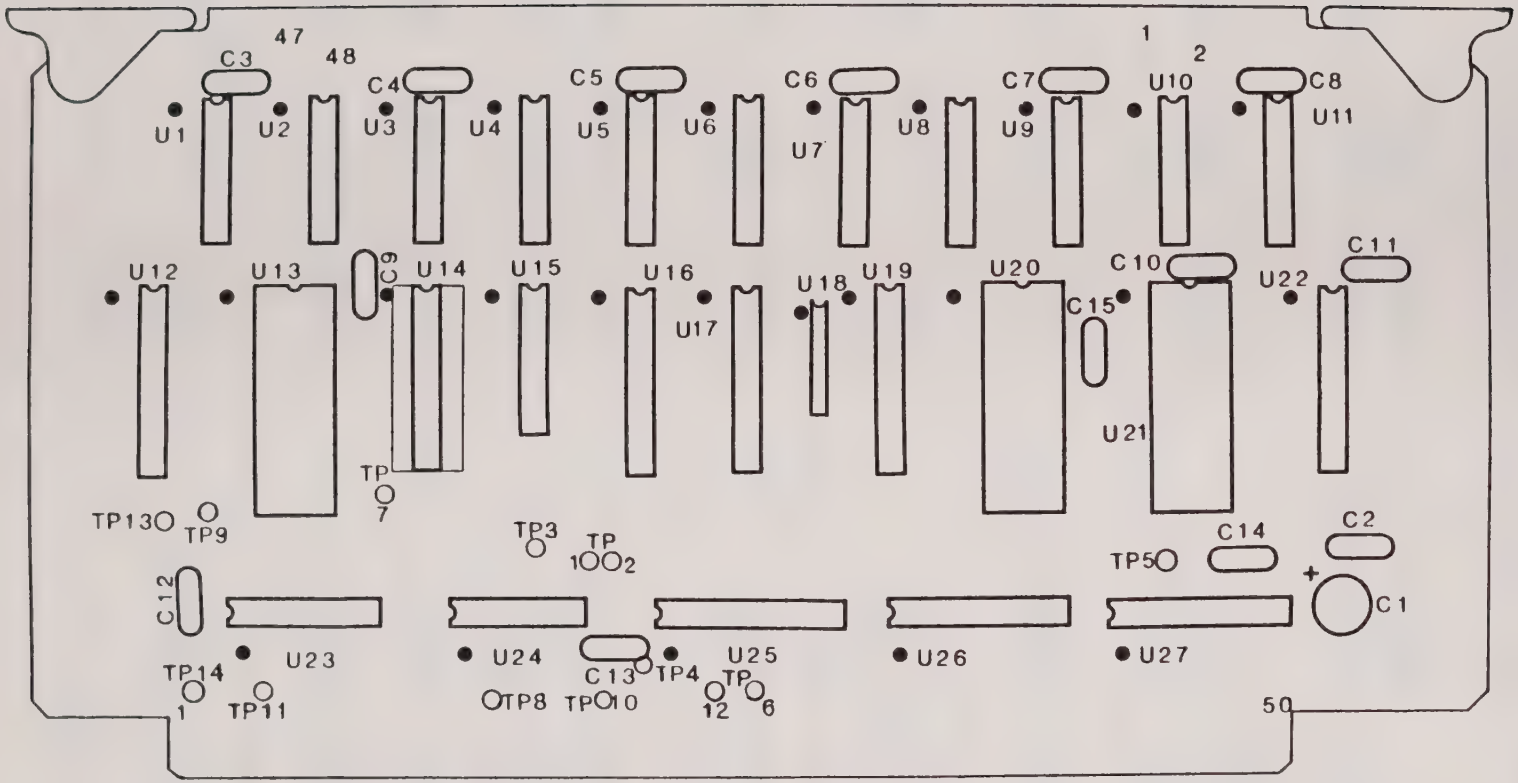


Figure 6-8. Accumulator CCA A6/A7 (P/N 787193-1 Revision A), Parts Location

Table 6-11. Replacement Parts List: Auto Calibration
Circuit Card Assembly A8 - 787274-2 Revision A

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Ceramic, Axial Lead, 0.1 uf, 50 V, ±20%	886063	16299	SR215E104MAA
C2-C20	Same as C1			
C21	Capacitor, Ceramic, 1500 pf, 100 V, ±10%	805357	72982	8133-000-W5R0152K
C22	Same as C21			
C23	Capacitor, Tantalum, 3.3 uf, 25 V, ±20%	886064	AAAAA	NDT3.3M-25VMZD
C24-C26	Same as C23			
C27	Capacitor, Ceramic 47 pf, 200 V, ±10%	808622	81349	CK05BX470K
C28	Same as C27			
C29	Capacitor, Tantalum, 20 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C30	Same as C29			
C31	Capacitor, Ceramic, 0.47 uf, 50 V, ±10%	882449	81349	CKR06BX474KP
C32	Capacitor, Ceramic, 0.047 uf, 100 V, ±1%	883330	81349	CK06BX473K
C33	Capacitor, Ceramic, 0.0047 uf, 50 V, ±10%	883359	81349	CK05BX472K
C34	Capacitor, Ceramic, 470 pf, 200 V, ±10%	883364	81349	CK05BX471K
C35	Same as C23			
C37	Capacitor, Ceramic, 1200 pf, 100 V, ±10%	884839	72982	CK05BX122K
C38	Capacitor, Ceramic, 560 pf, 200 V, ±10%	805283	81349	CK05BX561K

Table 6-11. Replacement Parts List: Auto Calibration
Circuit Card Assembly A8 - 787274-2 Revision A (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C39	Capacitor, Ceramic, 390 pf, 200 V, ±10%	805284	81349	CK05BX391K
C40-C43	Same as C1			
C44	Capacitor, Solid Tantalum, 22 uf, 10 V, ±10%	886176	AAAAA	MDT47M10VM
CR1	Diode, Sig., 1N6263	883449	07980	5082-HSCH-1001
CR2-CR4	Same as CR1			
CR5	Rectifier, Schottky, 125 V, 1 A	886006	81349	1N5805
CR6	Same as CR5			
J1	Not used			
J2	Header, 2-Pin	886058	51306	TSW-136-09-T-S-RP
R1	Resistor, Metal Film, 15 k, 1/8 W, ±1%	806538	16299	NC4
R2	Same as R1			
R3	Resistor, Metal Film, 1 k, 1/10 W, ±1%	808213	16299	NC55
R4	Resistor, Metal Film, 5.62 k, 1/10 W, ±1%	808231	16299	NC555621F
R6	Resistor, Variable, 500 ohm, 25 Turn, ±10%	807655	32997	3299X-1-501
R7	Resistor, Fixed, Metal Film, 4.75 k, 100 PPM TC, ±1%	886175	91637	CMF-55D4751F
R8	Resistor, Variable, Pot, 100 k	808428	32997	3299X-1-104
R9	Same as R8			

Table 6-11. Replacement Parts List: Auto Calibration
Circuit Card Assembly A8 - 787274-2 Revision A (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R10	Resistor, Metal Film, 80.6 k, 1/10 W, ±1%	808242	16299	NC558062F
R11	Resistor, Metal Film, 13.3 k, 1/10 W, ±1%	807633	91637	MF1/10,13.3 K,1%
R12	Resistor, Fixed, Metal Film, 51.1 k, 1/8 W, ±1%	806550	16299	RN55C5112F
R13	Resistor, Variable, 5 k, 1/2 W, 25 Turn, Cermet	807250	32997	3299X-5KOHM
R14-R16	Same as R3			
R17	Resistor, Metal Film, 8.06 k, 1/10 W, ±1%	807016	81349	RN55D8061F
R18	Resistor, Composition, 10 ohm, 1/4 W, ±5%	883106	01121	CB1005
R19	Same as R18			
R20	Resistor, Composition, 1 k, 1/4 W, ±5%	880084	01121	CB1025
R21	Same as R20			
R22	Resistor, Composition, 10 k, 1/4 W, ±5%	880092	01121	CB1035
R23	Resistor, Composition, 62 k, 1/4 W, ±5%	802082	01121	CB6235
SW1	Switch, Misc., DIP, 16-Pin, 8 Piano	808582	81073	76PSB08S
SW2	Switch, DPDT, Rt. Angle, PC Mount	886739	70255	TSS2ING-RA
TP1	Post, P and Cont., Mod II, Machine Applied	880007	00779	87022-9
TP2-TP5	Same as TP1			

Table 6-11. Replacement Parts List: Auto Calibration Circuit Card Assembly A8 - 787274-2 Revision A (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U1	IC, Reg., Adj, 14-Pin, DIP	886173	04713	MC14682
U2	IC, Function Generator	886172	52062	XR8038N
U3	IC, Analog Switch	886082	17856	DG212CJ
U4	IC/L Op Amp, St, NML	884427	01295	TL081CP
U5	IC, Amp, OP-37GZ	886029	06665	OP-37GZ
U6	IC/L, Op Amp, St, NML	808302	12040	LM311N
U7	IC, TTL, Quad D Flip-Flop	883603	01295	SN74LS175
U8	IC, DAC, 12-Bit, Buffered Multiplying	886033	24355	AD7545JN
U9	Same as U8			
U10	IC, TTL, Octal Buffer/Line Driver	885098	01295	SN74LS240
U11	IC, Amp, OP-27GZ	886028	06665	OP-27GZ
U12	Same as U11			
Z1	Resistor, Network, 3.3 k, 9 Res.	886057	01121	110A332

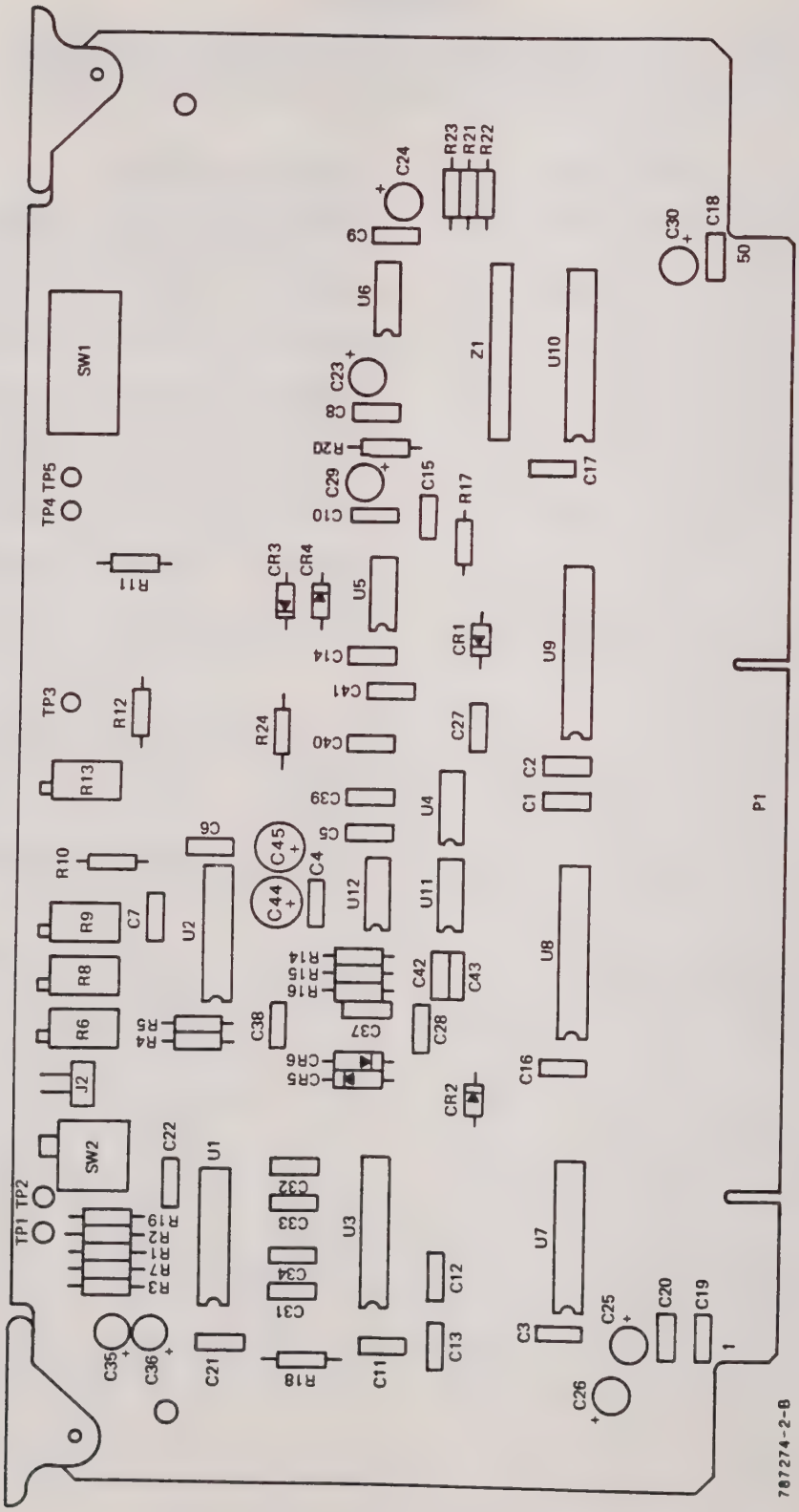


Figure 6-9. Auto Calibration CCA A8 (P/N 787274-2 Revision B), Parts Location

Table 6-12. Replacement Parts List: A/D Converter Circuit Card Assembly A9,A12 - 787664 Revision E

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Ceramic, 0.01 uf, 50 V, +80-20%	886061	AAAAA	NCD-.01M50VZZ5V
C2	Same as C1			
C3	Not used			
C4	Not used			
C5-C8	Same as C1			
C9	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C10,C11	Same as C9			
C12-C14	Same as C1			
C15	Capacitor, Mica, 47 pf, 500 V, ±5%	886079	81349	M04EC470J
C16,C17	Same as C1			
C18	Not used			
C19,C20	Same as C1			
C21	Capacitor, Ceramic, 680 pf, 200 V, ±10%	807627	81349	CK05BX681K
C22	Capacitor, Ceramic, 270 pf, 200 V, ±10%	885595	81349	CKR05BX271KP
C23	Capacitor, Ceramic, 0.0022 uf, 100 V, ±10%	882037	81349	CK06BX222K
C24-C28	Same as C1			
C29	Capacitor, Tantalum, 4.7 uf, 25 V, ±20%	886059	AAAAA	NDT4.7M25VMZD
C30	Same as C29			
C31,C32	Same as C9			

Table 6-12. Replacement Parts List: A/D Converter
Circuit Card Assembly A9,A12 - 787664 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C33	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	886063	16299	SR215E104MAA
C34-C36	Same as C33			
C37,C38	Same as C1			
C39	Not used			
C40	Capacitor, Ceramic, 1.0 uf, 50 V, ±5%	886073	81349	CK06BX105J
C41,C42	Same as C40			
C43,C44	Same as C33			
C45	Capacitor, Ceramic, 0.39 uf, 50 V, ±5%	886076	81349	R055C394JAA
C46	Same as C40			
C47	Capacitor, Ceramic, 0.056 uf, 100 V, ±10%	805454	81349	CK06BX563K
C48,C49	Same as C33			
C50,C51	Same as C9			
C52	Same as C40			
C53	Capacitor, Ceramic, 560 pf, 200 V, ±10%	805283	81349	CK05BX561K
C54-C56	Same as C1			
C100	Capacitor, Ceramic 27 pf, 200 WVdc, ±10%	808401	72982	CK05BX270K
C101	Same as C22			
CR1	Rectifier, Schottky, 125 V, 1A	886006	81349	N5805
CR2	Same as CR1			

Table 6-12. Replacement Parts List: A/D Converter
Circuit Card Assembly A9,A12 - 787664 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
CR3	Diode, Sig.	882195	81349	AN1N914
CR4	Same as CR3			
K1	Relay, Form C, 5 Coil, DIP	886719	95348	847C-1/-2
R1	Resistor, Composition, 2 k, 1/4 W, ±5%	880086	01121	CB2025
R2	Resistor, Composition, 510 ohm, 1/4 W, ±5%	880082	01121	CB5115
R3	Resistor, Composition, 1.1 k, 1/4 W, ±5%	802415	01121	CB1125
R4	Not used			
R5	Not used			
R6	Resistor, Metal Film, 51 k, 1/8 W, ±1%	806550	16299	RN55C5112F
R7	Resistor, Variable, 50 k, 1/2 W, 25-Turn, Cermet	807251	32997	3299X50KOHM
R8	Resistor, Metal Film, 10 ohm, 1/10 W, ±.1%	808240	16299	RN55D10R0B
R9	Resistor, Variable, 500 ohm, 25 Turn, ±10%	807655	32997	3299X-1-501
R10	Resistor, Metal Film, 64.9 k, 1/10 W, ±1%	807425	81349	N55D6492F
R11	Resistor, Metal Film, 2.37 k, 1/10 W, ±1%	886723	81349	N55D2371F
R12	Resistor, Metal Film, 1.5 k, 1/10 W, ±1%	807537	81349	N55D1501F
R13	Resistor, Metal Film, 1 k, 1/10 W, ±1%	808213	16299	NC55
R14,R15	Same as R1			

Table 6-12. Replacement Parts List: A/D Converter Circuit Card Assembly A9,A12 - 787664 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R16	Resistor, Composition, 1 M, 1/4 W, ±5%	880100	01121	CB1055
R17	Resistor, Fixed, Comp-K ohm, 160 k, 1/4 W	803995	01121	CB1645
R18	Resistor, Fixed, 69.8 k, 1/8 W, ±1%	885979	81349	N55D69R8F
R19	Resistor, Composition, 1 k, 1/4 W, ±5%	880084	01121	CB1025
R20	Resistor, Composition, 5.6 k, 1/4 W, ±5%	801983	01121	CB5625
R21	Same as R20			
R22	Resistor, Composition, 470 ohm, 1/4 W, ±5%	880567	01121	CB4715
R23	Same as R22			
R24,R25	Same as R20			
R26,R27	Same as R22			
R28	Same as R1			
R29	Resistor, Composition, 3.9 k, 1/4 W, ±5%	801409	01121	CB3925
R30	Same As R1			
R31	Same as R2			
R32	Same as R19			
R33	Same as R3			
R34	Same as R19			
R35	Not used			
R36	Resistor, Composition, 33 k, 1/4 W, ±5%	880097	01121	CB3335

Table 6-12. Replacement Parts List: A/D Converter
Circuit Card Assembly A9,A12 - 787664 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R37	Resistor, Variable, 5 k, 1/2 W, 25 Turn, Cermet	807250	32997	3299X-5KOHM
R38	Same as R29			
R39	Same as R22			
R40	Same as R20			
R41	Resistor, Variable, 1 k, 1/2 W, 25 Turn, Cermet	807296	32997	3299K-1-102
R42	Resistor, Metal Film, 4.22 k, 1/10 W, ±1%	808100	91637	MF-1/104.22K 1%
R43	Resistor, Metal Film, 634 ohm, 1/10 W, ±1%	887664	91637	MF-1/10 6340HM 1%
R44	Resistor, Metal Film, 732 ohm, 1/10 W, ±1%	808154	01121	CB1015
R45	Same as R13			
R46	Not used			
R47	Resistor, Composition, 2.2 k, 1/4 W, ±5%	880670	01121	CB2225
R48	Same as R47			
R49,R50	Same as R22			
R51	Not used			
R52	Not used			
R53	Resistor, Composition, 7.5 M, 1/4 W, ±5%	807102	01121	CB7555
R54	Same as R53			
R55	Resistor, Composition, 10 k, 1/4 W, ±5%	806813	81349	RCR07GF103JS

Table 6-12. Replacement Parts List: A/D Converter
Circuit Card Assembly A9,A12 - 787664 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R56	Resistor, Composition, 270 k, 1/4 W, ±5%	804400	01121	CB2745
R57,R58	Same as R56			
R59	Resistor, Composition, 100 ohm, 1/4 W, ±1%	880077	01121	CB1015
R60	Same as R59			
R61	Not used			
R62	Not used			
R63	Not used			
R64	Not used			
R65	Same as R1			
R66	Same as R22			
R67	Same as R59			
R68	Resistor, Metal Film, 15 k, 1/8 W, ±1%	806538	16299	NC4
R69	Not used			
R70	Resistor, Carbon, 5.1 M, 1/4 W, ±5%	806371	01121	RC07GF515J
R71	Potentiometer, 10 k	807507	32997	3299X-1-103
SW1	Switch, DPDT, Rt. Angle, PC Mount	886739	70255	TSS21NG-RA
TP1	Post, P and Cont., Mod II, Machine Applied	880007	00779	87022-9
TP2-TP19	Same as TP1			
U1	IC, Amp, OP-37GZ	886029	06665	OP-37GZ
U2	IC, Amplifier	886051	34371	HA1-5320-2
U3	IC, A/D Converter, 12-Bit	888135	13919	ADC-806CM

Table 6-12. Replacement Parts List: A/D Converter Circuit Card Assembly A9,A12 - 787664 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U4	IC, TTL, Quad 2-Input NAND Gate	808137	01295	SN74LS00N
U5	IC, Analog Switch	886030	17856	DG509ACJ
U6	IC, Dual Darlington Driver	886050	80183	ULN2061M
U7	IC/L, Op Amp, St, NML	808302	12040	LM311N
U8	IC, Interface Optocoupler	887665	28480	HCPL2400
U9	IC, Interface	886048	28480	HCPL2630
U10	Same as U9			
U11	IC, Interface	885991	58361	MCT6
U12	Same as U11			
U13	IC, TTL	870313	07263	96S02PC
U14	IC/L, Op Amp St, NML	808211	12040	LF356N
U15	IC, TTL, Quad Bus Buffer Gate	808342	07263	74LS125APC
U16	Same as U11			
U17	Same as U9			
U18	IC/L, Dif Comp St, NML	884448	81349	M393N
U19	IC, Quad Op Amp	887660	13919	OPA404BG
U20	IC, Linear Quad Analog Switch	808733	12040	LF13333N
U21	Same as U8			
Z1	Resistor, Network, 1 k, 2 k, 4 k	885349	07342	885349
Z2	Resistor, Network, 1 k, 3 k	885352	07342	885352
Z3	Resistor, Network, 470 ohm, 7 Res	886044	01121	108A471
Z4	Same as Z3			

Table 6-12. Replacement Parts List: A/D Converter Circuit Card Assembly A9,A12 - 787664 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
Z5	Resistor, Network, NML PRCN, 10 k Pair	808859	07342	808859
Z6	Resistor, Network, 4 P, 10 k, 10 k, 5 k	887526	07342	887526

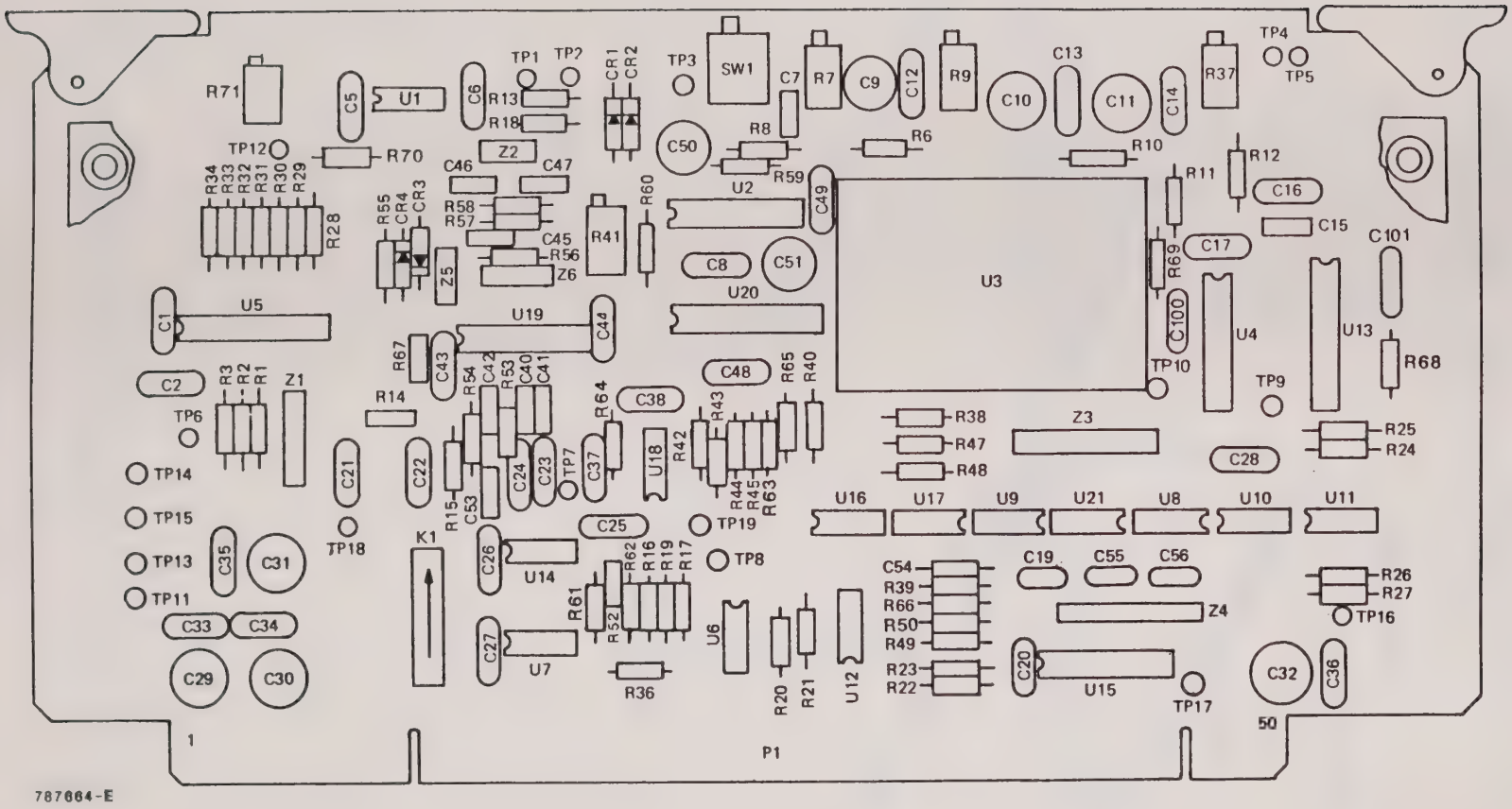


Figure 6-10. A/D Converter CCA A9/A12 (P/N 787664 Revision E), Parts Location

Table 6-13. Replacement Parts List: Filter Circuit Card Assembly A10, A13 - 787176-1 Revision B

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
A10,A13	Filter, 10 Hz-100 kHz	787176	07342	787176
	Shield	299115	07342	299115
	Shield	299116	07342	299116

NOTE

This circuit card assembly is a proprietary item and therefore no parts breakdown or schematic diagram is supplied for it. Maintenance of this circuit card assembly is performed at the manufacturer's facility.

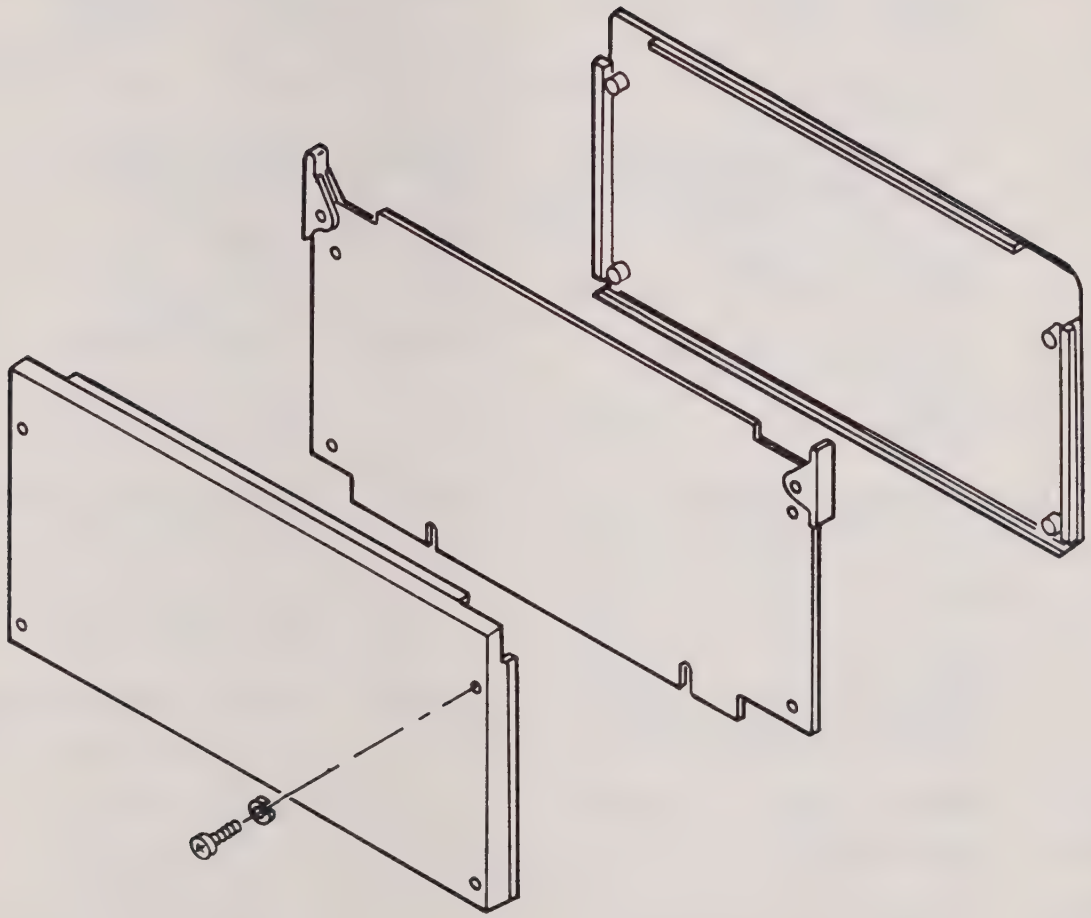


Figure 6-11. Filter CCA A10, A13 (P/N 787176-1 Revision B), Parts Location

Table 6-14. Replacement Parts List: Front End
Circuit Card Assembly A11,A14 - 787505-1 Revision E

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Mylar, 0.68 uf, 400 V, ±1%	886857	12406	2D4A684F
C2	Capacitor, Polyst, 43 pf, 750 V, ±5%	887678	84411	602.1 43pf 5%750V
C3	Capacitor, Glass, 11.0 pf, 750 V (0.8-11.0 pf)	887679	52769	GHL11000
C4	Capacitor, Glass, PS, 0.027, 100 V, ±1%	808175	84171	1PGL273F
C5	Capacitor, Glass, PS, 22 pf, 750 V, ±5%	808288	07342	808288
C6	Not used			
C7	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C8	Same as C2			
C9,C10	Same as C7			
C11	Capacitor, Ceramic, Axial Lead, 0.1 uf, 50 V, ±20%	885498	96095	SA105E104MAA
C12-C28	Same as C11			
C29-C32	Same as C7			
C33,C34	Same as C11			
C35	Capacitor, Mica, 150 pf, 500 V, ±1%	886010	11869	CM04FD151F03
C36	Capacitor, Mica, 82 pf, 500 V, ±1%	807434	72136	DM15 820F
C37	Same as C3			
C38,C39	Same as C7			
C40-C44	Same as C11			

Table 6-14. Replacement Parts List: Front End
Circuit Card Assembly A11,A14 - 787505-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C45	Capacitor, Ceramic, 560 pf, Temp Stable	884148	71590	CW15A561K
	NOTE Capacitor C46 is a select-at-test component with a nominal value of 5 pf, but which may vary within a range of 1-5 pf. During alignment procedures select appropriate component as needed.			
C46	Capacitor, Mica, 5 pf, 300 V, ±1 pf (Nominal Value)	806244	72136	DM5 05A
	Select at Test Capacitor, Mica, 1 pf, 500 V, ±0.5 pf	802619	72136	DM15-010D
	Capacitor, Mica, 2 pf, 500 V, ±0.5 pf	808258	72136	DM15-020D
	Capacitor, Mica, 3 pf, 500 V, ±0.5 pf	807459	72136	DN10-030-J
CR1	Diode, Zener	880714	81349	1N4735A
CR2	Same as CR1			
CR3	Diode, Sig, IN	802924	07263	1N3600
CR4	Same as CR3			
CR5	Diode, Zener	803552	81349	1N4734A
CR6	Same as CR5			
CR7	Rectifier, Schottky, 125 V, 1A	886006	81349	1N5805
CR8	Same as CR7			
CR9	Not used			
CR10	Not used			

Table 6-14. Replacement Parts List: Front End
Circuit Card Assembly A11,A14 - 787505-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
CR11	Diode, Sig, IN	808974	81349	1N4148
CR12	Same as CR11			
K1	Relay, Form C, 5-Coil, Dip	886719	95348	847C-1/-2
K3-K4	Same as K1			
Q1	Transistor, Mosfet, N-Chan, NML	806213	81349	2N5246
Q2	Same as Q1			
Q3	Transistor, Mosfet	886496	17856	VN0300N
Q4,Q5	Same as Q3			
R1	Resistor, Mtch Set, 1.998 Meg	885353	07342	885353-0002
R2	Resistor, Mtch Set, 2.00 Meg	885353	07342	885353-0001
R3	Resistor, Metal Film, 2 Meg, 1/4 W, ±1%	886863	81349	RN60D2004F
R4	Resistor, Fixed, WW, 27 k, 9 W, ±5%	807231	91637	CW-7,9W,±5% .27KOHM
R5	Resistor, Metal Film, 14.3 k, 1/8 W, ±1%	807475	16299	NC4 14.3K
R6	Resistor, Metal Film, 1.24 k, 1/10 W, ±1%	887688	91637	CMF-55 1.24K
R7	Resistor, Composition, 10 k, 1/4 W, ±5%	880092	01121	CB1035
R8	Resistor, Composition, 100 ohm, 1/4 W, ±5%	880077	00779	87022-9
R9	Same as R8			
R10	Resistor, Variable, Pot, 100 k	808428	32997	3299X-1-104

Table 6-14. Replacement Parts List: Front End
Circuit Card Assembly A11,A14 - 787505-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R11	Resistor, Composition, 910 ohm, 1/4 W, ±5%	807165	01121	CB9115
R12	Resistor, Composition, 820 ohm, 1/4 W, ±5%	803693	01121	CB8215
R13	Resistor, Composition, 1 k, 1/4 W, ±5%	880084	01121	CB1025
R14	Resistor, Variable, 10 k	807507	32997	3299X-1-103
R15	Not used			
R16	Resistor, Metal Film, 16.2 k, 1/8 W, ±1%	806559	16299	NC4
R17	Resistor, Metal Film, 1 k, 1/10 W, ±1%	808213	16299	NC55
R18	Resistor, Composition, 68 k, 1/4 W, ±5%	880098	01121	CB6835
R19	Resistor, Fixed, WW, 100 ohm, 2 W, ±1%	807648	81349	RW80U1000F
R20	Same as R5			
R21	Not used			
R22	Resistor, Composition, 3.3 k, 1/4 W, ±5%	803388	01121	CB3325
R23	Same as R22			
R24	Resistor, Metal Film, 392 ohm, 1/8 W, ±1%	887537	01121	RN55D3920F
R25	Resistor, Metal Film, 59 ohm, 1/8 W, ±1%	887538	01121	RN55D0590F
R26	Same as R7			
R27	Resistor, Composition, 750 ohm, 1/4 W, ±5%	880602	01121	CB7515
R28	Same as R27			

Table 6-14. Replacement Parts List: Front End
Circuit Card Assembly A11,A14 - 787505-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R29	Not used			
R30	Resistor, Composition, 270 k, 1/4 W, ±5%	804400	01121	CB2745
R31	Same as R30			
R32	Resistor, Composition, 5.6 k, 1/4 W, ±5%	801983	01121	CB5625
R33	Same as R32			
R34	Resistor, Metal Film, 4.12 k, 1/20 W, ±1%	886373	91637	EMF-50-100-4.12K
R35	Resistor, Metal Film, 4.32 k, 1/20 W, ±1%	887763	81349	RN50STY1/20W
R36	Resistor, Composition, 18 k, 1/4 W, ±5%	802183	01121	CB1835
R37	Not used			
R38	Not used			
R39	Resistor, Composition, 2 M, 1/4 W, ±5%	807094	01121	CB2055
R40	Same as R39			
R41	Resistor, Trimpot, 20 ohm, Side Adj, 25 Turn	887936	32997	3299-X-1-200
TP1	Post, P and Cont., Mod II, Machine Applied	880007	00779	87022-9
TP2-TP6	Same as TP1			
TP7	Not used			
TP8-TP11	Same as TP1			
U1	IC, Op Amp, 8-Pin, DIP	886495	06665	OP16-EZ
U2	IC, Analog Switch	886030	17856	DG509ACJ

Table 6-14. Replacement Parts List: Front End
Circuit Card Assembly A11,A14 - 787505-1 Revision E (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U3	IC, Op Amp, OP-37GZ	886029	06665	OP-37GZ
U4	IC, Linear Quad Analog Switch	808733	12040	LF13333N
U5	Same as U4			
U6,U7	Same as U3			
U8	IC, Interface	885991	58361	MCT6
U9-U11	Same as U8			
U12	IC, Quad Timer	887532	18324	NE559
U13	IC/L, Op Amp, St, NML	808302	12040	LM311N
U14	Same as U13			
Z1	Resistor, Network, 100 ohm, 900 ohm, 9 k	885350	07342	885350
Z2	Resistor, Network, 1 k, 16.3205 k	885351	07342	885351
Z3	Resistor, Network, 3 Pin, 100 ohm, 1.63205 k	887758	07342	887758
Z4	Resistor, Network, 470 ohm, 5 Res	885989	01121	106A471
Z5	Resistor, Network, 5.6 k, 5 Res	886046	01121	106A562
Z6	Resistor, Network, NML, 8 Pin, 4 Res, SIP	808626	32997	4308R-102-103

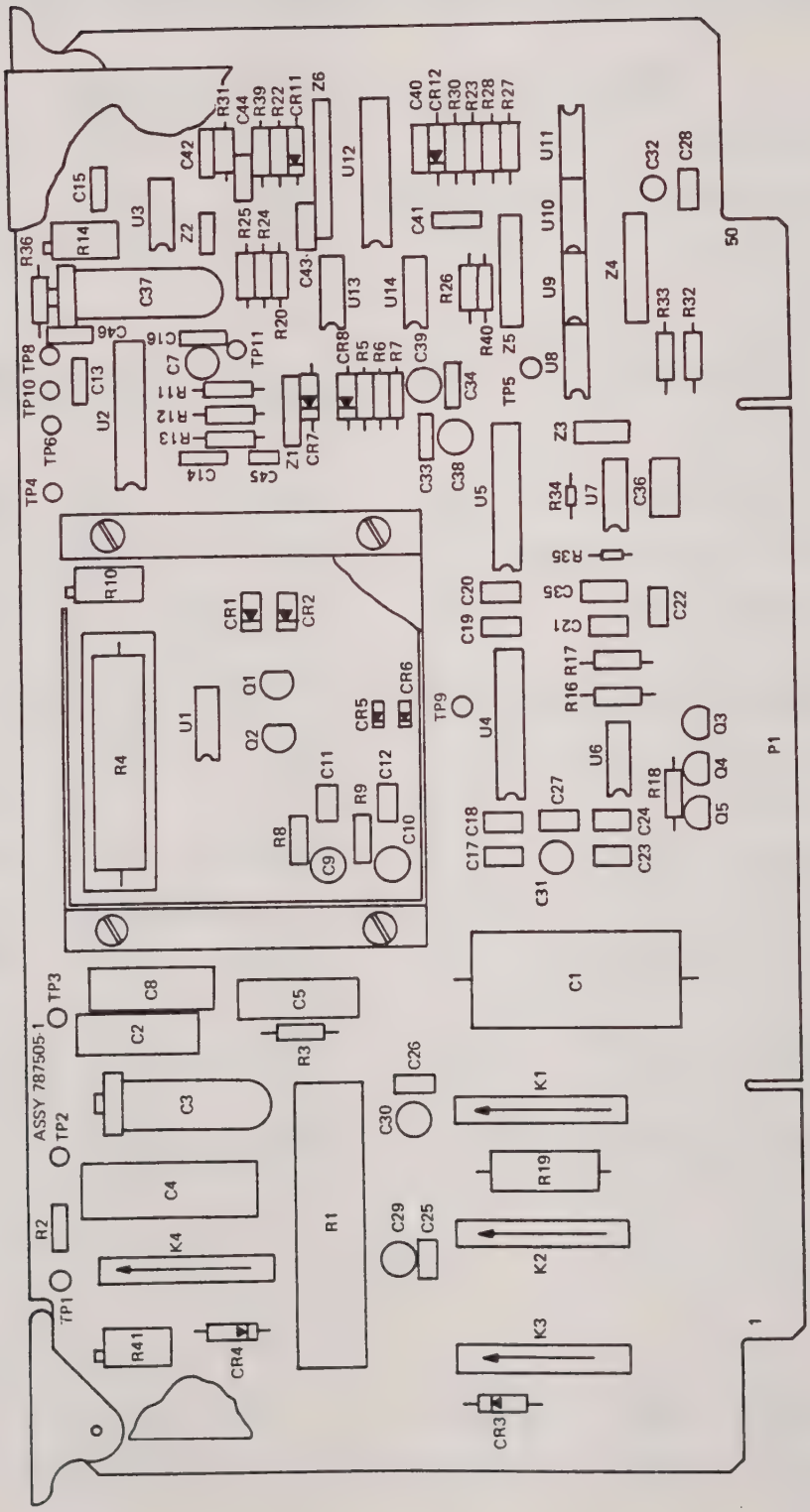


Figure 6-12. Front End CCA A11/A14 (P/N 787505-1 Revision E), Parts Location

Table 6-16. Replacement Parts List: Display Driver Circuit Card Assembly A15A2 - 787179 Revision D

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25V-M-ZD
C2	Capacitor, Solid, Tantalum, 47 uf, 20 V, ±10%	883985	90201	CGS612U050R4C
C3-C11	Same as C2			
C12	Capacitor, Ceramic, 0.01 uf, 50 V, +80-20%	886061	AAAAA	NCD-.01M50V-ZZ5V
C13-C19	Same as C12			
C20	Same as C2			
J1	Post, P and Cont, Mod II, Machine Applied	880007	00779	87022-9
J2-J4	Same as J1			
J5	Connector, Wafer, 2-Pin	886037	27264	26-48-1024
Q1	Transistor, Sig.	886018	81349	2N3444
Q2-Q21	Same as Q1			
U1	IC, Dual 4-Input NAND Gate	884629	01295	SN74LS20N
U2	Transistor Array	886602	02735	CA3082
U3	IC, TTL, Octal D Flip-Flop	808576	01295	SN74LS374N
U4	IC, TTL, Hex Inverter Buffer/Driver	808971	01295	SN7406N
U5	IC, TTL, Hex Inverter	885980	01295	74LS05N
U6	IC, Interface	885994	27014	MM74C911N
U7	IC, Interface	883412	04713	MC6821P
U8	Same as U3			
U9	Same as U4			

Table 6-16. Replacement Parts List: Display Driver Circuit Card Assembly A15A2 - 787179 Revision D (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
U10	IC, TTL, 1-of-8 Decoder/Demultiplexer	808699	01295	SN74LS138
U11	IC, TTL, 5-Bit Shift Register	884214	01295	SN74LS96N
U12	Same as U6			
U13	IC, LV TTL, Bus Receiver, 20-Pin	886186	04713	SN74LS645
U14	Same as U6			
U15	IC, Expandable Segment Display Controller	885995	27014	MM74C912N
U16	Same as U10			
U17	IC, TTL, Quad 2-Input OR Gate	808898	01295	SN74LS32N
U18	Same as U6			
Z1	Resistor, Network, 33 ohm, 4 Res.	886023	01121	108B330
Z2-Z4	Same as Z1			
Z5	Resistor, Network, 10 k, 8 Res.	886020	01121	316B103
Z6	Same as Z5			
Z7	Resistor, Network, 75 ohm, 8 Res.	886022	01121	316B750
Z8	Same as Z7			
Z9	Resistor, Network, 47 ohm, 16-pin, 8 Res. DIP	886451	01121	316B470
Z10	Same as Z9			

Table 6-16. Replacement Parts List: Display Driver
Circuit Card Assembly A15A2 - 787179 Revision D (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
Z11	Resistor, Network, 3.3 k, SIP, 6-P, 3 Res, L PF	884755	01121	106B-3.3K
Z12-Z15	Same as Z1			
Z16	Resistor, Network, 470 ohm, 8 Res.	886021	01121	316B471

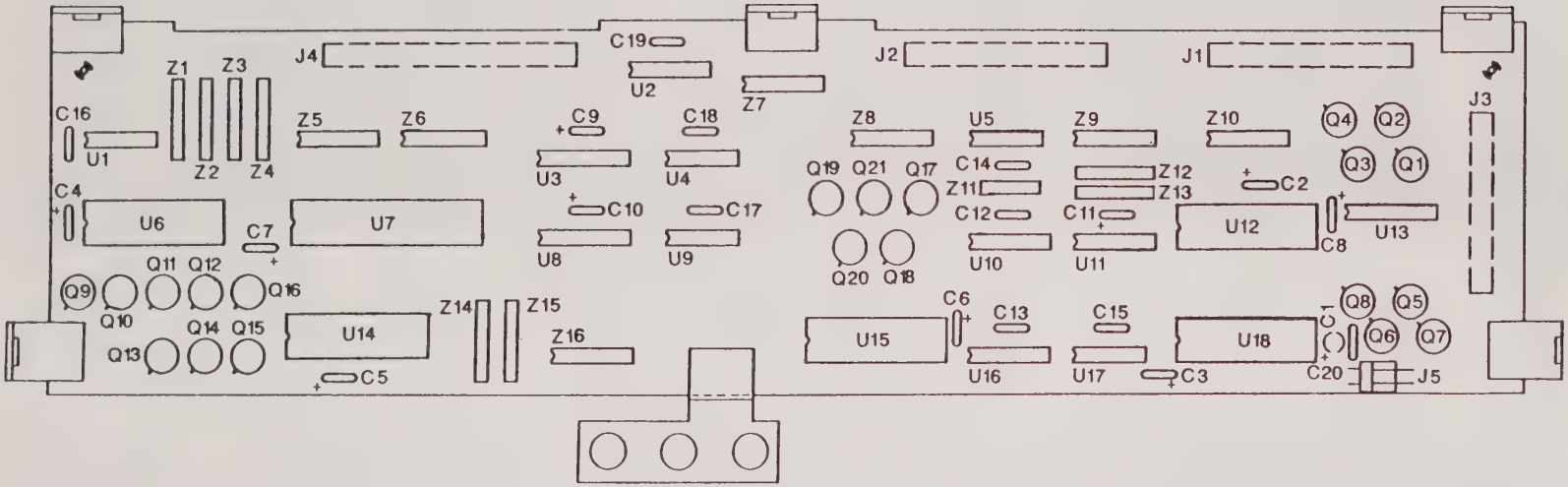


Figure 6-14. Display Driver Board A15A2 (P/N 787179 Revision D), Parts Location

Table 6-17. Replacement Parts List: Display
Circuit Card Assembly A15A3 - 787178 Revision D

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
	NOTE			
	NAI P/N 887339 represents a matched set of 3 LTD-6940 HR LEDs. NAI P/N 887340 represents a matched set of 5 LTS-3940 HR/315 AHR LEDs.			
DS1-DS3	Digital Display (Matched Set of 3)	887339	CCCCC	LTD-6940HR
DS4-DS8	Digital Display (Matched Set of 5)	887340	CCCCC	LTS-3940HR/315 AHR
DS9	Diode, LED	886043	CCCCC	LTL-57173
DS10-DS17	Same as DS9			
DS18	Digital Display	886042	CCCCC	LTA-1000E
DS19-DS23	Same as DS18			
DS24-DS30	Same as DS9			
J1	Header, PC, 40-Pin	880422	28218	3432-1002
J2	Same as J1			
XUDS4-	Socket, 14-Pin, Low Profile	887876	GGGGG	BU-14-02SF
XUDS5-XUDS8	Same as XUDS4			

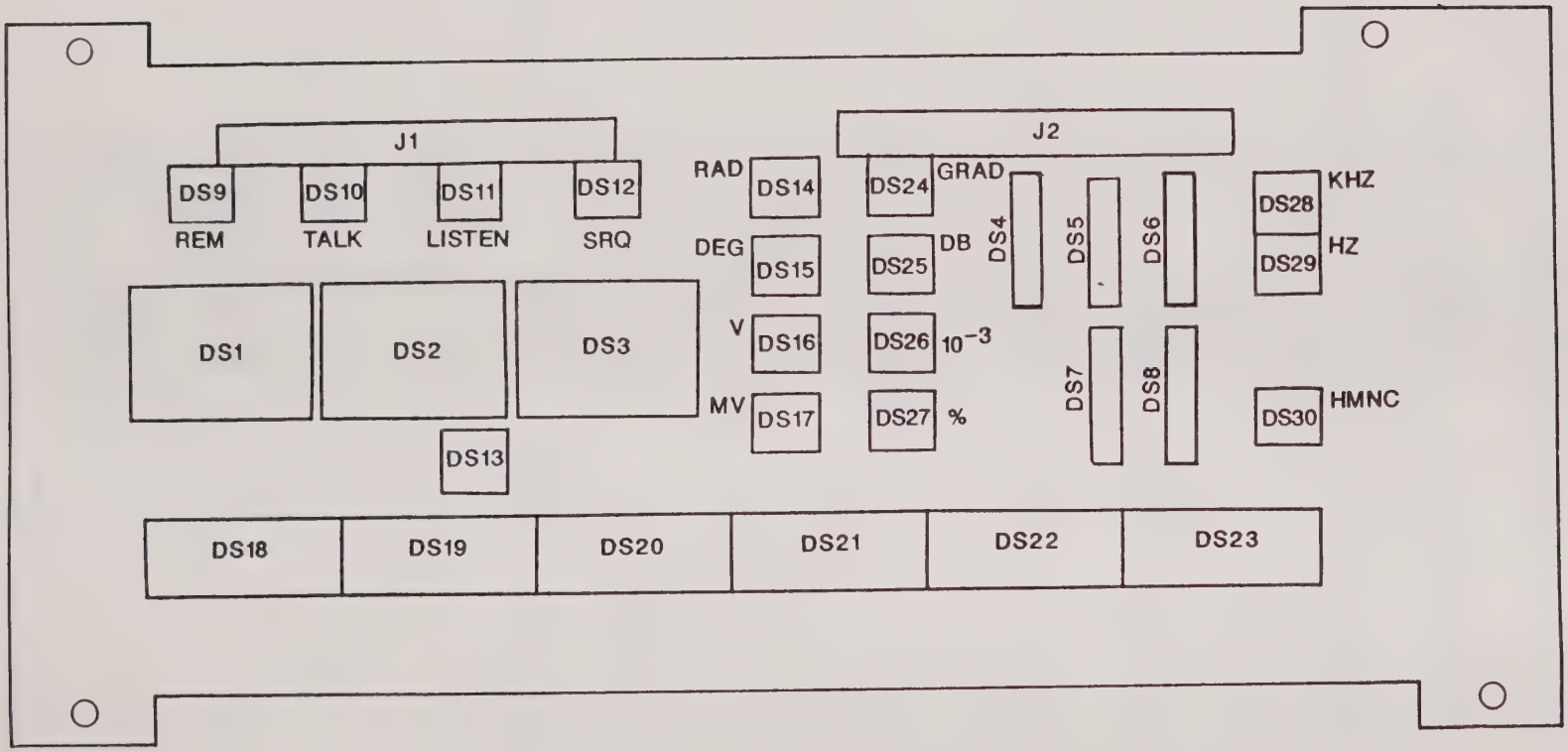


Figure 6-15. Display CCA A15A3 (P/N 787178 Revision D), Parts Location

Table 6-18. Replacement Parts List: Signal and Reference Isolation Circuit Card Assemblies A15A4, A15A5 - 787448-1, -2 Revision D

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
CR1	Diode, Schottky, 30 V	886005	81349	1N5818
K1	Relay, Form C, 5-Coil, DIP	886719	95348	847C-1/-2
K2,K3	Same as K1			
P1	Connector, Right Angle, 8-Pos, 0.156 Ctrs	886720	06383	MLAS156-8
P2	Connector, Right Angle 5-Pos, 0.156 Ctrs	886721	06383	HLAS156-5
Q1	Transistor, Mosfet	886496	17896	VN0300N
Q2	Same as Q1			
R1	Resistor, Composition, 330 ohm, 1/4 W, ±5%	880080	01121	CB3315
R2	Resistor, Composition, 5.6 k, 1/4 W, ±5%	801983	01121	CB5625
U1	IC, Interface	885991	58361	MCT6
W1	Relay Isolation Cable Assembly (#1)	548513	07342	548513

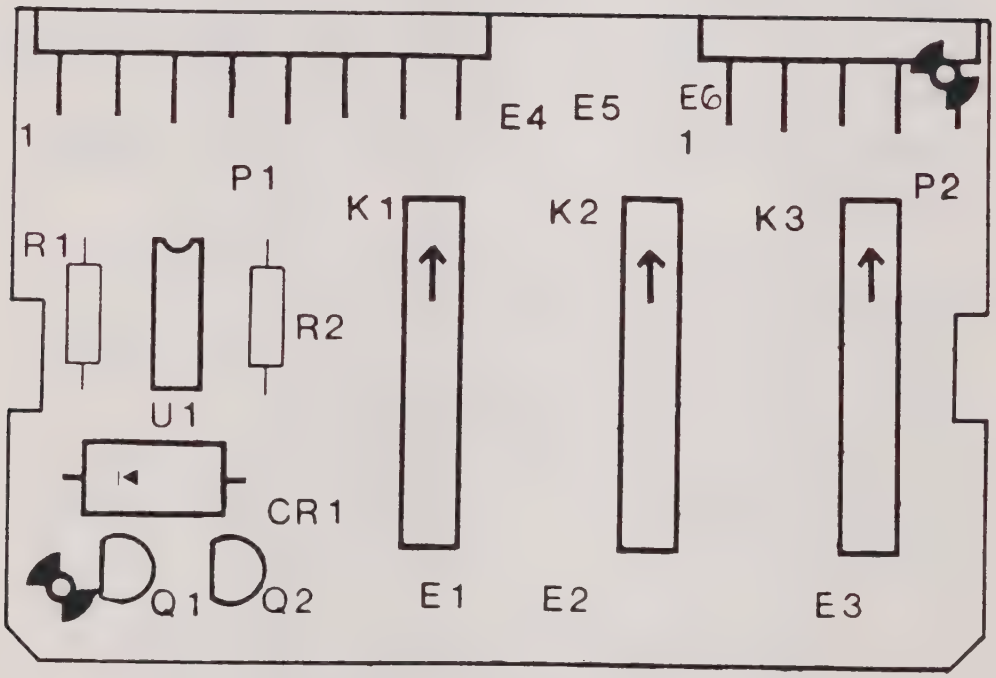


Figure 6-16. Signal and Reference Isolation CCA A15A4, A15A5 (P/N 787448-1, -2 Revision D), Parts Location

Table 6-19. Replacement Parts List: Front Bezel Switch Assembly
A15S1 - 548493 Revision E

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
J1	Connector, Rack and Panel, Plug, Nylon w/o Ear	880352	27264	03-09-2062
SW1	Switch, Pushbutton	886085	31918	01-003-00-FA-NE15-F2U103EE

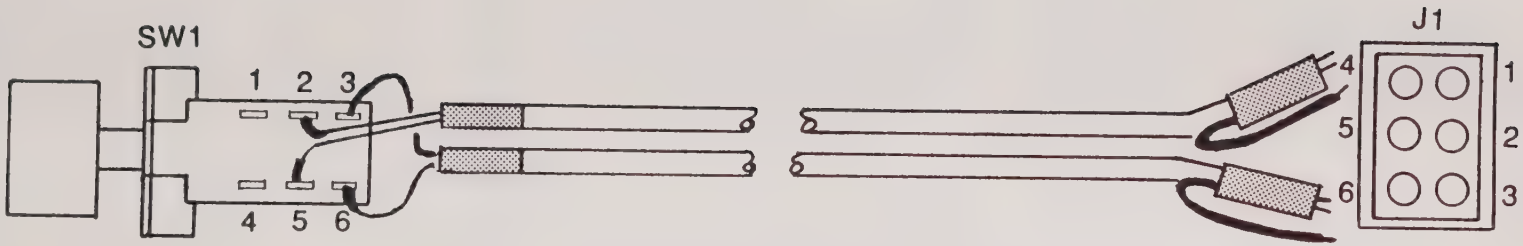


Figure 6-17. Assembly Switch A15S1 (P/N 548493 Revision E), Parts Location

Table 6-20. Replacement Parts List: Mother Circuit Card Assembly A16A1 - 787177 Revision J

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Tantalum, 3.3 uf, 25 V, ±20%	886064	AAAAA	NDT3.3M-25 V MZD
C2	Capacitor, Ceramic, 0.01 uf, 50 V, +80-20%	886061	AAAAA	NCD-.01M50VZZ5V
C3	Same as C1			
C4	Same as C2			
C5	Same as C1			
C6	Same as C2			
C7	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C8	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	886063	16299	SR215E104MAA
J1	Post, P and Cont., Mod II, Machine Applied	880007	00779	87022-9
J2	Connector, Card Edge, 100-Pin	886094	54453	EZA50DCSH
J3-J15	Same as J2			
J16	Connector, Male, 4-Pin	886095	06383	HLSS156-4
J17	Same as J16			
J18	Connector, Wafer, 6-Pin	886170	06383	HLSS156-6
J19	Not used			
J20	Connector, Wafer, 5-Pin, 0.156 Ctrs, 0.045	886581	06383	HLSS156-5
J21	Same as J18			
J22	Not used			
J23	Same as J20			
J24	Connector, Wafer, Lock, 0.156 CTRS, 3 P	886948	06383	HLSS156-3

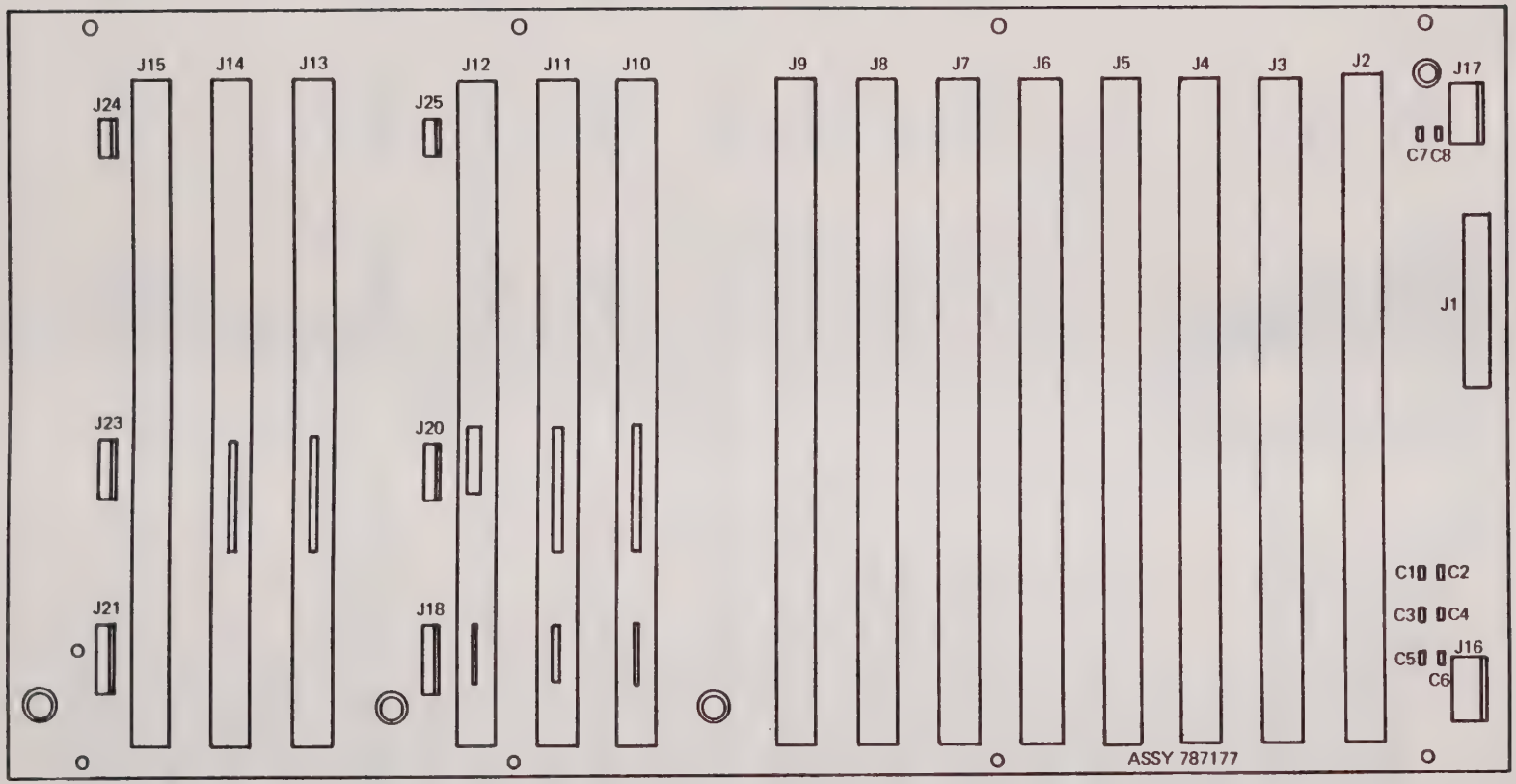


Figure 6-18. Mother Circuit Card Assembly A16A1 (P/N 787177 Revision J), Parts Location

Table 6-21. Replacement Parts List: Rear Panel Assembly
A17 - 787277 Revision D

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
A17A1	Recorder Filter Assembly	787667	07342	787667
A17B1	Fan Blo, 3 1/8-inch square, 115 V ac, 60 Hz	808689	92702	AS115AAES
A17B1MP1	Guard, HDW, 3 1/8-inch sq.	808688	81040	6-182036
A17J1	Socket, Power Cord	886093	56289	200JMJ6-2
A17E1	Binding Post, Green	886326	18310	01-1102-1-0315
A17E2	Binding Post, Black	886327	18310	01-1102-1-0310
A17PS1	Main Power Supply	787181	07342	787181
A17PS2	Reference Isolated Power Supply Assembly	787313-1	07342	787313-1
A17PS3	Signal Isolated Power Supply Assembly	787313-1	07342	787313-1
A17T1	Main Transformer Assembly	787314	07342	787314
A17T1J1	Connector, Housing, 6-Pin	880352	27264	03-09-2062
A17W1	Main Harness Assembly	548504	07342	548504
A17W2	Relay Isolation Cable Assembly #2	548514	07342	548514
A17W3	Relay Isolation Cable Assembly #3	548515	07342	548515
A17W4J3	Connector, BNC, Isolated	886750	05276	3778
A17W5	I/O Cable Assembly	548502	07342	548502
A17W5J4	Connector, Screw Lock	808967	00779	552633-3
A17W5S1	IEEE Address Switch	298891	07342	298891
A17W6	Link, Shorting	800339	24655	938L

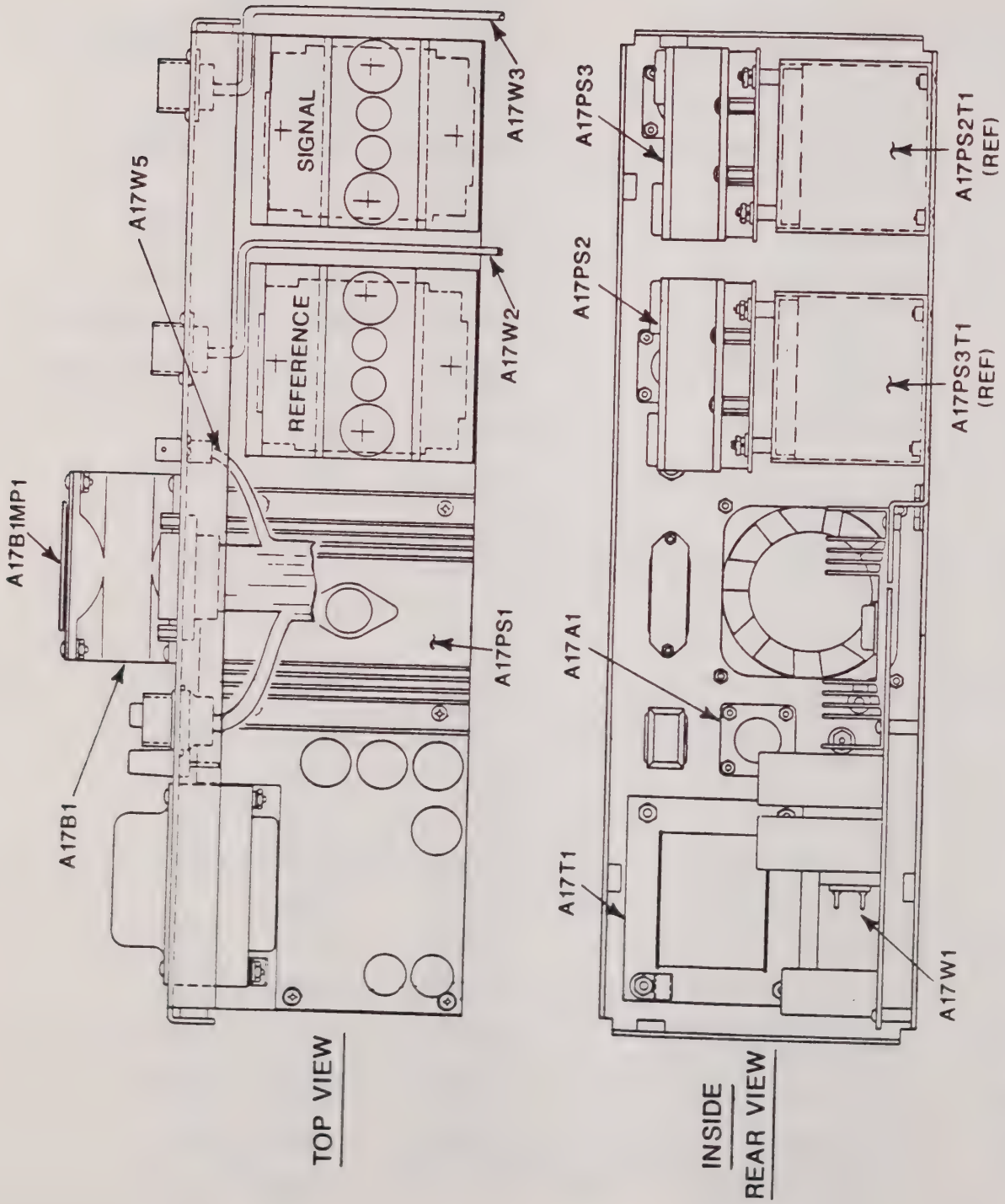


Figure 6-19. Rear Panel Assembly A17 (P/N 787277 Revision D), Parts Location (Sheet 1 of 2)

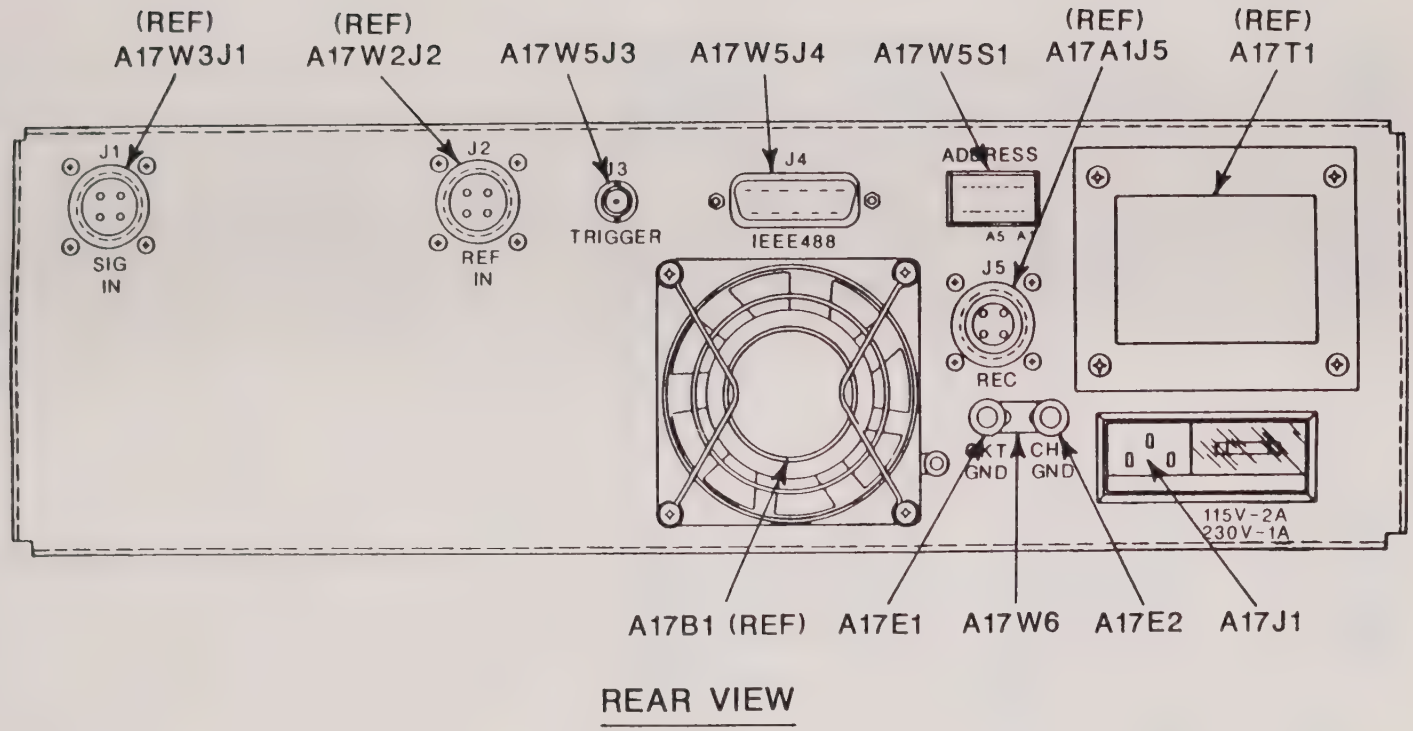


Figure 6-19. Rear Panel Assembly A17 (P/N 787277 Revision D), Parts Location
(Sheet 2 of 2)

Table 6-22. Replacement Parts List: Recorder Filter Assembly A17A1 - 787667 Revision A

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Tantalum, Radial Leads, 3.3 uf, 25 V, ±20%	886064	AAAAA	NDT3.3M-25VMZD
C2-C4	Same as C1			
J1	Connector, Circular	801431	81349	MS-3102A-145-2S
J2	Connector, Wafer, 4 Pos	887595	06383	NLSS100-4
R1	Resistor, Composition, 2 k, 1/4 W, ±5%	880086	01121	CB2025
R2	Same as R1			

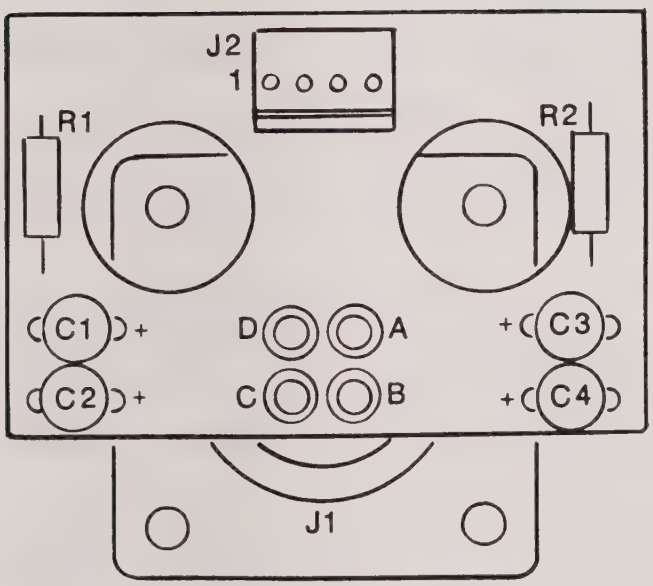


Figure 6-20. Recorder Filter Assembly A17A1 (P/N 787667 Revision A), Parts Location

Table 6-23. Replacement Parts List: Main Power Supply Circuit Card Assembly A17PS1 - 787181 Revision H

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, El, Aluminum, 10000 uf, 25 V, Radial	886166	AAAAA	NRE-10000M25V
C2-C4	Same as C1			
C5	Capacitor, El, Tantalum, 0.33 uf, 35 V, Radial, LDS	886167	AAAAA	NDT.33M35VNZ
C6	Capacitor, Ceramic, 0.1 uf, 50 V, ±20%	886063	16299	SR215E104MAA
C7	Capacitor, Tantalum, 4.7 uf, 25 V, ±20%	886059	AAAAA	NDT4.7M25VMZD
C8	Capacitor, Tantalum, 10 uf, 25 V, ±20%	886060	AAAAA	NDT-10M-25VM-ZD
C9	Same as C7			
C10	Same as C6			
C11	Capacitor, Ceramic, 0.01 uf, 50 V, +80-20%	886061	AAAAA	NCD-.01M50V-ZZ5V
C12	Capacitor, El, Aluminum, 2200 uf, 35 V	887264	AAAAA	NRE-E-2200M35V
C13	Same as C12			
C14	Capacitor, El, Tantalum, 4.7 uf, 35 V, ±20%	881427	56289	196D475X0035JE3
C15	Same as C14			
C16	Capacitor, Tantalum, 3.3 uf, 25 V, ±20%	886064	AAAAA	NDT3.3M-25V MZD
C17	Same as C16			
C18,C19	Same as C11			
C20	Same as C6			
CR1	Diode, Dual Rectifier, Schottky	886164	81483	12CTQ040

Table 6-23. Replacement Parts List: Main Power Supply
Circuit Card Assembly A17PS1 - 787181 Revision H (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
CR2	Same as CR1			
CR3	Diode, PWR/Rectifier	808787	81349	JAN1N4001
CR4	Same as CR3			
CR5	Diode, Bridge, Rectifier	884735	04713	MDA970A-1
CR6-CR9	Same as CR3			
J1	Connector, Wafer, 6-Pin	886170	06383	HLSS156-6
R1	Resistor, Fixed, 1.1 k, 1/2 W, ±5%	801595	01121	EB1125
R2	Resistor, Fixed, Metal Film, 120 ohm, 1/4 W, ±0.5% @ 70°C	886168	91637	CMF-60T2-1200D
R3	Resistor, Fixed, Metal Film, 383 ohm, 1/4 W, ±0.5% @ 70°C	886169	91637	CMF-60T2-3830D
R4	Resistor, Composition, 5.1 k, 1/2 W, ±5%	800613	01121	EB5125
R5	Same as R4			
R6	Resistor, Composition, 47 k, 1/2 W, ±5%	800870	01121	EB4735
R7	Same as R6			
VR1	IC, Voltage Regulator, +5 V	808498	12040	LM340T-5.0
VR2	IC, Regulator, 3 Terminal, Adjustable, 10 A	886161	27014	LM396K Steel
VR3	IC, Regulator, 3 Terminal, +15 V, 1 A	886162	27014	LM340T-15
VR4	IC, Regulator, 3 Terminal, -15 V, 1 A	886163	27014	LM320T-15
W1	Cable Assembly, Main Power Supply	548496	07342	548496

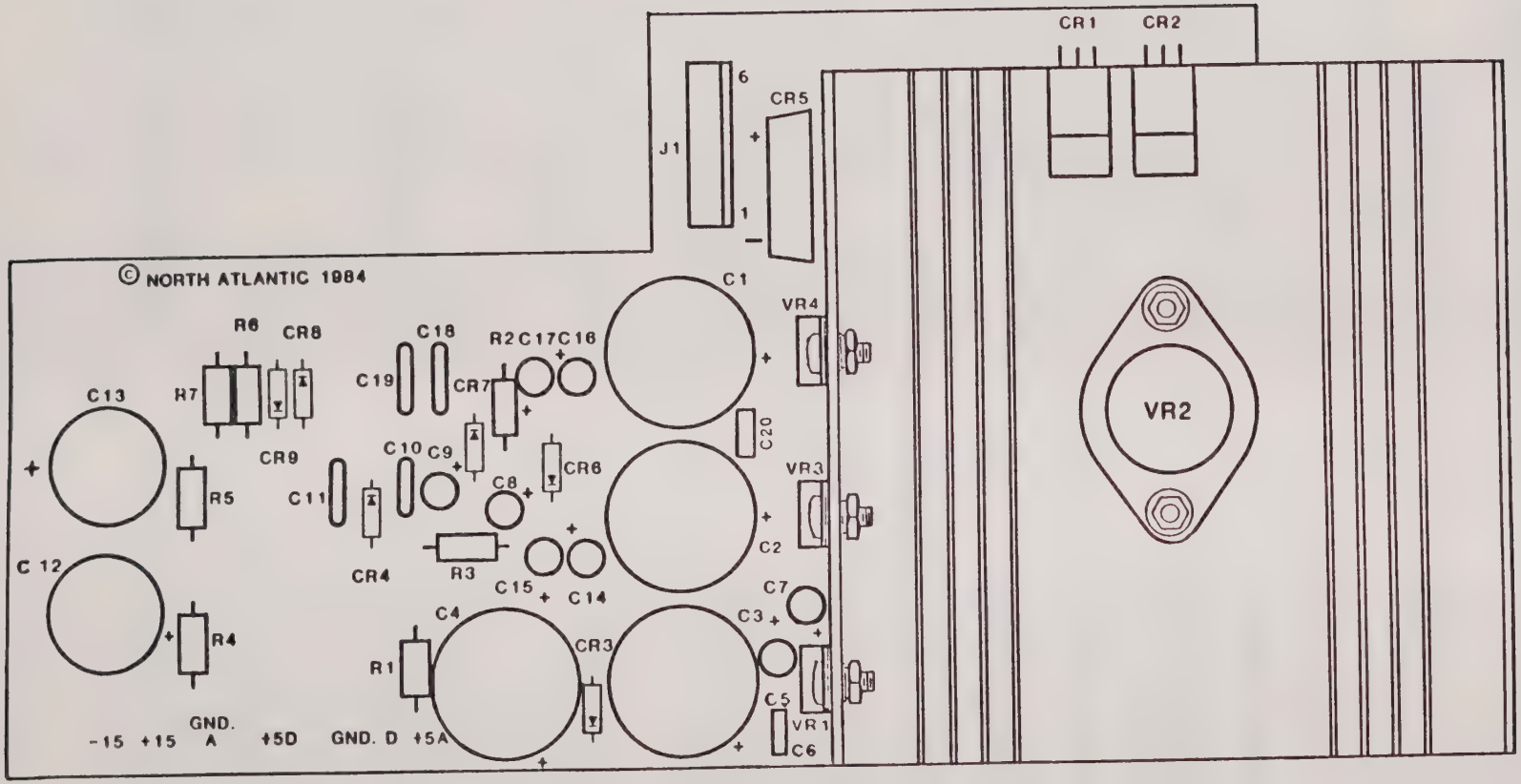


Figure 6-21. Main Power Supply CCA A17PS1 (P/N 787181 Revision H), Parts Location

Table 6-24. Replacement Parts List: Cable Assembly
Main Power Supply A17PS1W1 - 548496 Revision B

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
P1-P4	Not used			
P5	Connector, Wafer, 2-Pin	886038	27264	09-50-7921
P6-P15	Not used			
P16	Connector, Housing, 4 P, 0.156 Centers	886452	06383	CR156F20-4
P17	Same as P16			

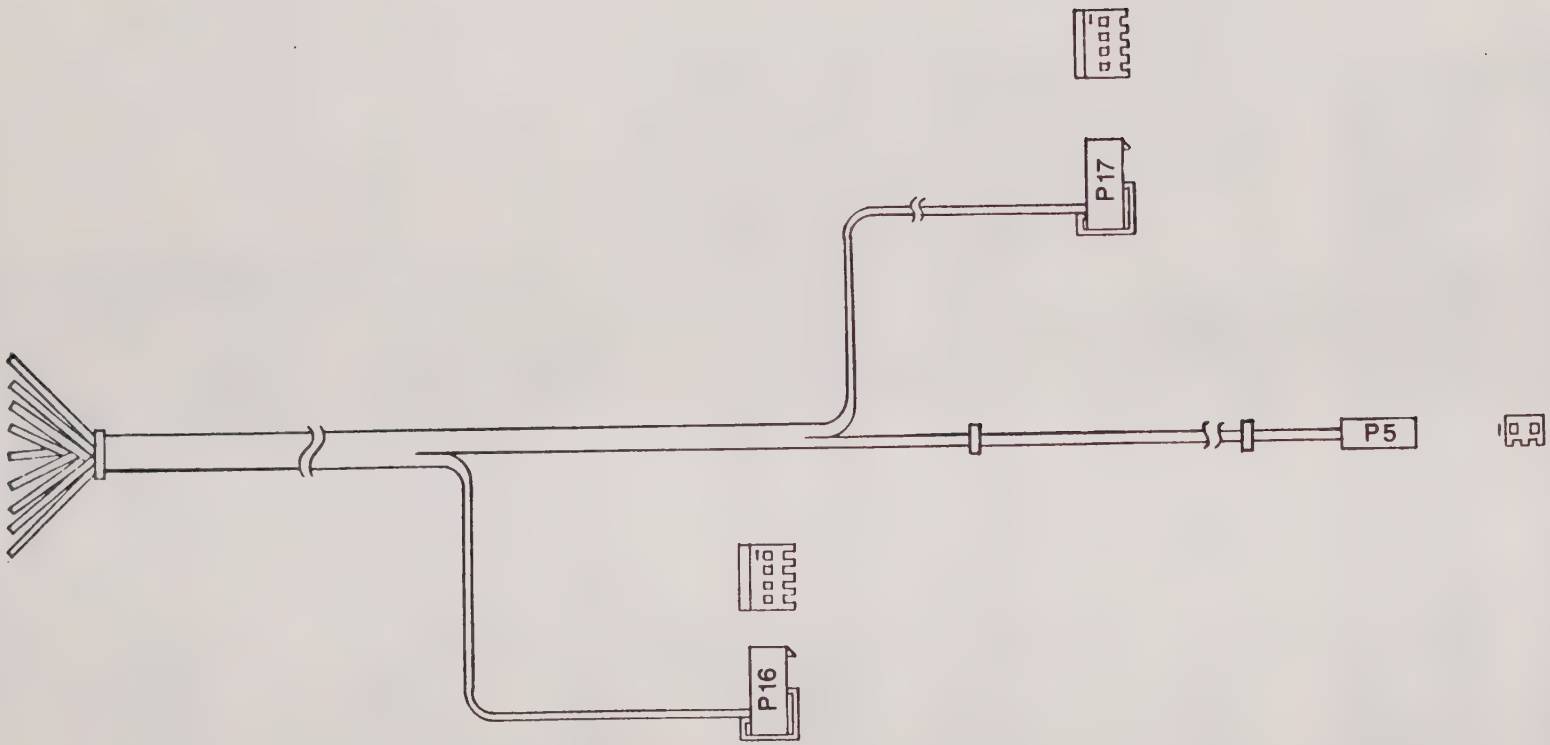


Figure 6-22. Main Power Supply Cable Assembly A17PS1W1 (P/N 548496 Revision B), Parts Location

Table 6-25. Replacement Parts List: Isolated Power Supply Assembly A17PS2, A17PS3 - 787313-1 Revision A

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
A17PS2A1	Isolated Power Supply Assembly	787180-1	07342	787180-1
A17PS2T1	Assembly, Transformer	787315	07342	787315

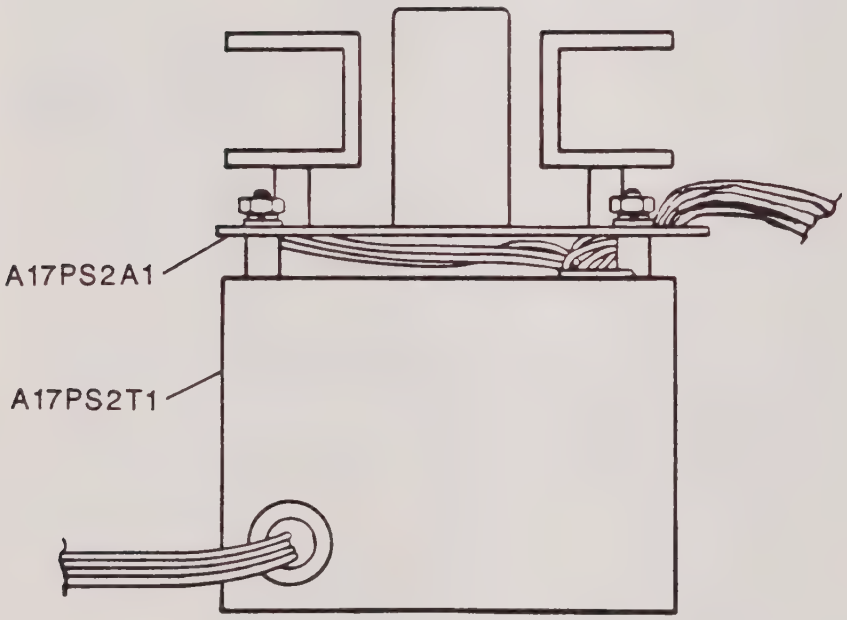


Figure 6-23. Isolated Power Supply Assembly A17PS2, A17PS3 (P/N 787313-1 Revision A), Parts Location

Table 6-26. Replacement Parts List: Isolated Power Supply Circuit Card Assembly A17PS2A1, A17PS3A1 - 787180-1 Revision A

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, El, Aluminum, 6800 uf, 16 V, ±20%	886363	AAAAA	NRS-E-6800M25
C2	Not used			
C3	Capacitor, El, Aluminum, 1500 uf, 35 V, ±20%	887265	AAAAA	NRE-E-1500M35
C4	Same as C3			
C5	Capacitor, Tantalum, 4.7 uf, 25 V, ±20%	886059	AAAAA	NDT4.7M25VMZD
C6-C8	Same as C5			
C9	Capacitor, El, Tantalum, 2.2 uf, 20 V, ±20%	808201	11100	PDT-2.2/35
C10-C12	Same as C9			
C13	Capacitor, Ceramic, 0.01 uf, 50 V, +80-20%	886061	AAAAA	NCD-.01M50V-ZZ5V
C14	Not used			
C15,C16	Same as C13			
CR1	Diode, Bridge Rectifier	884735	04713	MDA970A-1
CR2	Same as CR1			
CR3	Diode, Power/Rectifier	808787	81349	JAN1N4001
CR4-CR8	Same as CR3			
R1	Resistor, Composition, 1.2 k, 1/2 W, ±5%	800522	01121	EB1225
R2	Not used			
R3	Resistor, Composition, 5.1 k, 1/2 W, ±5%	800613	01121	EB-5125

Table 6-26. Replacement Parts List: Isolated Power Supply
Circuit Card Assembly A17PS2A1, A17PS3A1 - 787180-1 Revision A (Continued)

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R4	Same as R3			
VR1	IC/L, VR St, NML	808498	12040	LM340T-5.0
VR2	IC/L, VR St, NML, -5 V	808901	27014	LM7905CT
VR3	IC, Reg., 3 Terminal, +15 V, 1 A	886162	27014	LM340T-15
VR4	IC, Reg., 3 Terminal, -15 V, 1 A	886163	27014	LM340T-15
W1	Cable Assembly, Isolated Power Supply	548491	07342	548491

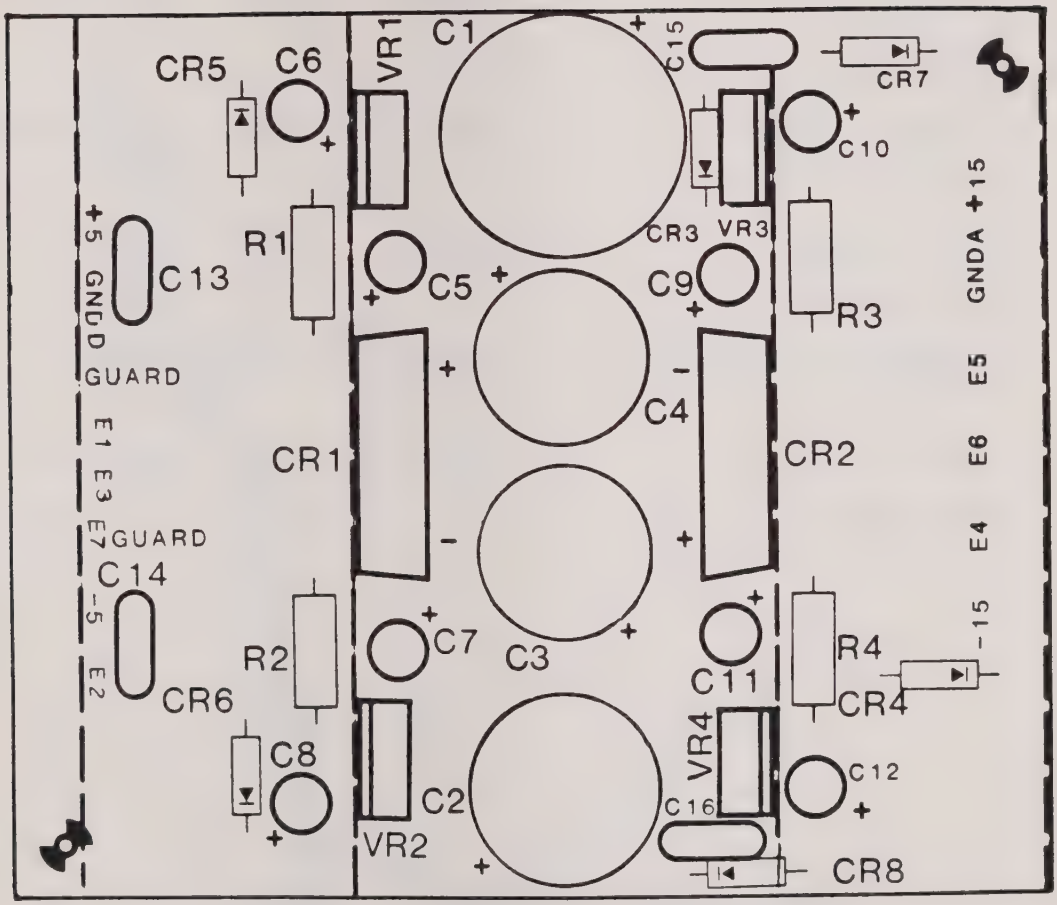


Figure 6-24. Isolated Power Supply A17PS2A1, A17PS3A1 (P/N 787180-1 Revision A), Parts Location

Table 6-27. Replacement Parts List: Main Harness Assembly
A17W1 - 548504 Revision A

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
E1	Terminal Lug	800249	83330	1466
E2-E6	Same as E1			
J1	Connector, 6 pin	886406	27264	126103-09-1063
J2	Same as J1			
J3	Socket Housing	886410	00779	1-480424-0
J4	Same as J3			
P1	Receptacle, AC Power Line Module	886093	56289	200JMJ6-2
VP1	Varistor, 130 V	807699	03508	V130LA10A
VP2	Same as VP1			

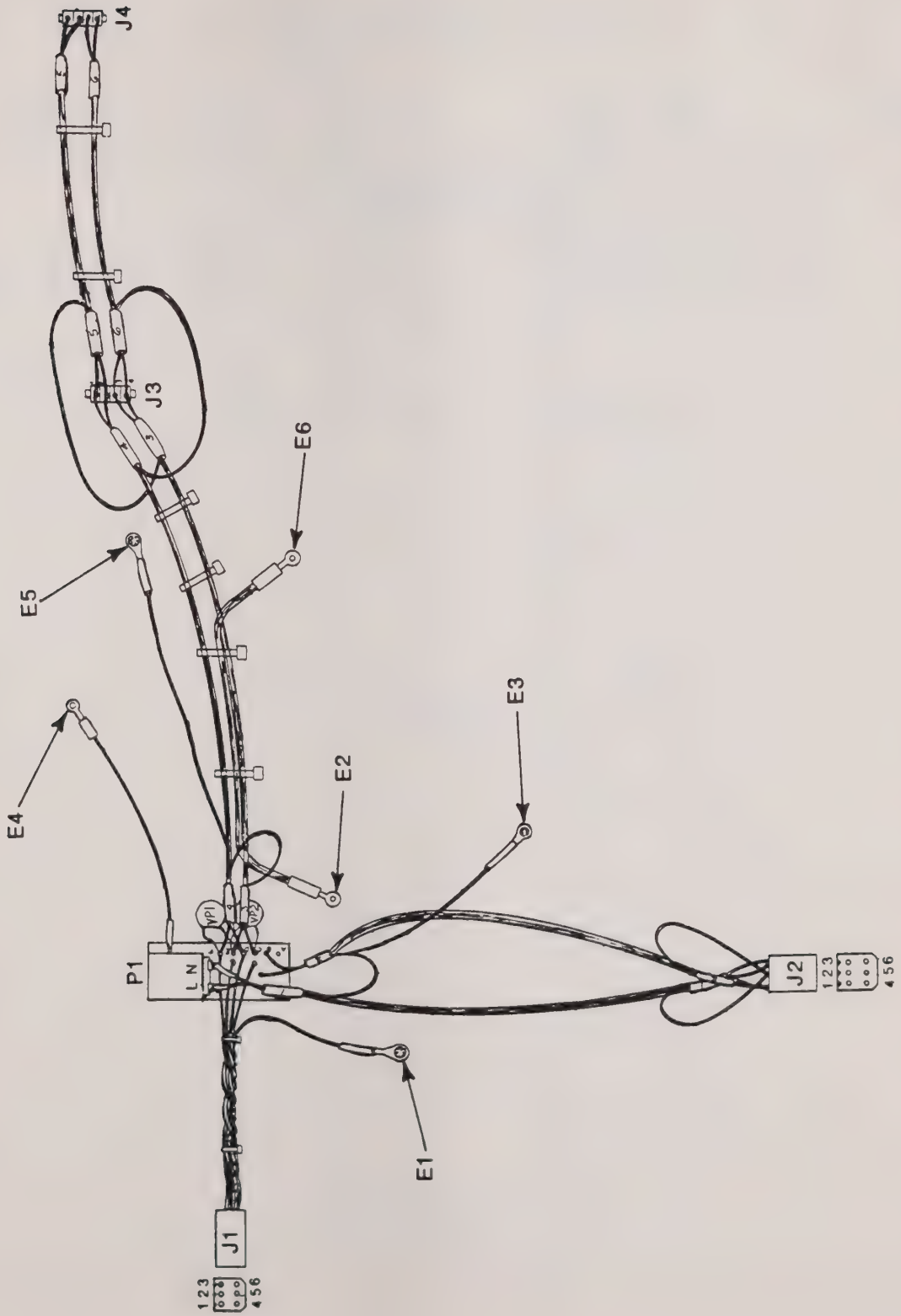


Figure 6-25. Main Harness Assembly A17W1 (P/N 548502 Revision D), Parts Location

Table 6-28. Replacement Parts List: Rear Panel Cable Assembly
A17W5 - 548502 Revision D

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
A3J2	Connector, Card Edge, IDC, 50 Contacts	886582	EEEEE	4401-50-00-P5
J4	Connector, Ribbon, Female	886235	26394	609-24F
J5A	Connector, Circular, Receptacle, 4 Pos	801431	81349	MS3102-A-14S-2S
S1	Switch, DIP, 16-Pin	883415	71450	206-8LPST-Std.
S1J2	Connector, DIP Switch	886236	26394	609-161DS

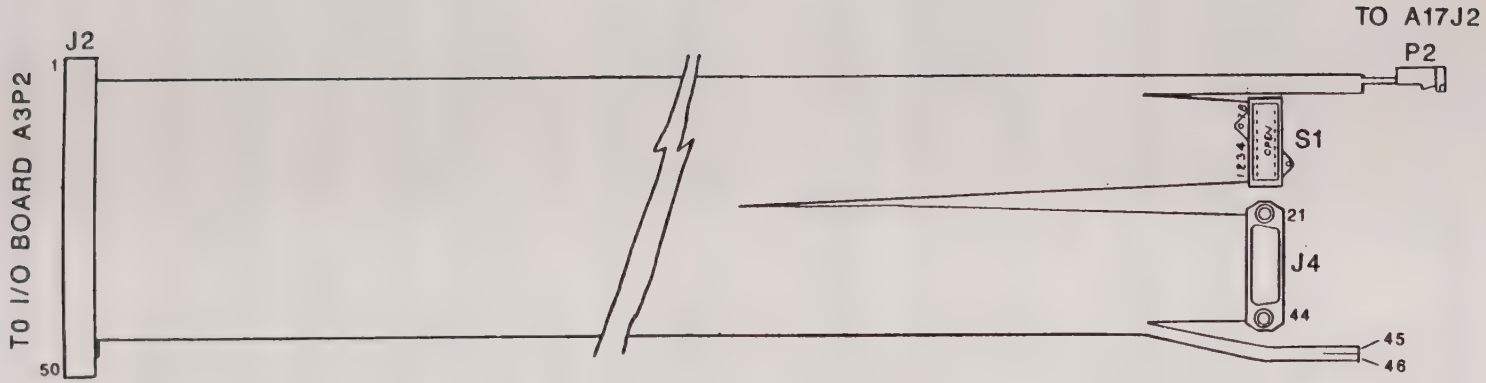
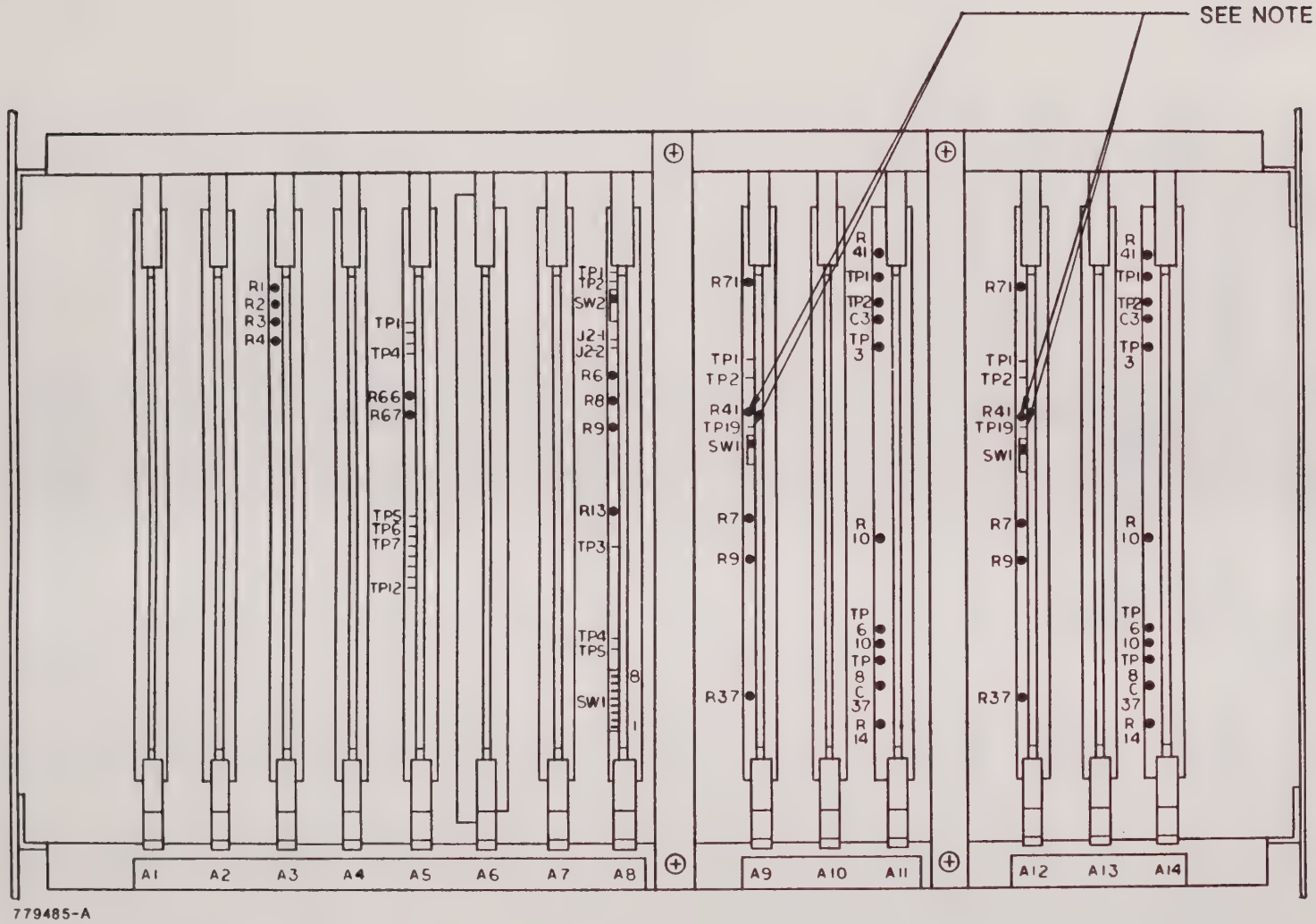


Figure 6-26. Rear Panel Cable Assembly A17W5 (P/N 548502 Revision D), Parts Location



NOTE:

TP19 AND R41 ARE LOCATED IN THE LOWER HALF OF THE BOARD. SEE FIGURE 6-10. A/D CONVERTER CCA A9/A12 (P/N 787664), PARTS LOCATION DIAGRAM FOR THE EXACT LOCATION.

Figure 6-27. Adjustable Component Test Points (P/N 779485 Revision A), Parts Location

Table 6-29. List of Manufacturers

FSCM	NAME AND ADDRESS
00779	AMP Inc. 2800 Fulling Mill P.O. Box 3608 Harrisburg, PA 17105
00815	Midland-Ross Corp. Northern Eng. Labs Div. 357 Beloit Street Burlington, WI 53105
01121	Allen-Bradley Co. 1201 S. 2nd Street Milwaukee, WI 53204
01295	Texas Instruments Semiconductor Group 13500 No Central Expwy P.O. Box 225012 M/S 49 Dallas, TX 75265
01637	Ford Motor Craft 29500 Plymouth Rd. P.O. Box 3000 Livonia, MI 48151
02114	Amperex Electronic Corp. Ferroxcube Div. 5083 Kings Highway Saugerties, NY 12477
02735	RCA - Solid State Route 202 Somerville, NJ 08876
03508	General Electric Co. Semiconductor Prods Dept. West Genesee Street Auburn, NY 13021
04713	Motorola, Inc. Semiconductor Prods Inc. 5005 E. McDowell Road Phoenix, AZ 85008
05276	ITT Pomona Elect. Div. 1500 E. 9th Street P.O. Box 2767 Pomona, CA 91766
06383	Panduit Corporation 17301 Ridgeland Tinley Park, IL 60477
06540	Mite Corp. Amatom Elect. Hardware Div. 446 Blake Street New Haven CT 06515
06665	Precision Monolithics Inc. Sub. of Bourns Inc. 1500 Space Park Drive Santa Clara, CA 95050
07263	Fairchild Camera and Instrument Corp. Semiconductor Division 401 Ellis Street P.O. Drawer 7284 Mountain View, CA 94042
07342	North Atlantic Inds, Inc. 60 Plant Avenue Hauppauge, NY 11788
07980	Hewlett-Packard Co. New Jersey Division 150 Green Pond Road Rockaway, NJ 07866
11100	Nemco Corporation 3329 Prospect Indianapolis, IN 46203
11869	Microsonics Inc. 60 Winter Street Weymouth, MA 02188

Table 6-29. List of Manufacturers (Continued)

FSCM	NAME AND ADDRESS
12040	Natl Semiconductor Corp Commerce Drive P.O. Box 443 Danbury, CT 06810
12406	Elpac Electronics Inc. 3131 S. Standard Avenue Santa Ana, CA 92705
13919	Burr-Brown Research Corp 6730 S. Tucson Boulevard P.O. Box 11400 Tucson, AZ 85734
14655	Cornell-Dubilier Elect. Div. Fed. Pac. Elect. Co. Government Contracts Dept. 150 Avenue L Newark, NJ 07101
16299	AVX Corporation 3900 Electronics Drive Raleigh, NC 27604
17856	Siliconix Inc. 2201 Laurelwood Road Santa Clara, CA 95054
18310	Concord Electronics Corp. 30 Great Jones Street New York, NY 10012
18324	Great Western Chemical Co. 860 Wharf Richmond, CA 94804-3558
18565	Chomerics Inc. 77 Dragon Court Woburn, MA 01801
19420	Merrimack Magnetics Corp. 121 Hale Street Lowell, MA 01851
19648	Eldre Components Inc. 1500 Jefferson Road Rochester, NY 14623
22526	DuPont E I DE Nemours and Co. Inc. Advanced Products Div. Military Products Group 515 Fishing Creek Rd. New Cumberland, PA 17070-3007
24355	Analog Devices Route 1 Industrial Park P.O. Box 280 Norwood, MA 02062
24655	Genrad, Inc. Board Test Division 300 Baker Avenue Concord, MA 01742
25088	Siemens Corporation 186 Wood Avenue S. Iselin, NJ 08830
26394	Ansley Electronics Corp. Sub. of Thomas & Betts Doylestown, PA
26625	MIALUSA, Inc. Nutley, NJ
27014	National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051
27264	Molex Inc. Corporate Headquarters 2222 Wellington Court Lisle, IL 60532
28218	Minn. Mining and Mfg Co. Business Prods Sales Div. 3M Center St. Paul, MN 55144
28480	Hewlett-Packard Co. Corporate Headquarters 3000 Hanover Street Palo Alto, CA 94304

Table 6-29. List of Manufacturers (Continued)

FSCM	NAME AND ADDRESS
31019	Solid State Scientifics Commerce Drive Montgomeryville, PA 18936
31918	ITT Schadow, Inc. 8081 Wallace Road Eden Prairie, MN 55343
32293	Intersil Inc. Sub. of General Elec. Co. 10600 Ridgeview Court Cupertino, CA 95014-0104
32997	Bourns, Inc. Trimpot Division 1200 Columbia Avenue Riverside, CA 92507
34335	Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94086
34371	Harris Corp., Harris Semiconductor Prod. 200 Palm Bay Blvd. P.O. Box 883 Melbourne, FL 32901
49956	Raytheon Co. 141 Spring Street Lexington, MA 02173
51306	Samtan Engineering Corp. 127 Wyllis Avenue Malden, MA 02148
51406	Murata Erie No. America 1148 Franklin Rd. S. E. Marietta, GA 30067
52062	Magnet Pulse Technology 1999 Robert Street Riverside, CA 92507
52464	OKI Electronics of Am. 4031 NE 12th Terrace Fort Lauderdale, FL 33334
52752	Electro-Films, Inc. 111 Gilbane Street Marwick, RI
54453	Sullins Electronic Corp. 269 Pico Avenue P.O. Box 757 San Marcos, CA 92069
56289	Sprague Electric 87 Marshall Street North Adams, MA 01247
58361	General Instrument Optoelectronics Division 3400 Hillview Avenue Palo Alto, CA 94304
70255	Alco Controls, Div. of Emerson Electric Co. P.O. Box 12700 St. Louis, MO 63141
70903	Belden Corporation 2000 S. Batavia Avenue Geneva, IL 60134
71400	Bussman, Div. McGraw Edison co. P.O. Box 14460 St. Louis, MO 63178
71450	CTS Corporation 905 North West Blvd. Elkhart, IN 46514
71590	Mepco/Centralab A North Am. Philips Co. Hwy. 20W P.O. Box 858 Fort Dodge, IA 50501
72136	Electro Motive Corp. Subs. of Intl. Electronics Corp. P.O. Box 7600 Florence, SC 29501

Table 6-13. List of Manufacturers (Continued)

FSCM	NAME AND ADDRESS
72149	Electronic Transformer 460 Totowa Avenue Patterson, NJ 07511
72982	Erie Technological Prod. 645 W. 11th Street Erie, PA 16512
76381	Minnesota Mining & Mfg. 3M Center St. Paul, MN 55101
80183	Sprague Products Co. 87 Marshall St. North Adams, MA 02147
81040	Haddock Engineers Ltd. Montebello, CA
81073	Grayhill, Inc. P.O. Box 373 561 Hillgrove Avenue LaGrange, IL 60525
81349	Military specifications promulgated by military departments/agencies under authority of Defense Standardization Manual 4120 3-M.
81483	International Rectifier P.O.B. 2321 Terminal Annex 9220 Sunset Boulevard Los Angeles, CA 90069
84171	Arco Electronics 400 Moreland Road Commack, NY 11725
84411	American Shizuki Corp 301 W. O St. Ogallala, NE 69153-1844
90201	Mallory Capacitor Co. Div. P.R. Mallory and Co. 4760 Kentucky Avenue P.O. Box 372 Indianapolis, IN 46206
91293	Johanson Manufacturing Co. P.O. Box 329 Boonton, NJ 07005
91506	Augat, Inc. 33 Perry Avenue P.O. Box 779 Attleboro, MA 02703
91637	Dale Electronics Inc. P.O. Box 609 Columbus, NE 68601
92702	IMC Magnetics Corp. Eastern Division 570 Main Street Westbury, NY 11591
93652	Dietz Design Inc. 100 Electronics Parkway Belton, MO 64012
95348	Gordos Corp. 250 Greenwood Ave Bloomfield, NJ 07003-2416
95750	Republic Electric Ind.Inc. 575 Broad Hollow Road Melville, NY 11746
96906	Military standards promulgated by military departments under authority of Defense Standardization Manual 4120 3-M applies to book form documents that establish engineering and technical limitations and applications for items and which are identified by numbers such as MIL-STD-198 and MIL-STD-242, etc. Also sheet form documents that depict design criteria for items and which are identified by numbers such as MS 3057 and MS 75052 etc.

Table 6-29. List of Manufacturers (Continued)

FSCM	NAME AND ADDRESS
AAAAA	NIC Components Corporation 6000 New Horizons Blvd. North Amityville, NY 11701
BBBBB	Hitachi America Ltd. 1800 Bering Drive San Jose, CA 95112
CCCCC	Lite-On Corp. (USA) Parkway Business Ctr.1 Suite 570 4950 Airport Parkway Dallas, TX 75248
DDDDD	AVX Ceramics Div. of AVX Corp. Seneca Avenue Olean, NY 14760
EEEEE	H & T Components 87 Sand Pit Road Danbury, CT 06810
FFFFF	Aptronics Div. of AP Products Inc. 9450 Pineneedle Drive P.O. Box 540 Mentor, OH 44060
GGGGG	EURO-DIP 1565 W. University Dr. Tempe, AZ 85281

MODEL 2250

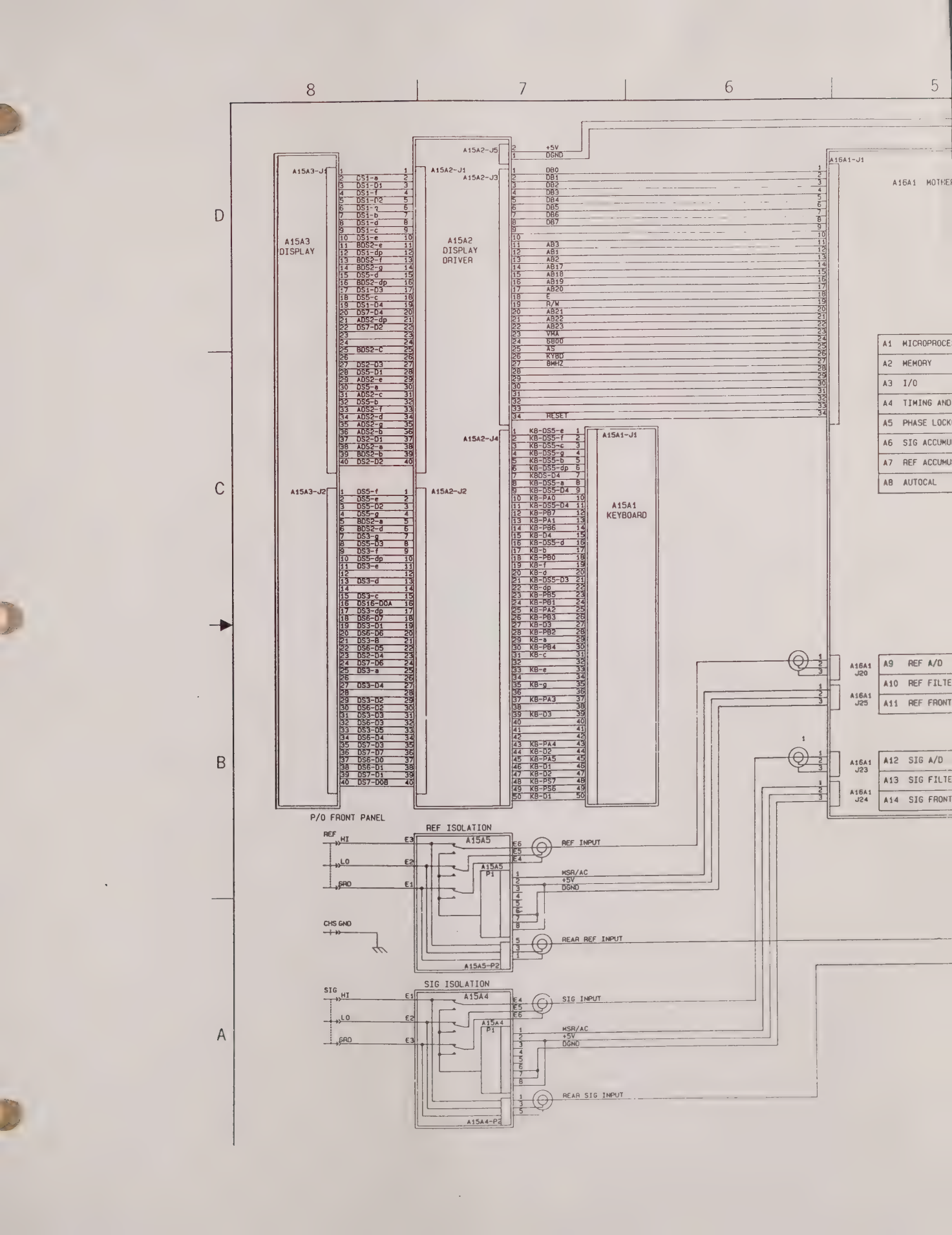
SECTION 7

SCHEMATIC DIAGRAMS

7-1. INTRODUCTION.

This section contains schematic diagrams for the Model 2250 Digital Analyzing Voltmeter.

FIGURE	DWG. NO./REV.	TITLE	PAGE
7-1	768928/B	Model 2250 DAV Interconnection Diagram	7-3/(7-4 blank)
7-2	768861/F	Microprocessor Circuit Card Assembly (CCA) A1	7-5/(7-6 blank)
7-3	768880-4/A	Memory CCA A2	7-7/(7-8 blank)
7-4	768882-2/B	I/O CCA A3	7-11/(7-12 blank)
7-5	768879-1/D	Timing and Control CCA A4	7-15/(7-16 blank)
7-6	768878-1/D	Phase-Locked Loop CCA A5	7-21/(7-22 blank)
7-7	768865-1/A	Accumulator CCA A6, A7	7-25/(7-26 blank)
7-8	768877-2/A	Auto Calibration CCA A8	7-29/(7-30 blank)
7-9	768987/D	A/D Converter CCA A9, A12	7-31/(7-32 blank)
7-10	768930-1/E	Front End CCA A11, A14	7-35/(7-36 blank)
7-11	768862/D	Display Driver CCA A15A2	7-37/(7-38 blank)
7-12	768864/D	Display CCA A15A3	7-41/(7-42 blank)
7-13	768910/D	Isolation CCA A15A4, A15A5	7-43/(7-44 blank)
7-14	768866/J	Mother Board A16A1	7-45/(7-46 blank)
7-15	768983/B	Recorder Filter Assembly A17A1	7-47/(7-48 blank)
7-16	768863/H	Main Power Supply CCA A17PS1	7-49/(7-50 blank)
7-17	768876-1/A	Isolated Power Supply A17PS2A1, A17PS3A1	7-51/(7-52 blank)


A15A3 DISPLAY
A15A2 DISPLAY DRIVER
A15A1 KEYBOARD
A16A1 MOTHER
A15A3-J1
A15A3-J2
A15A2-J1
A15A2-J2
A15A2-J3
A15A2-J4
A15A2-J5
A15A1-J1
A16A1-J1
P/O FRONT PANEL
REF ISOLATION
SIG ISOLATION
A15A5
A15A4
REF INPUT
SIG INPUT
REAR REF INPUT
REAR SIG INPUT
MSR/AC
+5V
DGND
CHS GND
A1 MICROPROCE
A2 MEMORY
A3 I/O
A4 TIMING AND
A5 PHASE LOCK
A6 SIG ACCUMU
A7 REF ACCUMU
A8 AUTOCAL
A9 REF A/D
A10 REF FILTE
A11 REF FRONT
A12 SIG A/D
A13 SIG FILTE
A14 SIG FRONT

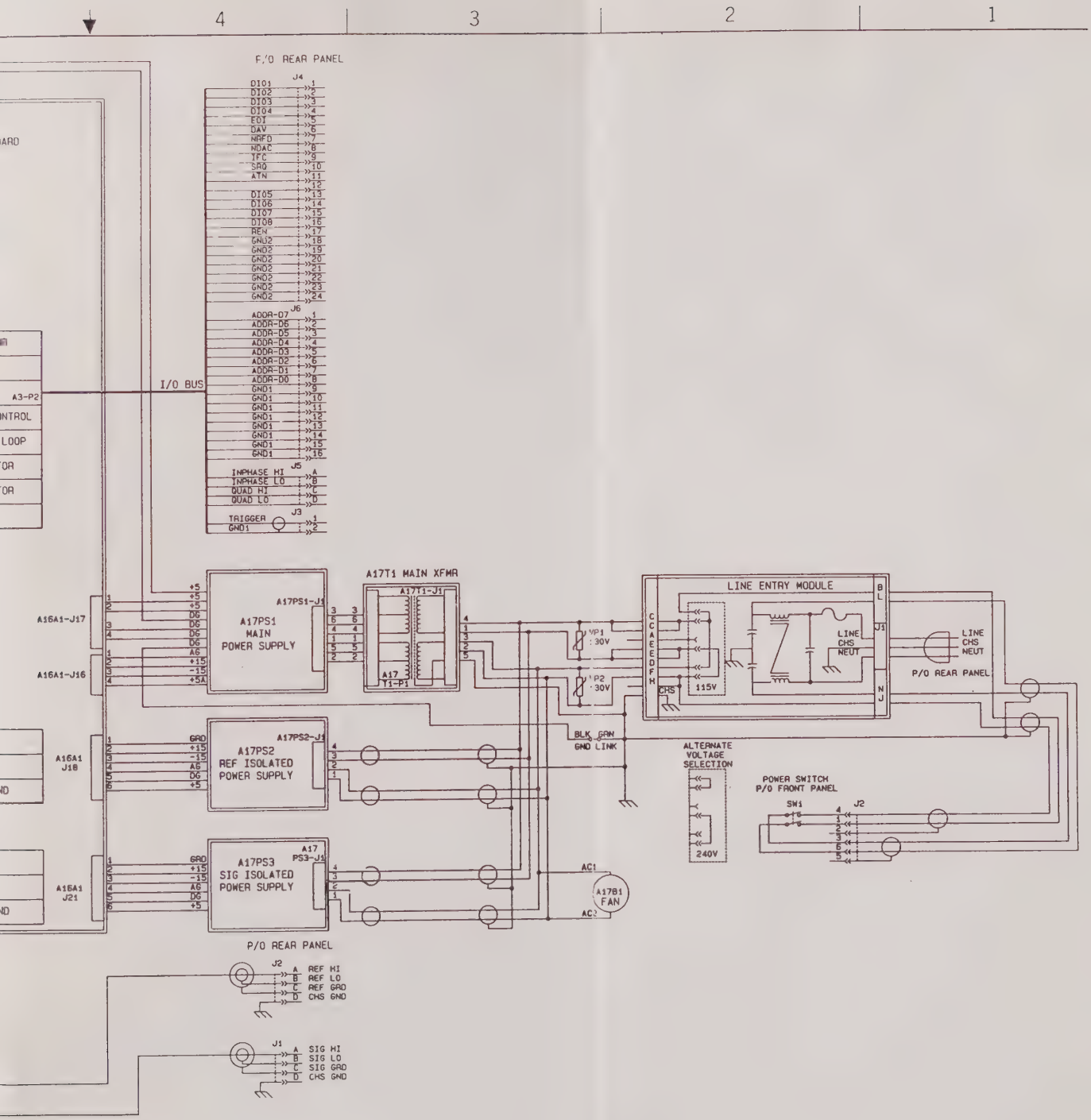
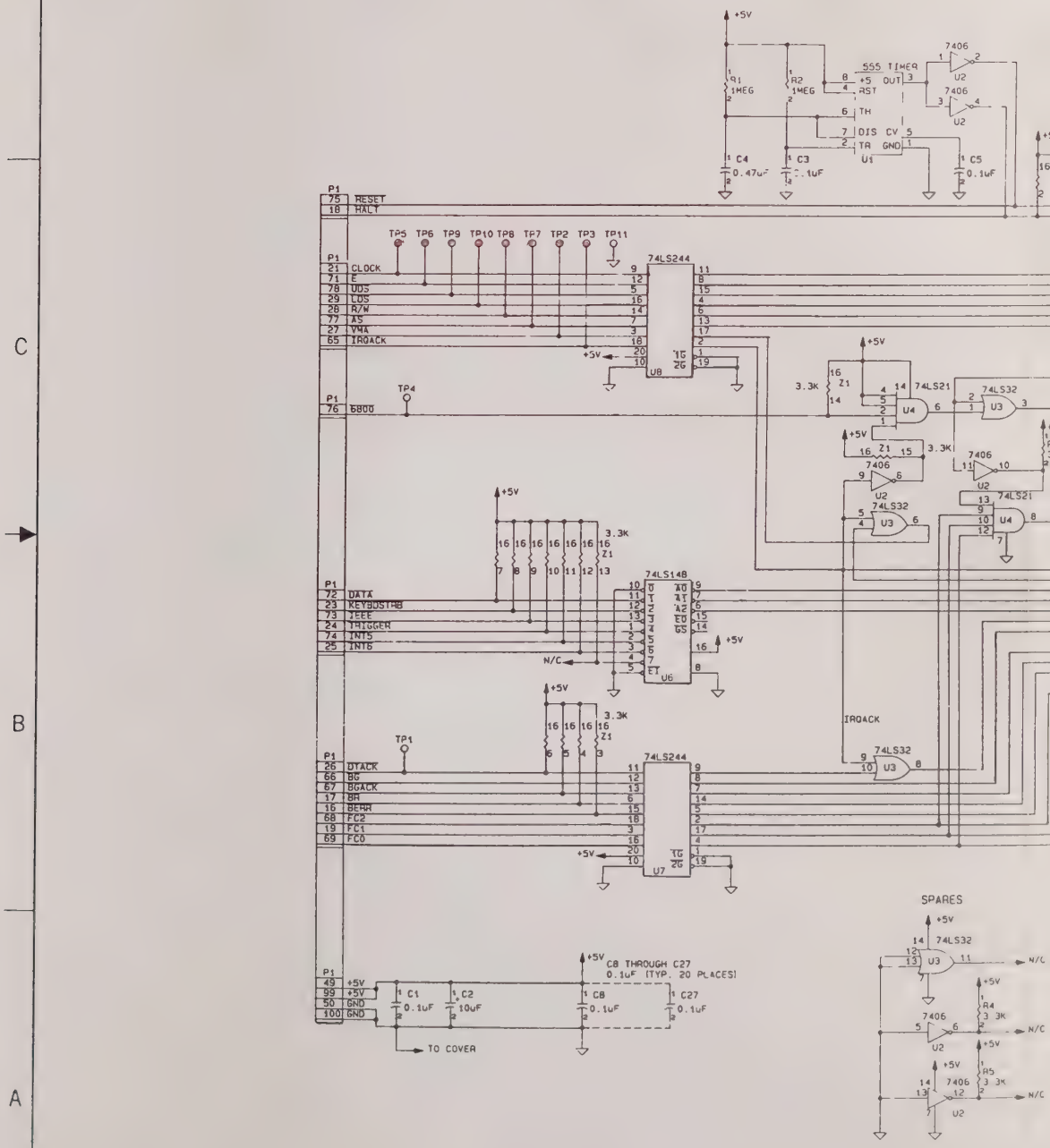


Figure 7-1. Model 2250 DAV Interconnection Diagram Schematic Diagram 768928/B


8
7
6
5
D
C
B
A
+5V
555 TIMER
R1 1MEG
R2 1MEG
C4 0.47uF
C3 .1uF
C5 0.1uF
U1
7406
U2
P1
75 RESET
18 HALT
21 CLOCK
71 E
78 UDS
29 LDS
28 R/W
77 AS
27 VMA
65 IRQACK
76 6800
72 DATA
23 KEYBDSTRB
73 IEEE
24 TRIGGER
74 INT5
25 INT6
26 DTACK
66 BG
67 BGACK
17 BR
16 BERR
68 FC2
19 FC1
69 FC0
49 +5V
99 +5V
50 GND
100 GND
TP1
TP2
TP3
TP4
TP5
TP6
TP9
TP10
TP8
TP7
TP11
74LS244
U8
U7
74LS148
U6
74LS21
U4
74LS32
U3
3.3K
Z1
N/C
IRQACK
C1 0.1uF
C2 10uF
C8 0.1uF
C27 0.1uF
C8 THROUGH C27
0.1uF (TYP. 20 PLACES)
TO COVER
SPARES
R4 3.3K
R5 3.3K

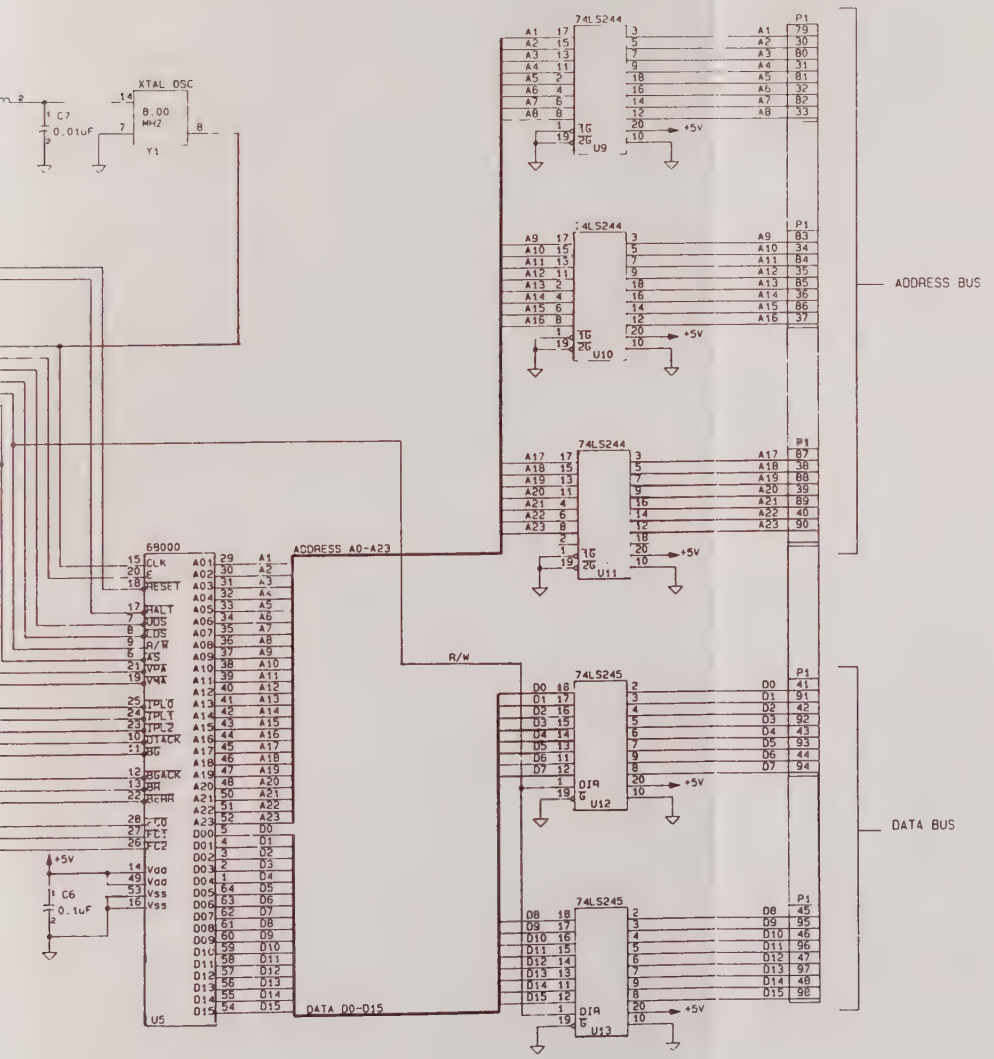
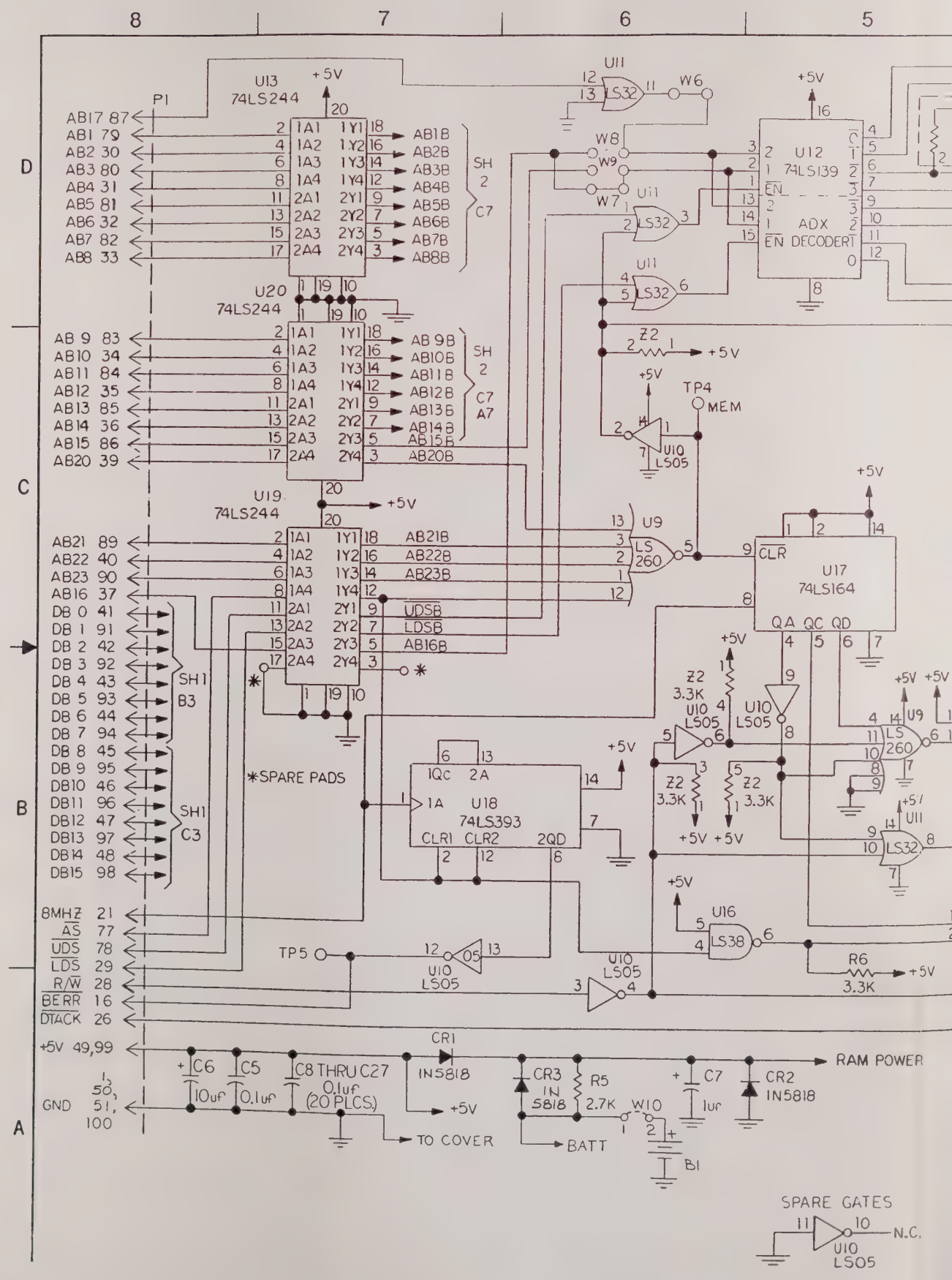
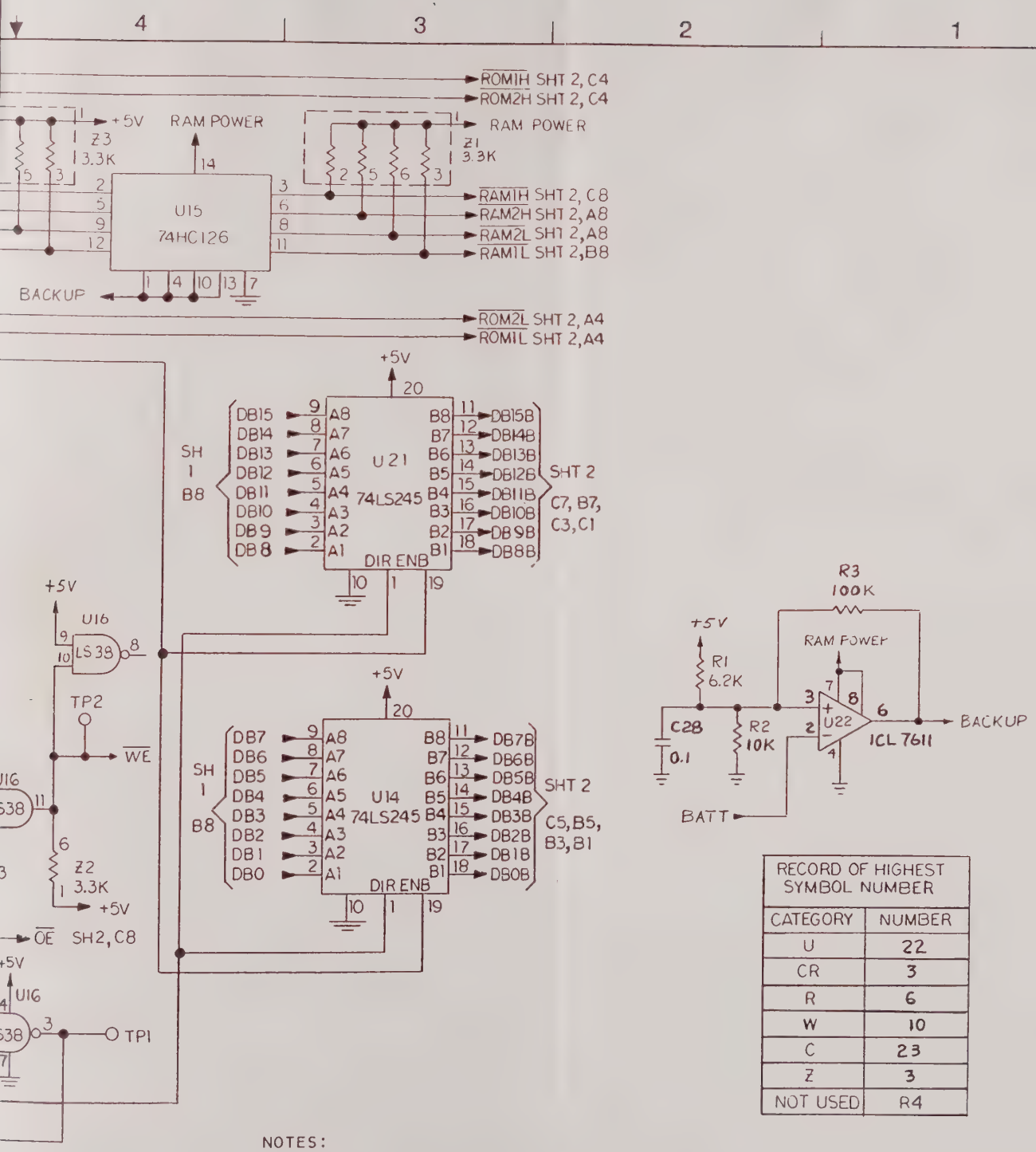


Figure 7-2. Microprocessor Circuit Card Assembly (CCA) A1 (P/N 787170), Schematic Diagram 768861/F

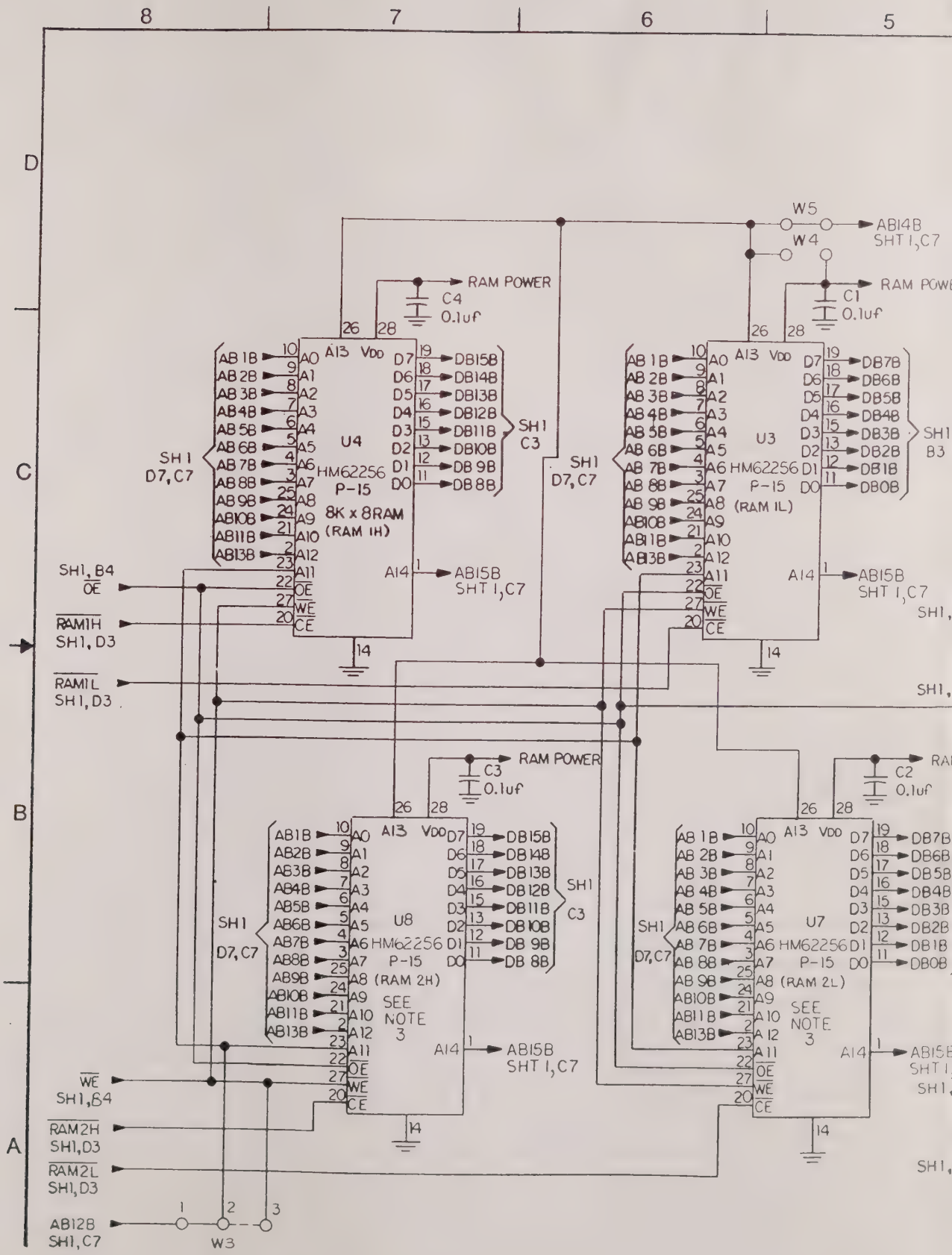

8
7
6
5
D
C
B
A
P1
U13
74LS244
+5V
AB17 87
AB1 79
AB2 30
AB3 80
AB4 31
AB5 81
AB6 32
AB7 82
AB8 33
AB1B
AB2B
AB3B
AB4B
AB5B
AB6B
AB7B
AB8B
SH 2 C7
U20
74LS244
AB 9 83
AB10 34
AB11 84
AB12 35
AB13 85
AB14 36
AB15 86
AB20 39
AB 9B
AB10B
AB11B
AB12B
AB13B
AB14B
AB15B
AB20B
SH 2 C7 A7
U19
74LS244
AB21 89
AB22 40
AB23 90
AB16 37
AB21B
AB22B
AB23B
AB16B
UDSB
LDSB
DB 0 41
DB 1 91
DB 2 42
DB 3 92
DB 4 43
DB 5 93
DB 6 44
DB 7 94
DB 8 45
DB 9 95
DB10 46
DB11 96
DB12 47
DB13 97
DB14 48
DB15 98
SH1 B3
SH1 C3
*SPARE PADS
8MHZ 21
AS 77
UDS 78
LDS 29
R/W 28
BERR 16
DTACK 26
+5V 49,99
GND 1, 50, 51, 100
U11
LS32
W6
W8
W9
W7
U12
74LS139
ADX DECODER
Z2
TP4
MEM
U10
LS05
U9
LS 260
U17
74LS164
QA QC QD
CLR
Z2 3.3K
U18
74LS393
CLR1 CLR2 2QD
1QC 2A 1A
U16
LS38
R6
3.3K
TP5
C6 10uf
C5 0.1uf
C8 THRU C27 0.1uf (20 PLCS.)
TO COVER
CR1 IN5818
CR3 IN 5818
R5 2.7K
W10
BATT
B1
C7 1uf
CR2 IN5818
RAM POWER
SPARE GATES
N.C.



RECORD OF HIGHEST SYMBOL NUMBER	
CATEGORY	NUMBER
U	22
CR	3
R	6
W	10
C	23
Z	3
NOT USED	R4

NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS 1/4 W ±5% AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. THIS BOARD NORMALLY HAS CONNECTIONS FOR 256 K DEVICES. TO USE 64 K AND 128 K DEVICES CUT W2,5,6 & 7 AND JUMP W1,4,8 & 9.
3. COMPONENT NOT USED IN CURRENT VERSION.

Figure 7-3. Memory CCA A2 (P/N 787171-4), Schematic Diagram 768880-4/A (Sheet 1 of 2)


8
7
6
5
D
C
B
A
W5
W4
AB14B
SHT 1,C7
RAM POWER
C4
0.1uf
C1
0.1uf
C3
0.1uf
C2
0.1uf
U4
U3
U8
U7
HM62256
P-15
8K x 8RAM
(RAM 1H)
(RAM 1L)
(RAM 2H)
(RAM 2L)
SEE NOTE 3
SH1 D7,C7
SH1 C3
SH1 B3
SH1,B4
OE
WE
CE
RAM1H
SH1,D3
RAM1L
SH1,D3
RAM2H
SH1,D3
RAM2L
SH1,D3
AB15B
SHT 1,C7
AB12B
SH1,C7
W3
DB15B
DB14B
DB13B
DB12B
DB11B
DB10B
DB 9B
DB 8B
DB7B
DB6B
DB5B
DB4B
DB3B
DB2B
DB1B
DB0B

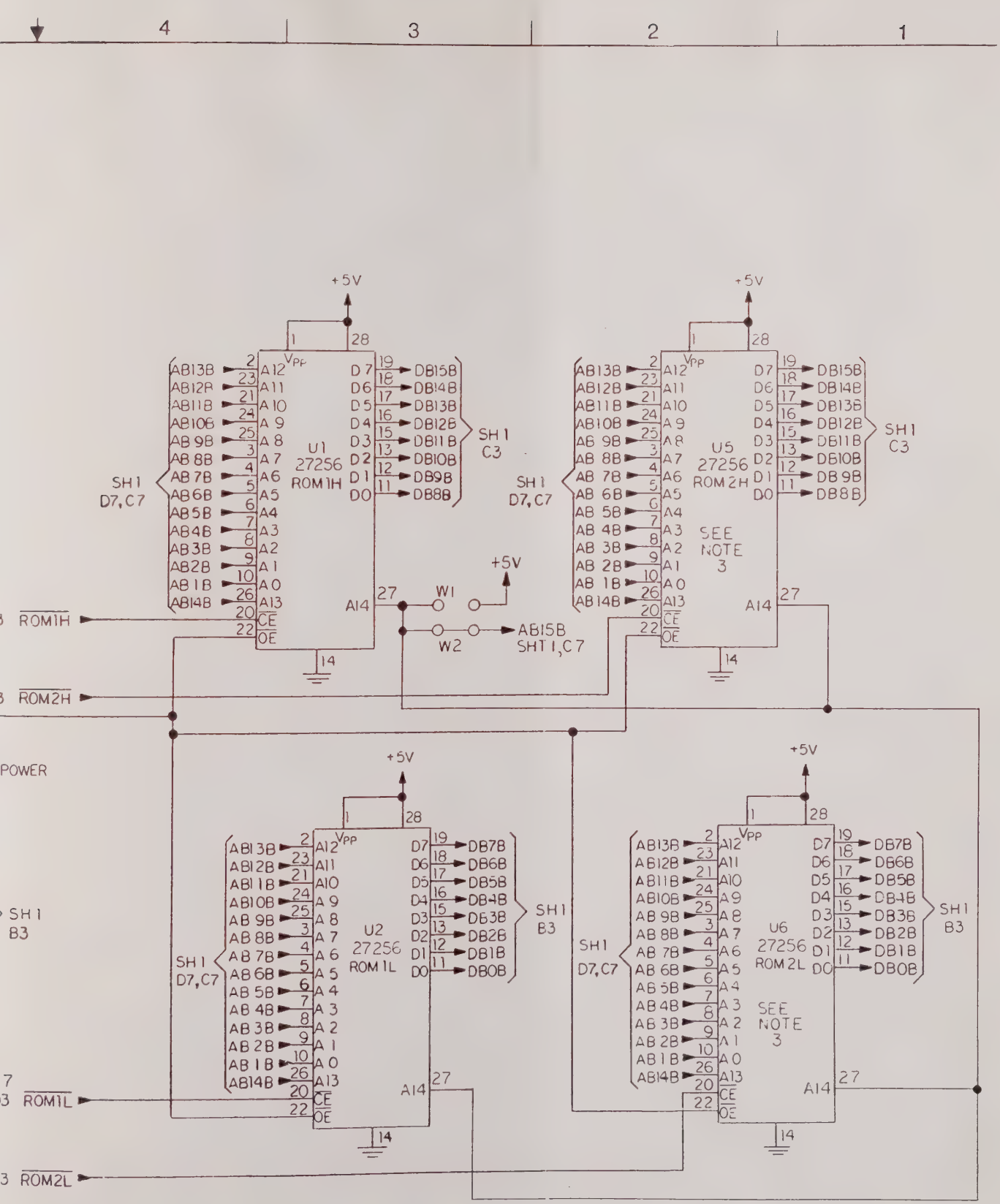
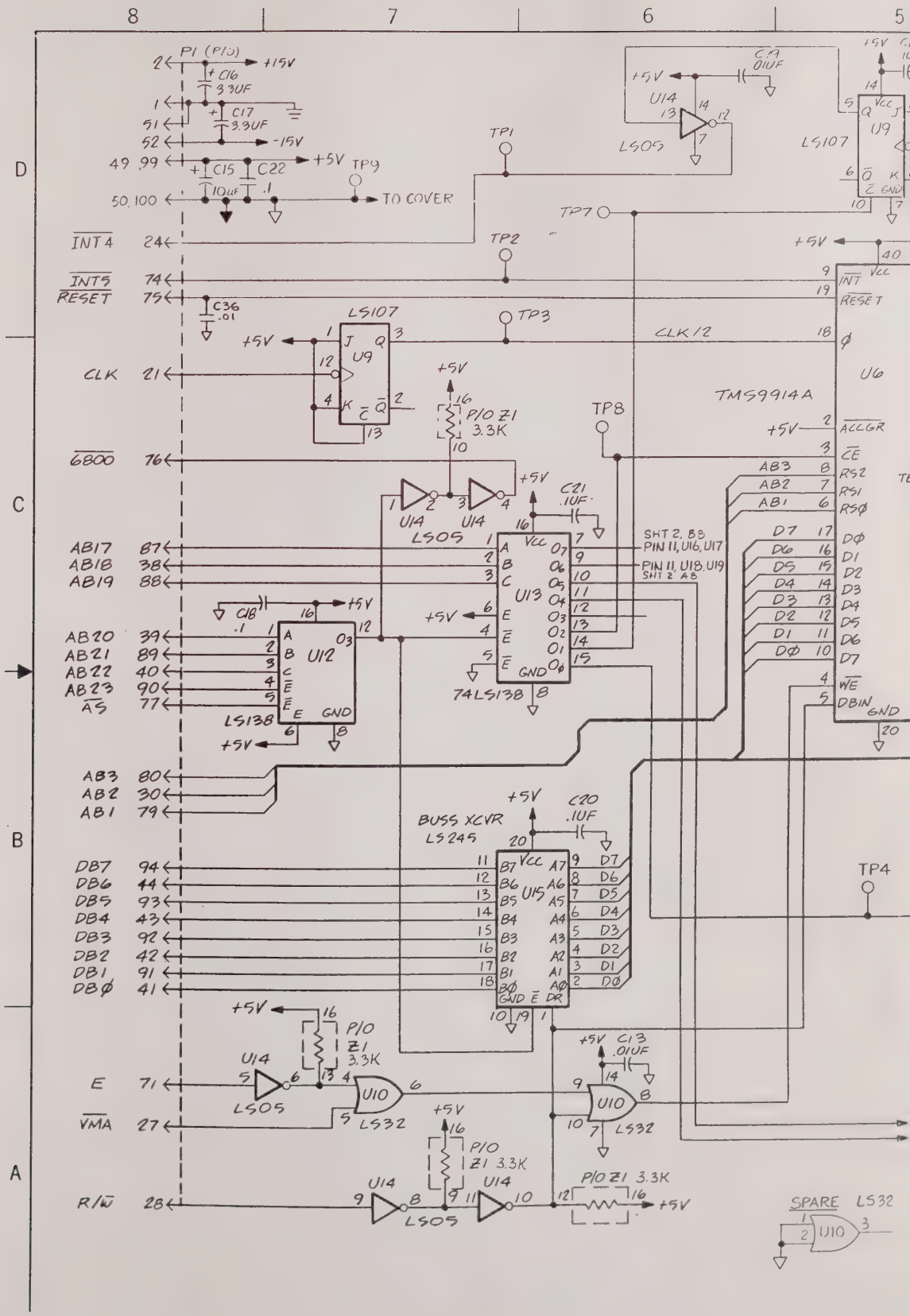
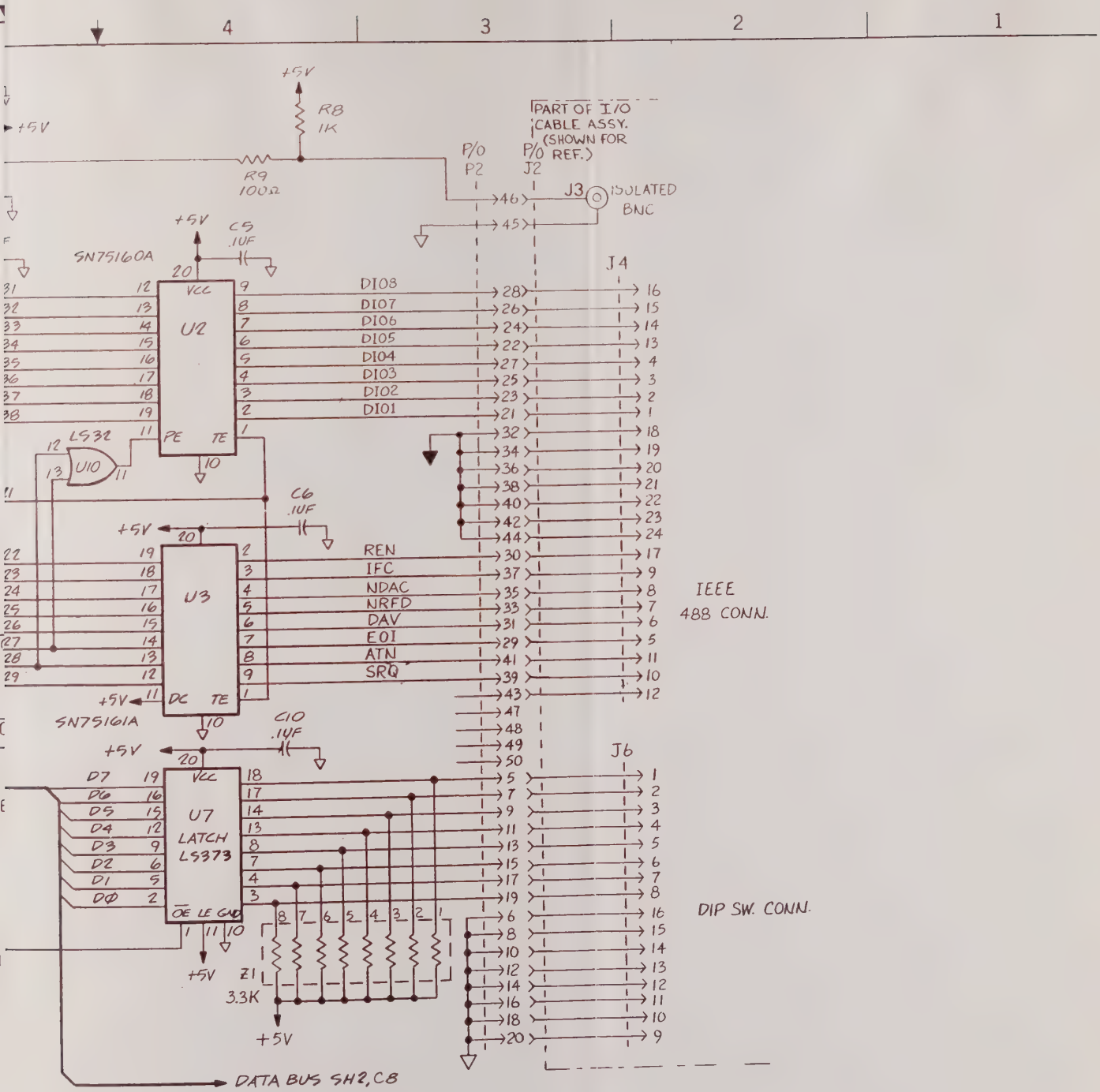


Figure 7-3. Memory CCA A2 (P/N 787171-4), Schematic Diagram 768880-4/A (Sheet 2 of 2)

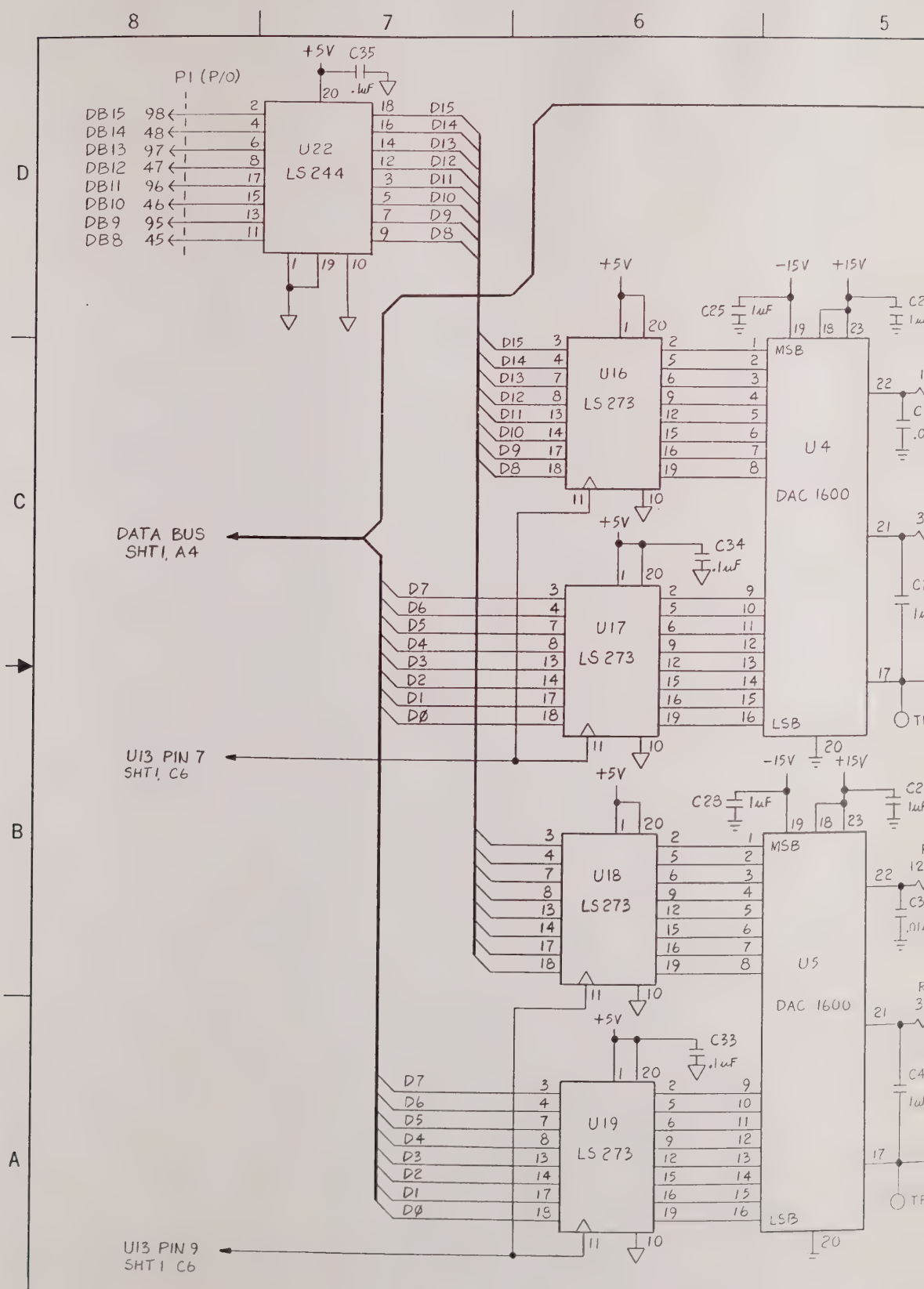

8
7
6
5
D
C
B
A
P1 (P10)
+15V
C16 3.3UF
C17 3.3UF
-15V
+5V
C15
C22
10uF
.1
TP9
TO COVER
TP1
TP2
TP3
TP7
TP8
TP4
INT4
INTS
RESET
C36 .01
LS107
U9
CLK
CLK/2
6800
P/O Z1 3.3K
U14
LS05
C21 .1UF
U13
74LS138
SHT 2, B8
PIN 11, U16, U17
PIN 11, U18, U19
SHT 2 AB
U6
TMS9914A
ACCLGR
CE
RS2
RS1
RSØ
DØ
D1
D2
D3
D4
D5
D6
D7
WE
DBIN
GND
C18 .1
U12
LS138
AB17
AB18
AB19
AB20
AB21
AB22
AB23
AS
AB3
AB2
AB1
BUSS XCVR
LS245
C20 .1UF
U15
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
E
VMA
R/W
U10
LS32
C19 .01UF
C13 .01UF
SPARE LS32



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W ±5%.
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS.

Figure 7-4. I/O CCA A3 (P/N 787172-2), Schematic Diagram 768882-2/B (Sheet 1 of 2)


8
7
6
5
D
C
B
A
P1 (P/O)
DB15 98
DB14 48
DB13 97
DB12 47
DB11 96
DB10 46
DB9 95
DB8 45
+5V
C35
.1uF
U22
LS244
DATA BUS
SHT1, A4
U16
LS273
U17
LS273
U18
LS273
U19
LS273
C34
C33
C28
C25
1uF
-15V
+15V
U4
DAC 1600
U5
DAC 1600
MSB
LSB
U13 PIN 7
SHT1, C6
U13 PIN 9
SHT1 C6

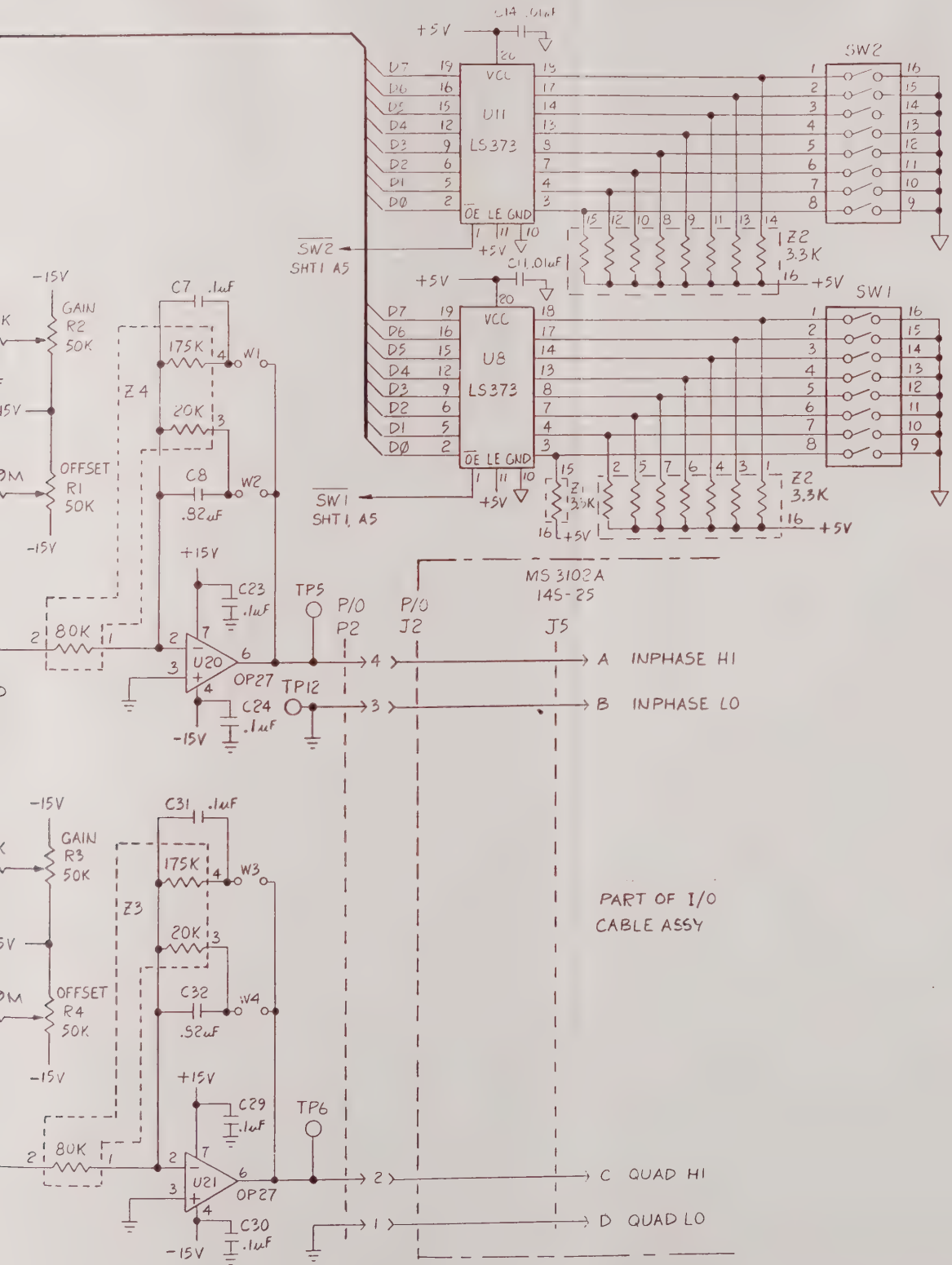
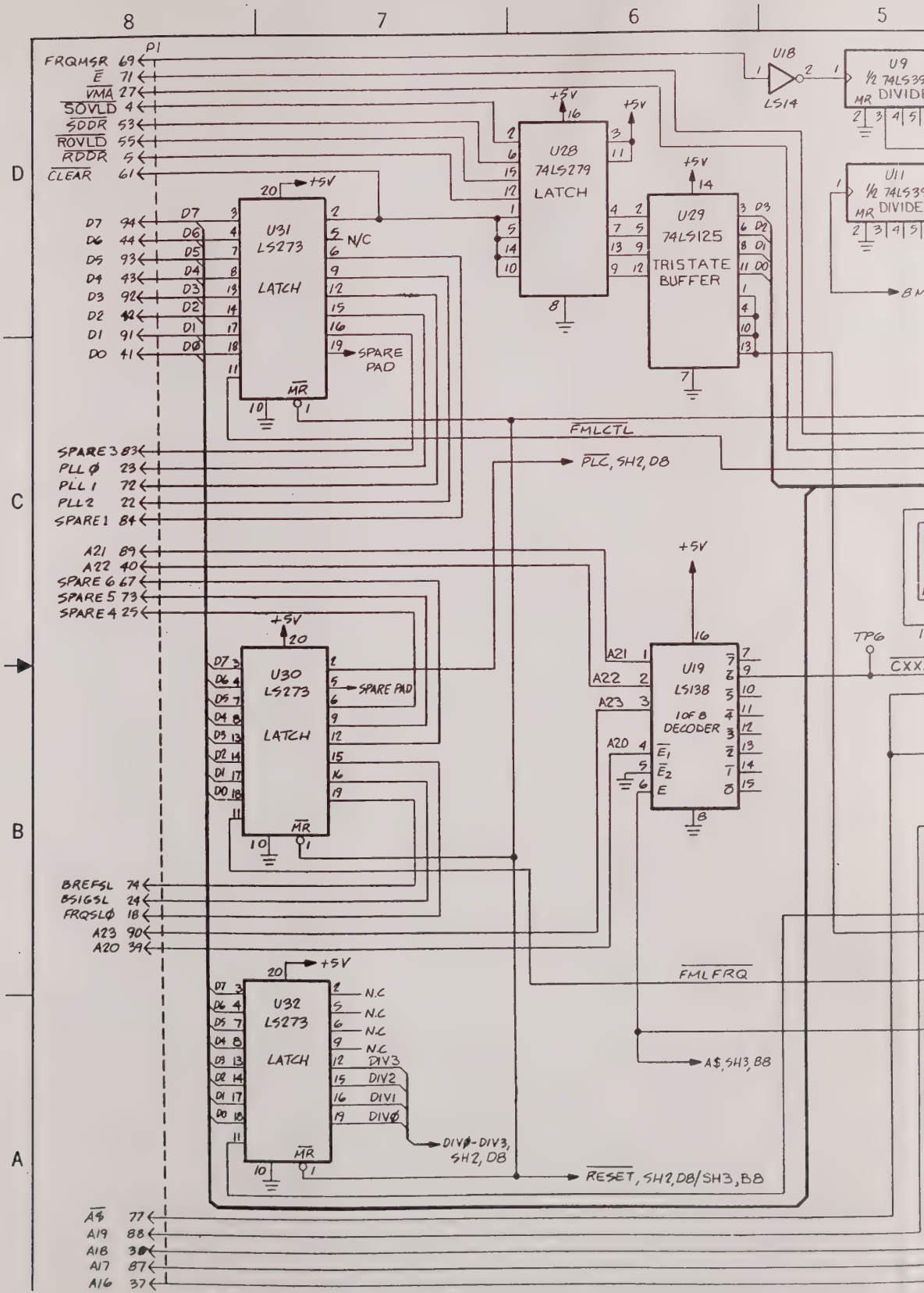
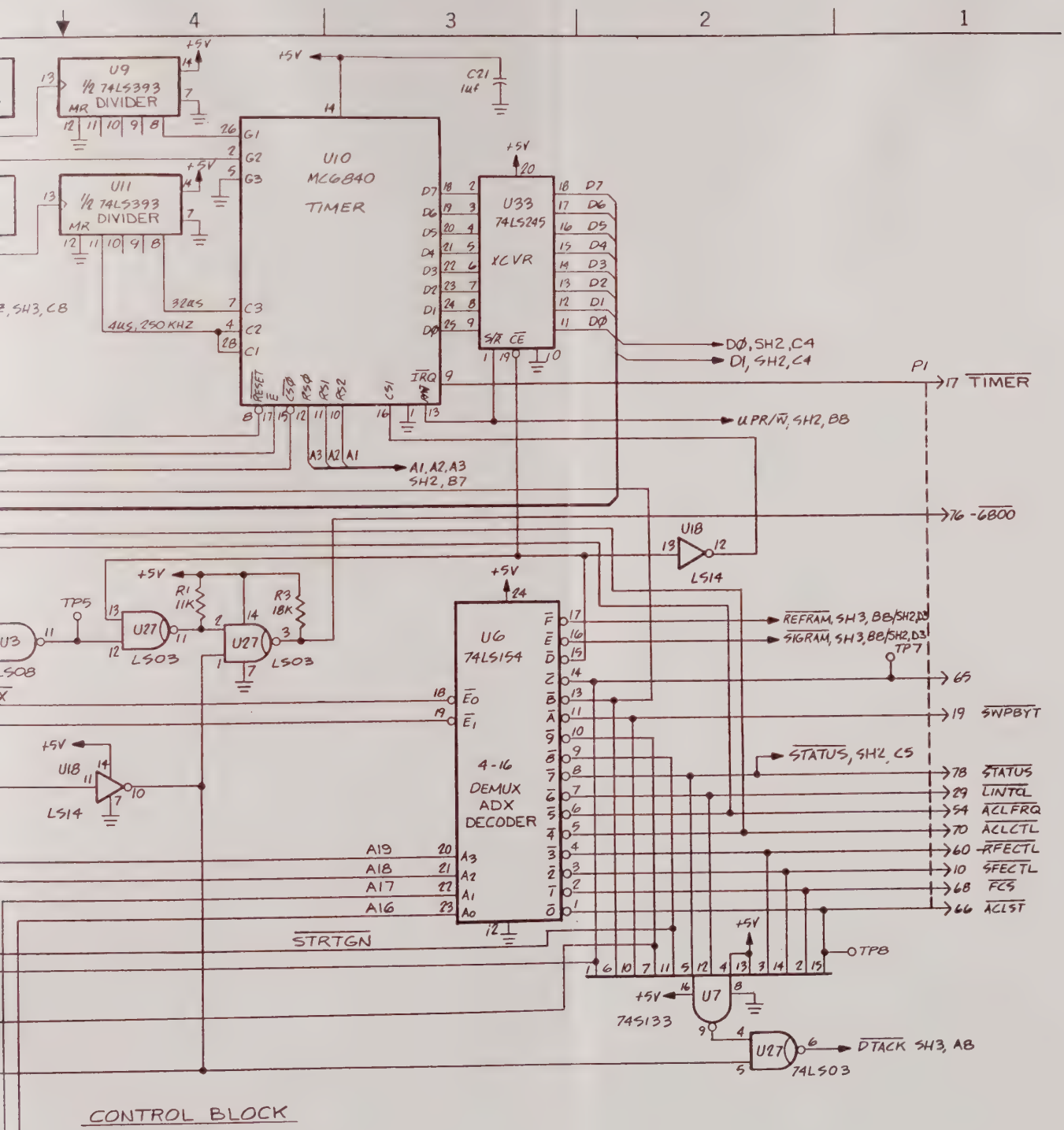


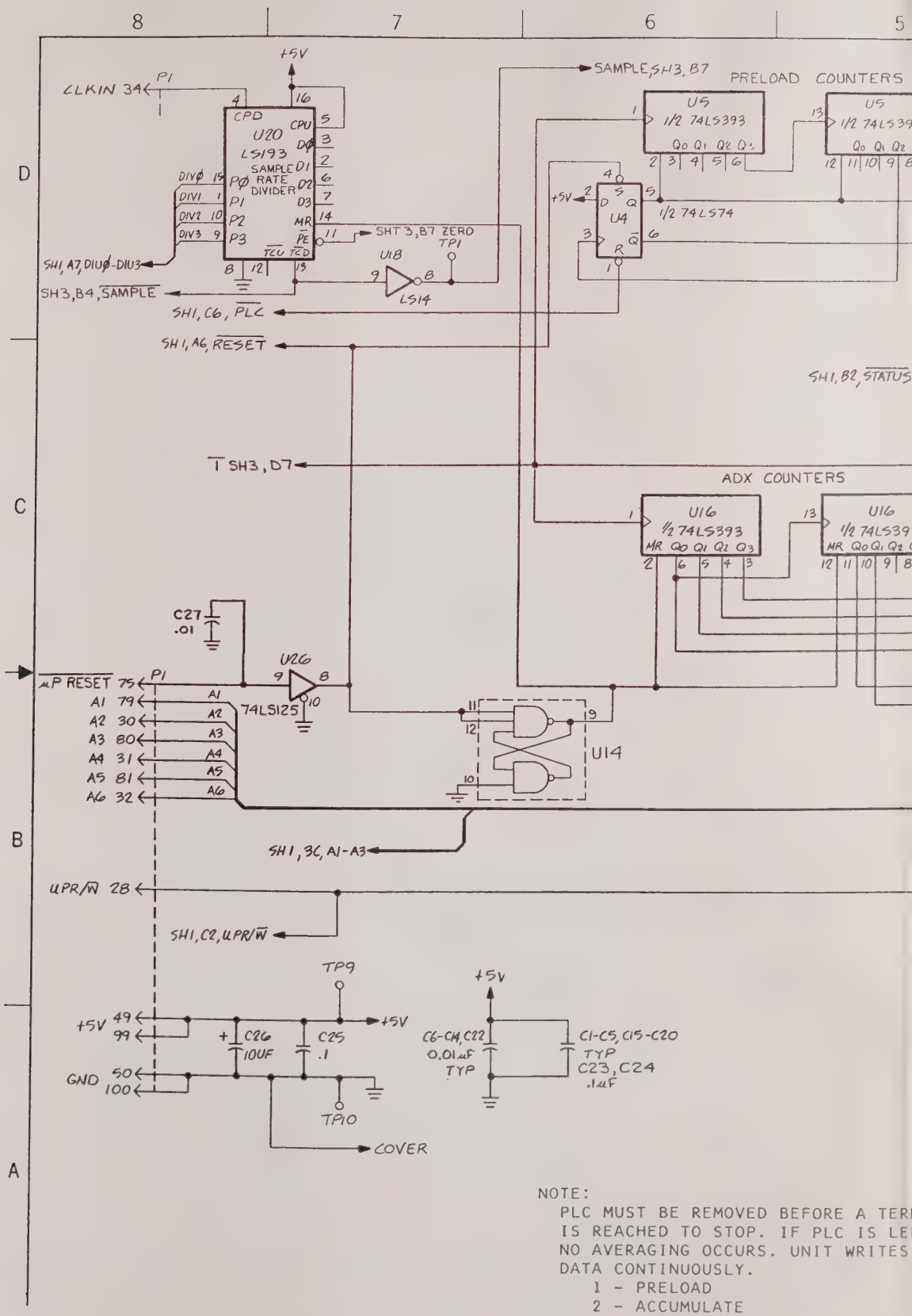
Figure 7-4. I/O CCA A3 (P/N 787172-2), Schematic Diagram 768882-2/B (Sheet 2 of 2)


8
7
6
5
D
C
B
A
P1
FRQMSR 69
E 71
VMA 27
SOVLD 4
SDDR 53
ROVLD 55
RDDR 5
CLEAR 61
U18
LS14
U9
1/2 74LS39
MR
DIVIDE
U11
1/2 74LS39
MR
DIVIDE
8M
+5V
U28
74LS279
LATCH
U29
74LS125
TRISTATE
BUFFER
U31
LS273
LATCH
N/C
SPARE
PAD
D7 94
D6 44
D5 93
D4 43
D3 92
D2 42
D1 91
D0 41
FMLCTL
PLC, SH2, DB
SPARE3 83
PLL Ø 23
PLL 1 72
PLL2 22
SPARE1 84
A21 89
A22 40
SPARE 6 67
SPARE 5 73
SPARE 4 25
U30
LS273
LATCH
SPARE PAD
U19
LS138
1 OF 8
DECODER
A21
A22
A23
A20
TP6
CXX
BREFSL 74
BSIGSL 24
FRQSLØ 18
A23 90
A20 39
U32
LS273
LATCH
N.C
DIV3
DIV2
DIV1
DIVØ
DIVØ-DIV3,
SH2, DB
FMLFRQ
A$, SH3, B8
RESET, SH2, DB/SH3, B8
A$ 77
A19 88
A18 38
A17 87
A16 37

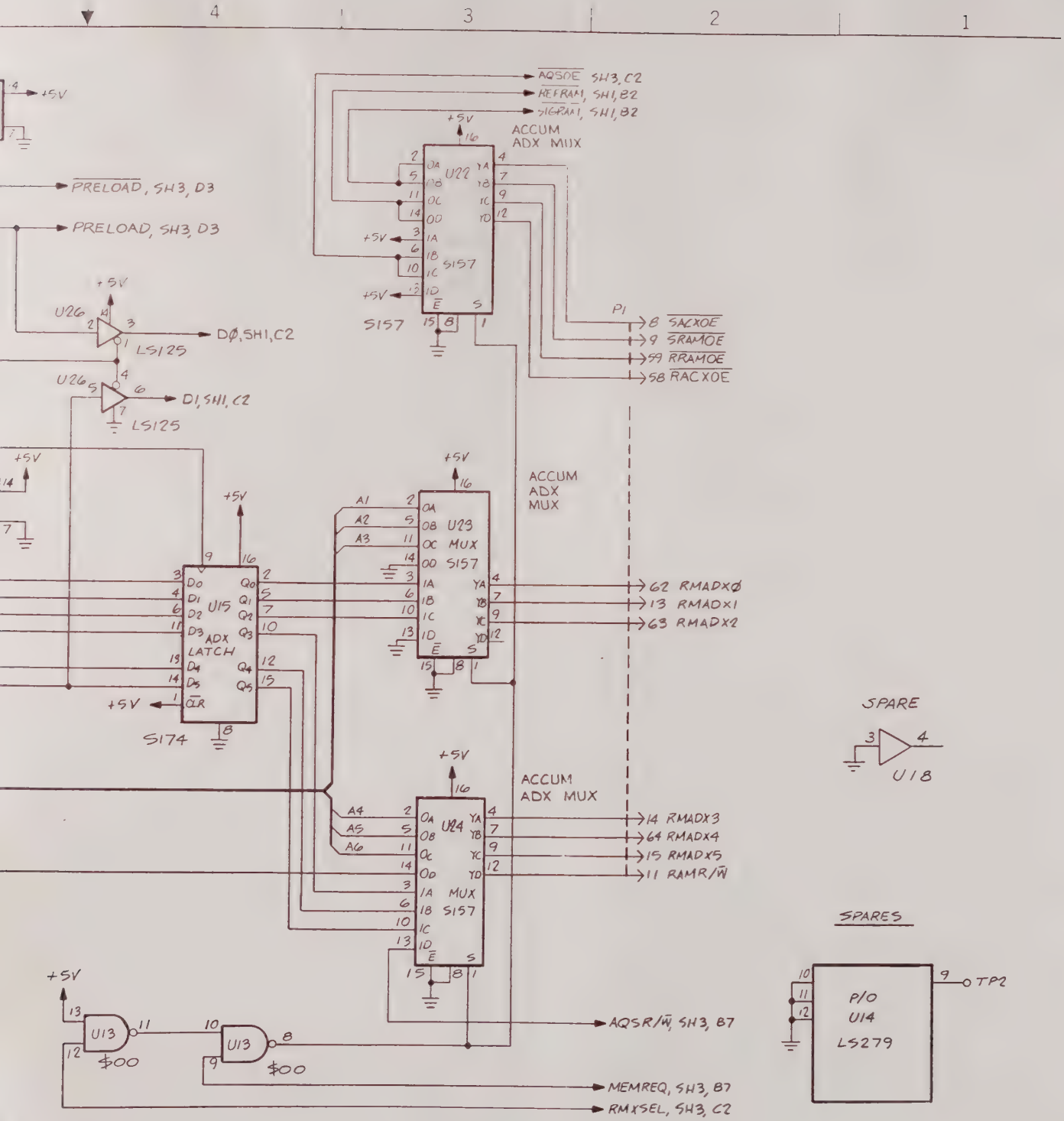


CONTROL BLOCK

Figure 7-5. Timing and Control CCA A4 (P/N 787173-1), Schematic Diagram 768879-1/D (Sheet 1 of 3)



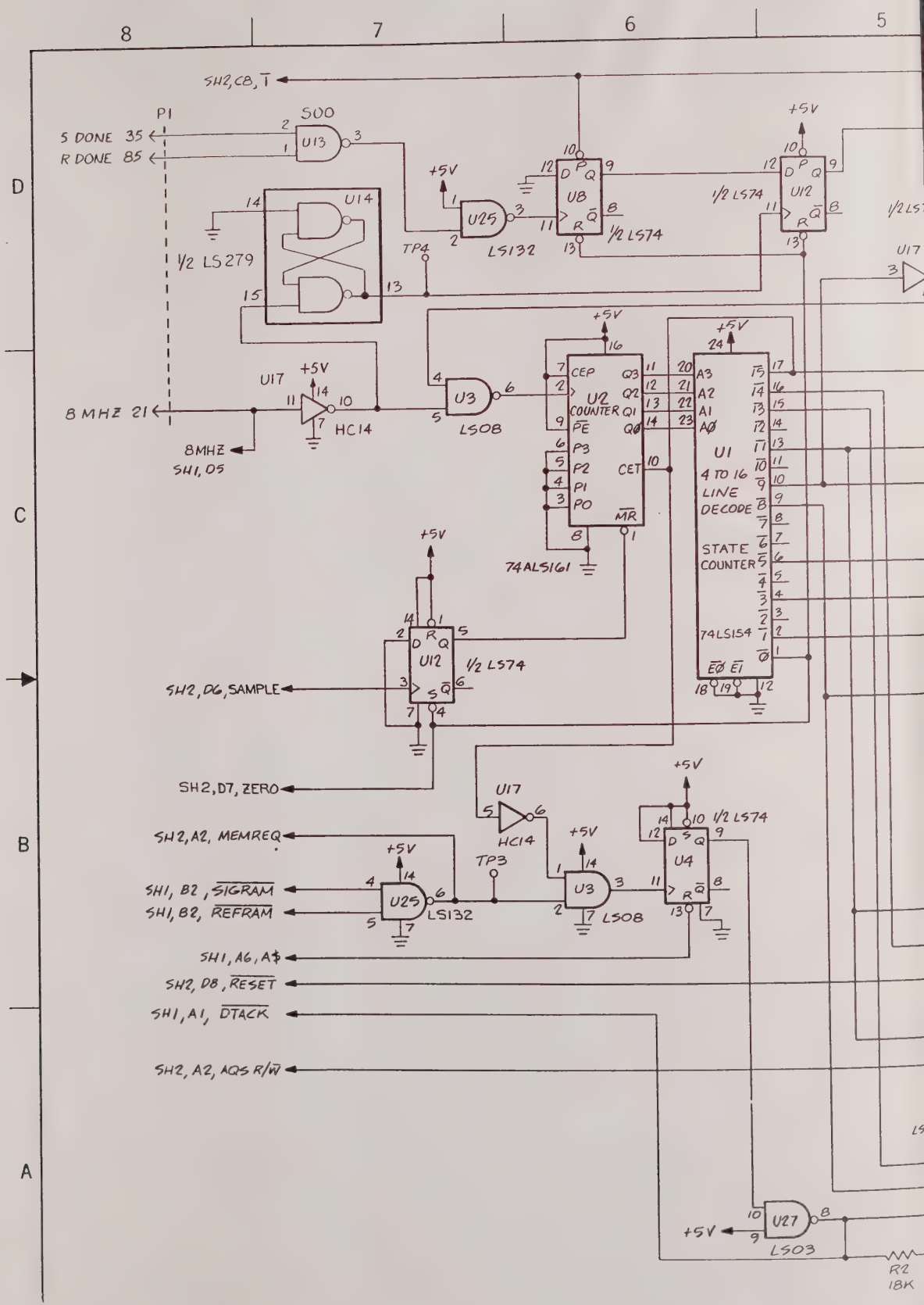
NOTE:
PLC MUST BE REMOVED BEFORE A TER
IS REACHED TO STOP. IF PLC IS LE
NO AVERAGING OCCURS. UNIT WRITES
DATA CONTINUOUSLY.
1 - PRELOAD
2 - ACCUMULATE



NAL COUNT
APPLIED,
VER OLD

DATA ACQUISITION BLOCK

Figure 7-5. Timing and Control CCA A4 (P/N 787173-1), Schematic Diagram 768879-1/D (Sheet 2 of 3)


8
7
6
5
D
C
B
A
SH2,C8,T
P1
S DONE 35
R DONE 85
500
U13
1/2 LS279
U14
TP4
+5V
U25
LS132
U8
1/2 LS74
U12
1/2 LS74
U17
8 MHZ 21
8MHZ
SH1,05
HC14
U3
LS08
U2
COUNTER
74ALS161
CEP
CET
MR
PE
P3
P2
P1
P0
Q3
Q2
Q1
Q0
U1
4 TO 16
LINE
DECODE
STATE
COUNTER
74LS154
A3
A2
A1
A0
SH2,D6,SAMPLE
SH2,D7,ZERO
SH2,A2,MEMREQ
SH1,B2,SIGRAM
SH1,B2,REFRAM
TP3
U4
SH1,A6,A$
SH2,D8,RESET
SH1,A1,DTACK
SH2,A2,AQS R/W
U27
LS03
R2
18K

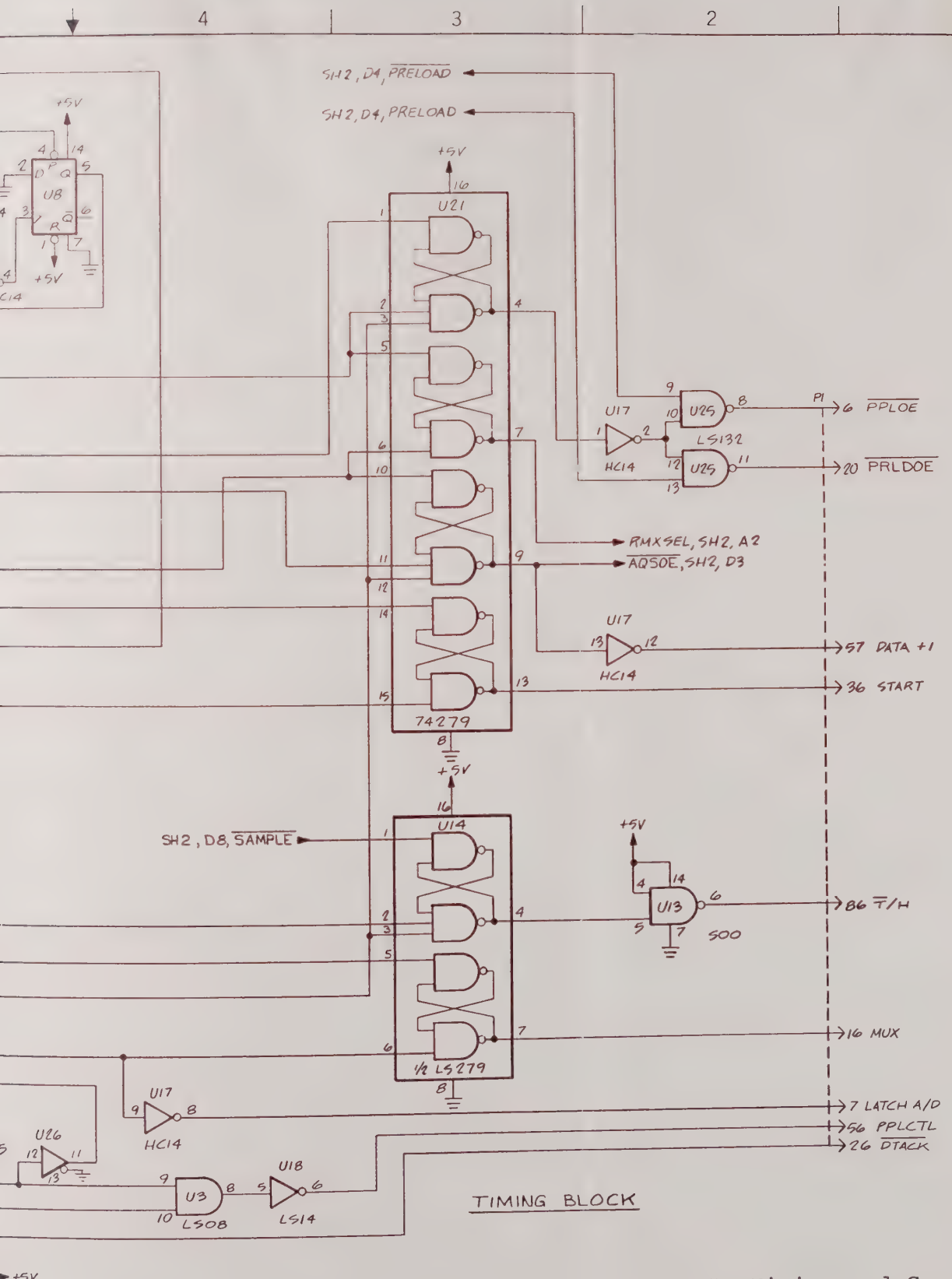
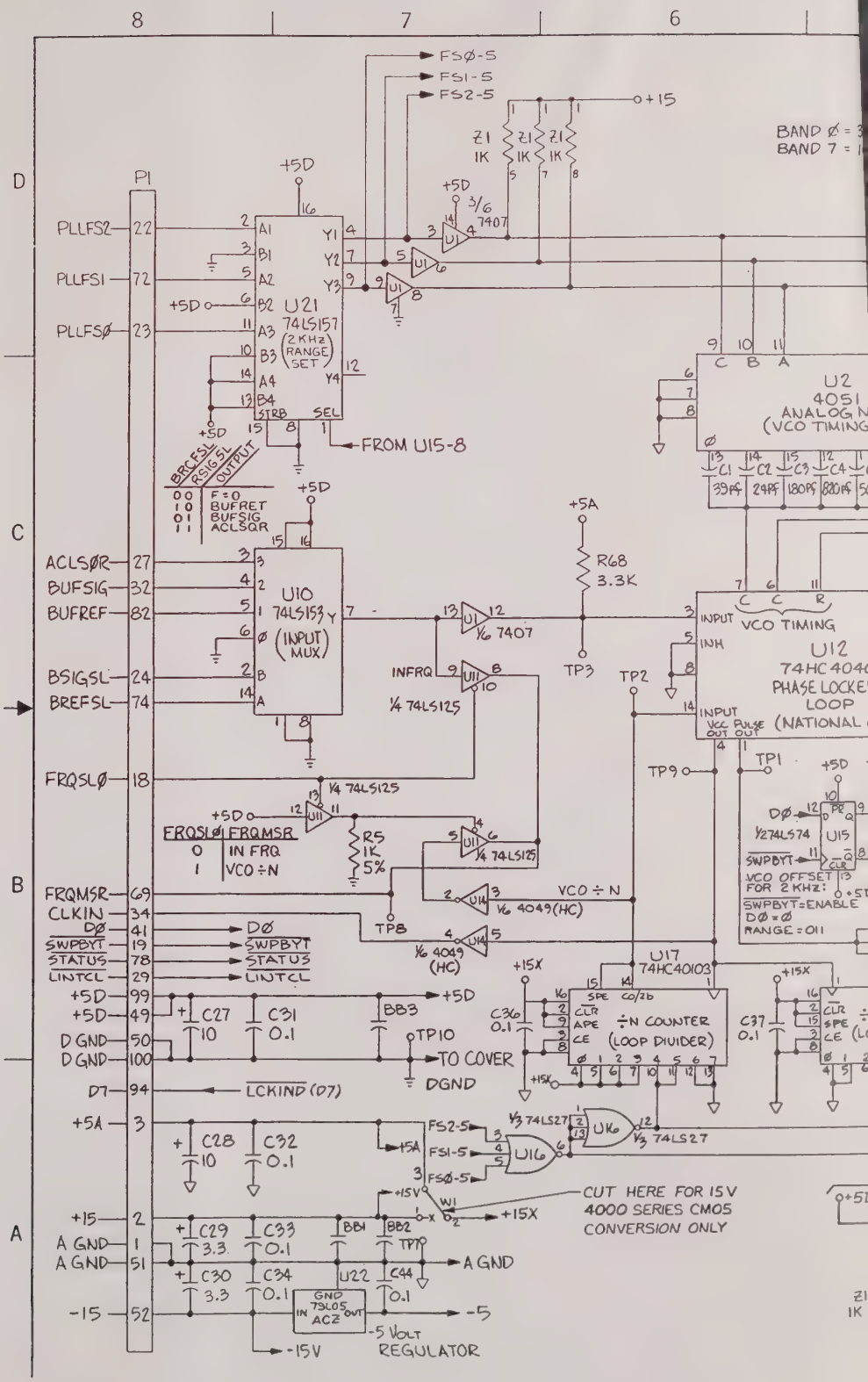
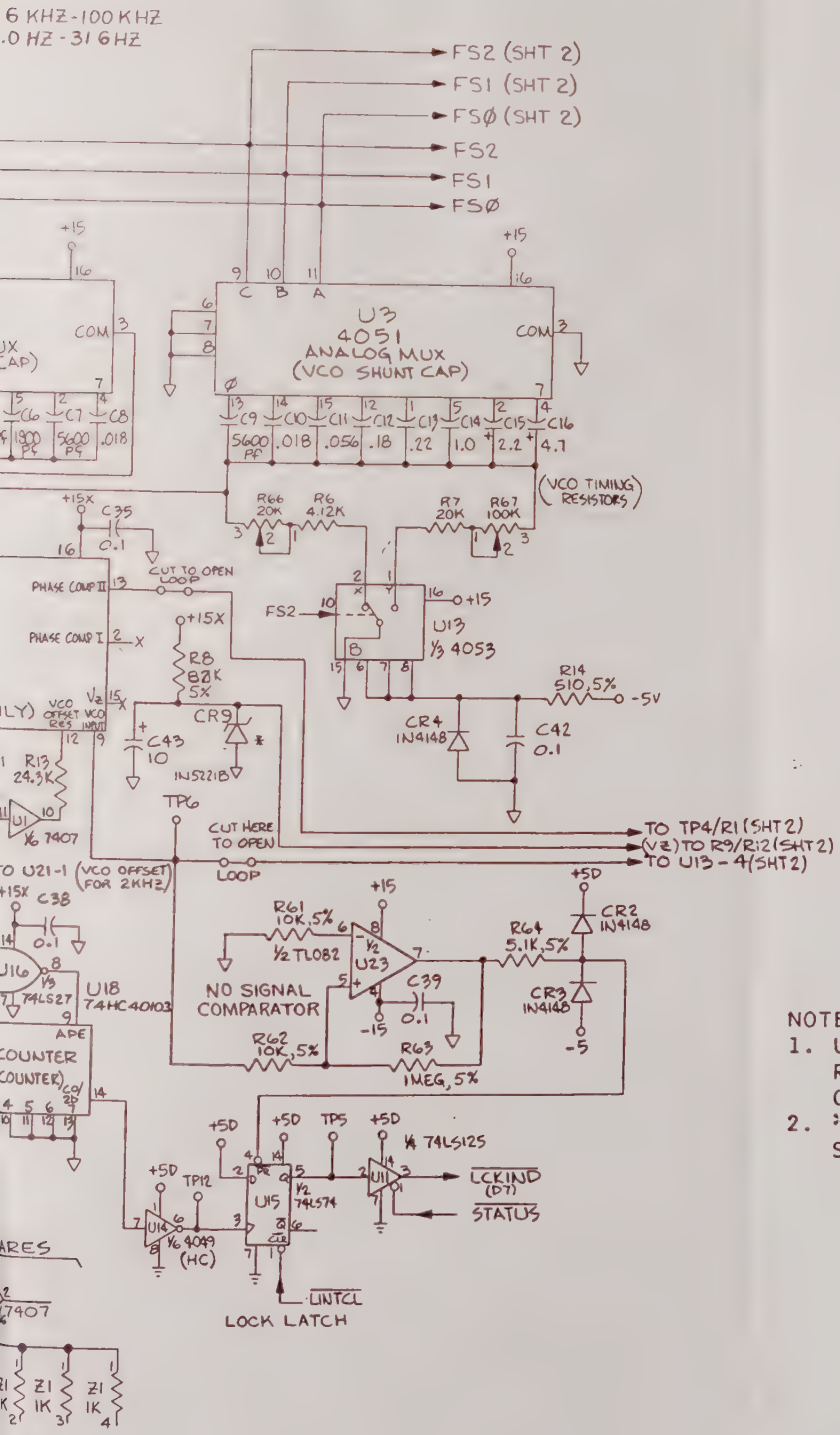


Figure 7-5. Timing and Control CCA A4 (P/N 787173-1), Schematic Diagram 768879-1/D (Sheet 3 of 3)



8
7
6
D
C
B
A
P1
PLLFS2
PLLFS1
PLLFSØ
ACLSØR
BUFSIG
BUFREF
BSIGSL
BREFSL
FRQSLØ
FRQMSR
CLKIN
DØ
SWPBYT
STATUS
LINTCL
+5D
D GND
D7
+5A
+15
A GND
-15
FSØ-5
FS1-5
FS2-5
+15
Z1 1K
3/6 7407
U21 74LS157 (2 KHz RANGE SET)
FROM U15-8
BRCFSL RSIGSL OUTPUT
00 F=0
10 BUFRET
01 BUFSIG
11 ACLSQR
U10 74LS153 (INPUT MUX)
1/6 7407
INFRQ
1/4 74LS125
R68 3.3K
TP3
TP2
TP9
TP1
U2 4051 ANALOG N (VCO TIMING
C1 39pf
C2 24pf
C3 180pf
C4 820pf
U12 74HC404 PHASE LOCKE LOOP (NATIONAL
VCO TIMING
INPUT
INH
VCC PULSE OUT OUT
FRQSLØ FRQMSR
0 IN FRQ
1 VCO ÷N
R5 1K 5%
VCO ÷ N
1/6 4049(HC)
TP8
U15
1/2 74LS74
VCO OFFSET FOR 2 KHz:
SWPBYT=ENABLE
DØ=Ø
RANGE=011
U17 74HC40103
÷N COUNTER (LOOP DIVIDER)
C36 0.1
C37 0.1
C27 10
C31 0.1
BB3
TP10
TO COVER
DGND
LCKIND (D7)
C28 10
C32 0.1
1/3 74LS27
U16
CUT HERE FOR 15V 4000 SERIES CMOS CONVERSION ONLY
W1
+15X
C29 3.3
C33 0.1
BB1
BB2
TP7
C30 3.3
C34 0.1
U22
C44 0.1
GND 79L05 ACZ
-5 VOLT REGULATOR
-5
-15V

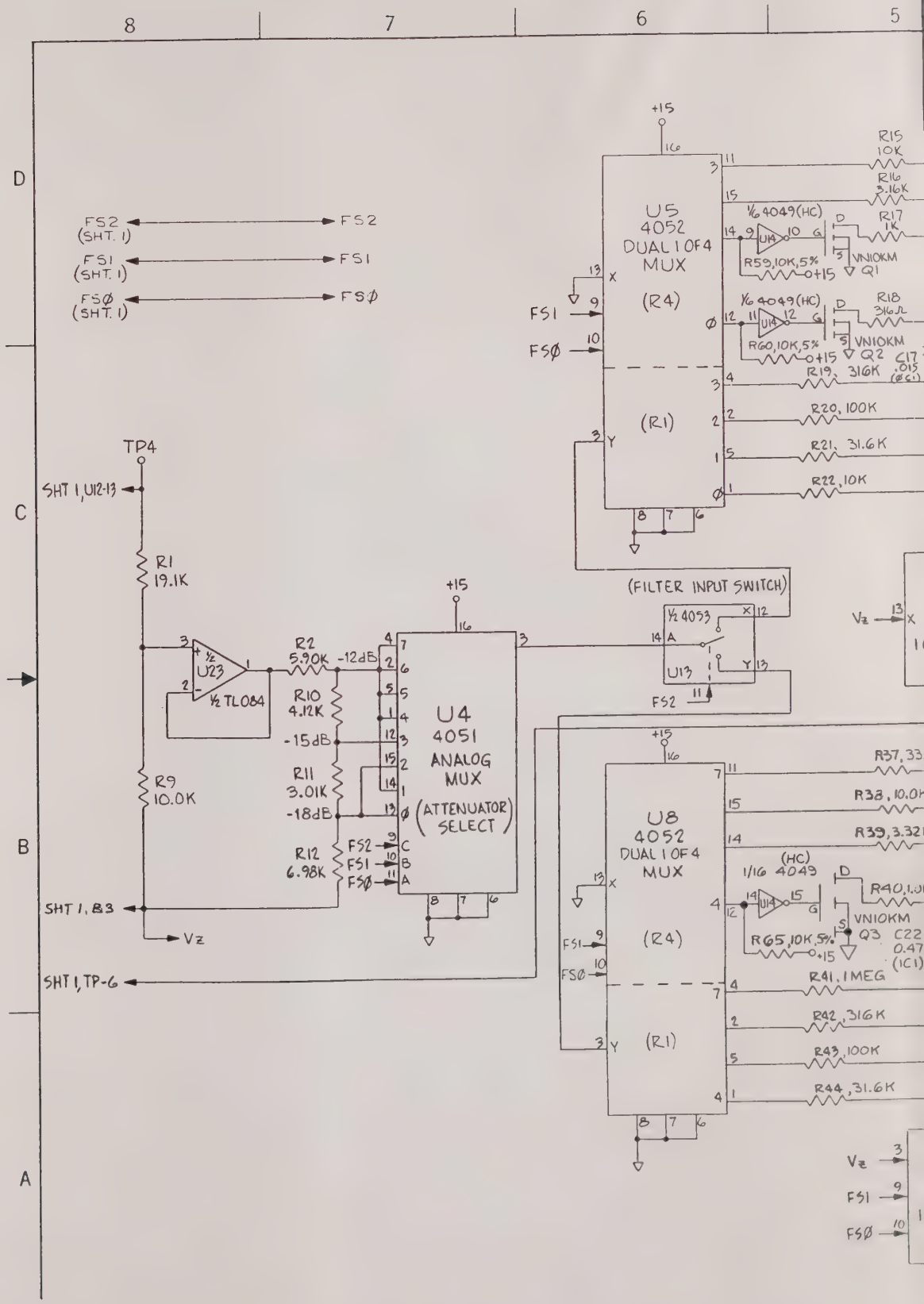
768878-1-E



NOTES:

1. UNLESS OTHER SPECIFIED RESISTANCE IS IN OHMS, 1/10 W, 1% CAPACITANCE IS IN MICROFARADS.
2. *DELETE COMPONENTS FOR 4000 SERIES CMOS OPERATION ONLY.

Figure 7-6. Phase-Locked Loop CCA A5 (P/N 787192-1), Schematic Diagram 786878-1/E (Sheet 1 of 2)


8
7
6
5
D
C
B
A
FS2 (SHT. 1)
FS1 (SHT. 1)
FSØ (SHT. 1)
FS2
FS1
FSØ
TP4
SHT 1, U12-13
R1 19.1K
R9 10.0K
SHT 1, B3
Vz
SHT 1, TP-6
½ U23 ½ TL084
R2 5.90K -12dB
R10 4.12K -15dB
R11 3.01K -18dB
R12 6.98K
U4 4051 ANALOG MUX (ATTENUATOR SELECT)
+15
U5 4052 DUAL 1 OF 4 MUX (R4) (R1)
R15 10K
R16 3.16K
R17 1K
R18 316Ω
R19, 316K
R20, 100K
R21, 31.6K
R22, 10K
1/6 4049(HC)
R59, 10K, 5%
R60, 10K, 5%
VN10KM
Q1
Q2
C17 .015 (ØC1)
(FILTER INPUT SWITCH)
½ 4053
U13
U8 4052 DUAL 1 OF 4 MUX (R4) (R1)
R37, 33
R38, 10.0K
R39, 3.32
1/16 4049 (HC)
R40, 1.0
R65, 10K, 5%
Q3
C22 0.47 (1C1)
R41, 1MEG
R42, 316K
R43, 100K
R44, 31.6K

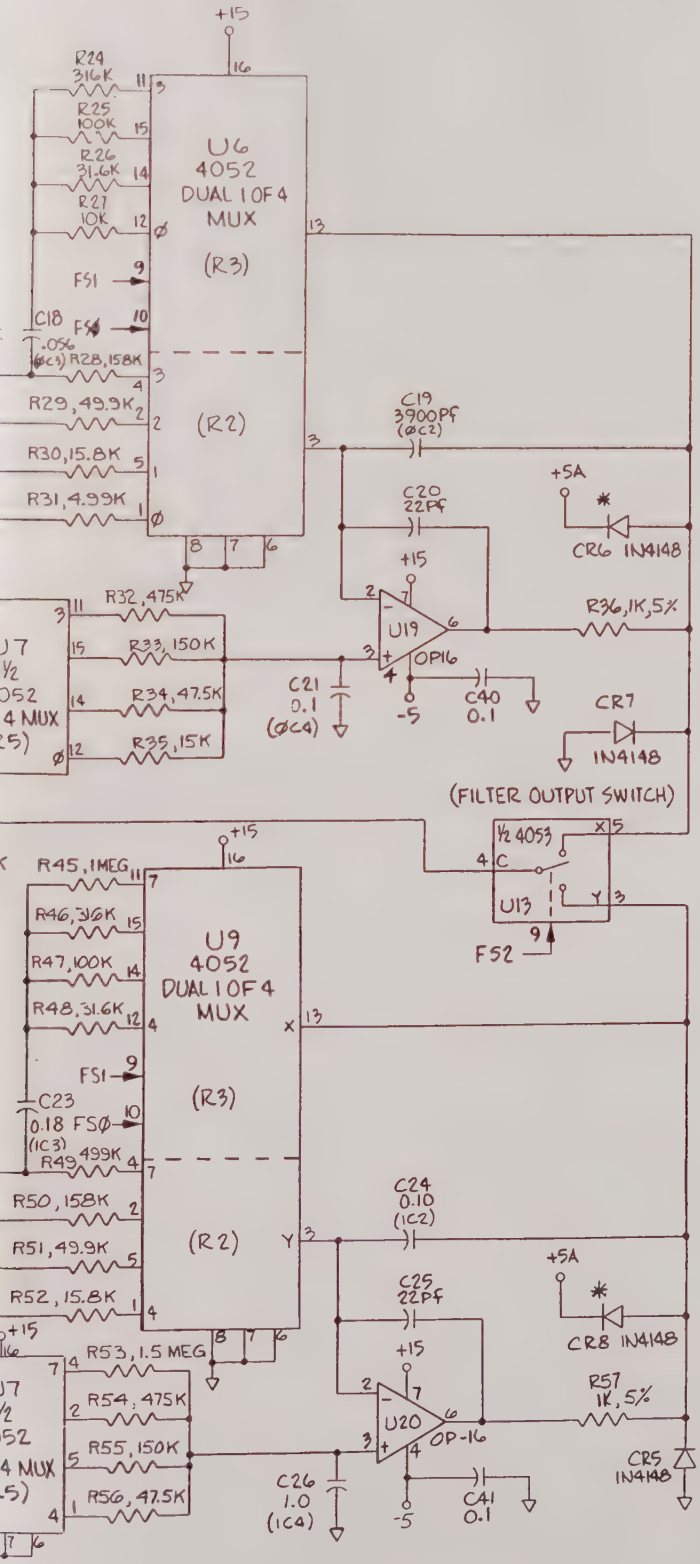
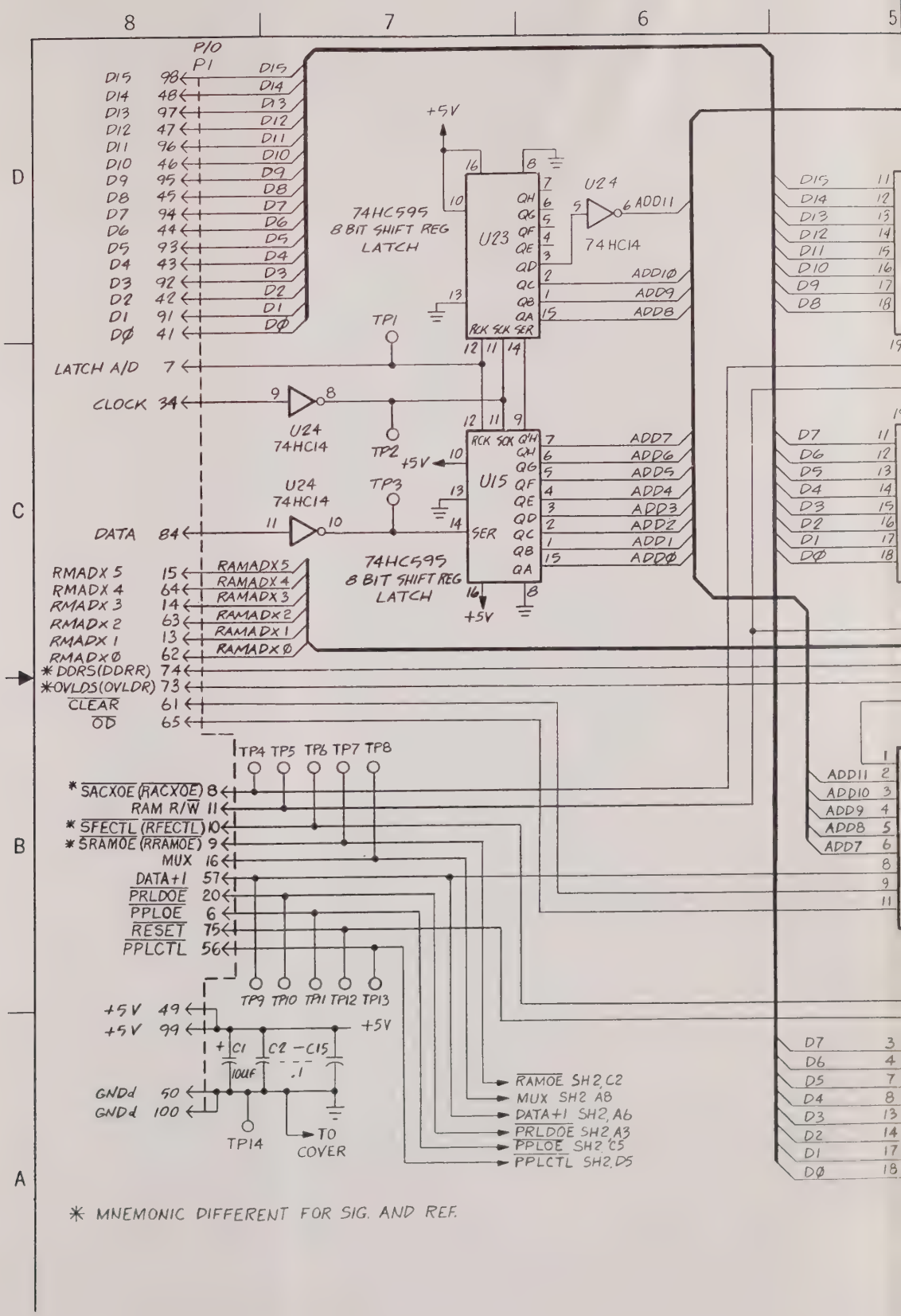


Figure 7-6. Phase-Locked Loop CCA A5 (P/N 787192-1), Schematic Diagram 768878-1/D (Sheet 2 of 2)


8
7
6
5
D
C
B
A
P/O
P1
D15 98
D14 48
D13 97
D12 47
D11 96
D10 46
D9 95
D8 45
D7 94
D6 44
D5 93
D4 43
D3 92
D2 42
D1 91
DØ 41
LATCH A/D 7
CLOCK 34
DATA 84
RMADX 5 15
RMADX 4 64
RMADX 3 14
RMADX 2 63
RMADX 1 13
RMADX Ø 62
*DDRS(DDRR) 74
*OVLDS(OVLDR) 73
CLEAR 61
OD 65
+5V
74HC595
8 BIT SHIFT REG
LATCH
U23
U24
74HC14
U15
TP1
TP2
TP3
TP4 TP5 TP6 TP7 TP8
TP9 TP10 TP11 TP12 TP13
TP14
ADD11
ADD10
ADD9
ADD8
ADD7
ADD6
ADD5
ADD4
ADD3
ADD2
ADD1
ADDØ
RAMADX5
RAMADX4
RAMADX3
RAMADX2
RAMADX1
RAMADXØ
*SACXOE (RACXOE) 8
RAM R/W 11
*SFECTL (RFECTL) 10
*SRAMOE (RRAMOE) 9
MUX 16
DATA+1 57
PRLDOE 20
PPLOE 6
RESET 75
PPLCTL 56
+5V 49
+5V 99
GNDd 50
GNDd 100
C1 10UF
C2 – C15 .1
TO COVER
RAMOE SH2, C2
MUX SH2 A8
DATA+1 SH2, A6
PRLDOE SH2, A3
PPLOE SH2, C5
PPLCTL SH2, D5
* MNEMONIC DIFFERENT FOR SIG. AND REF.

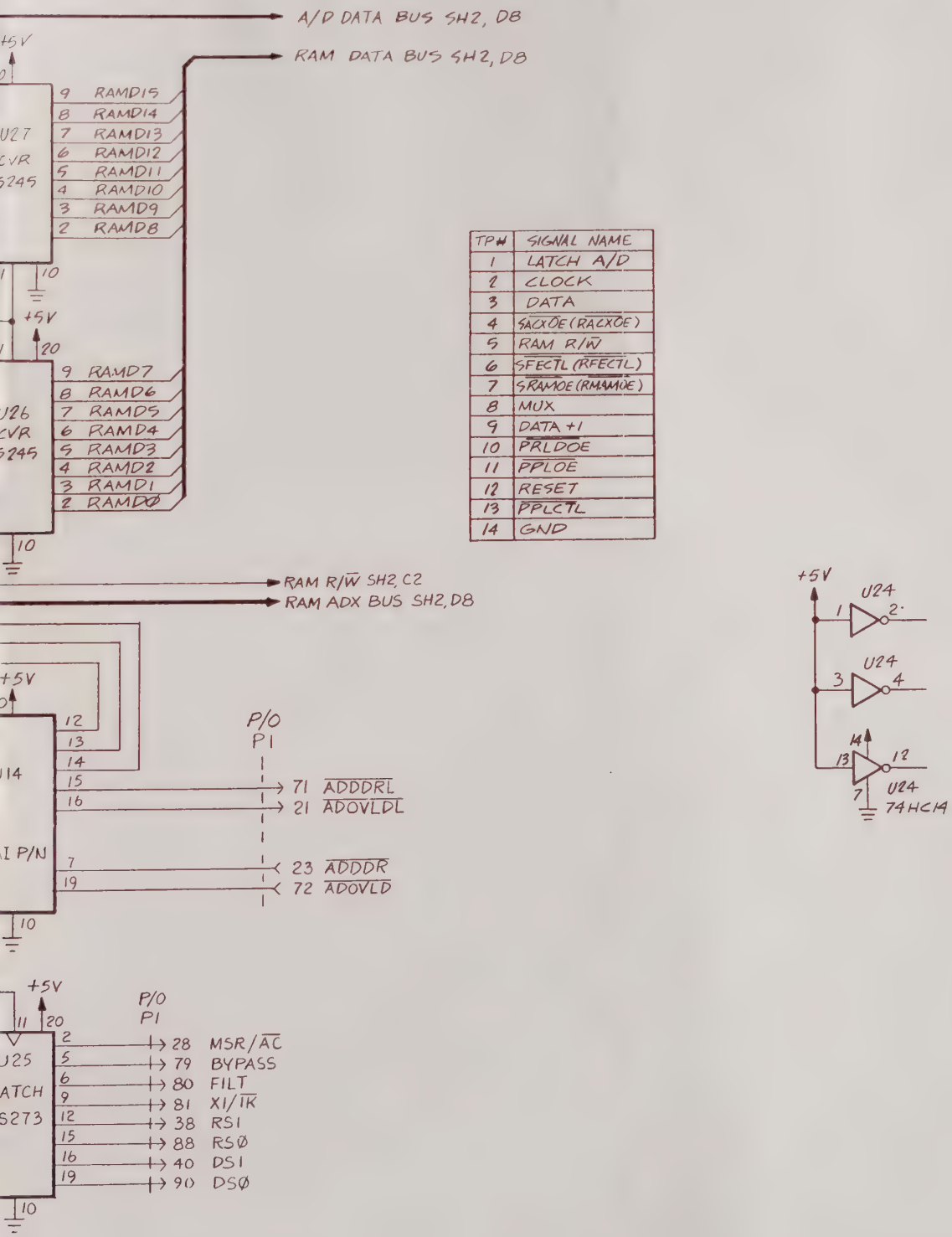
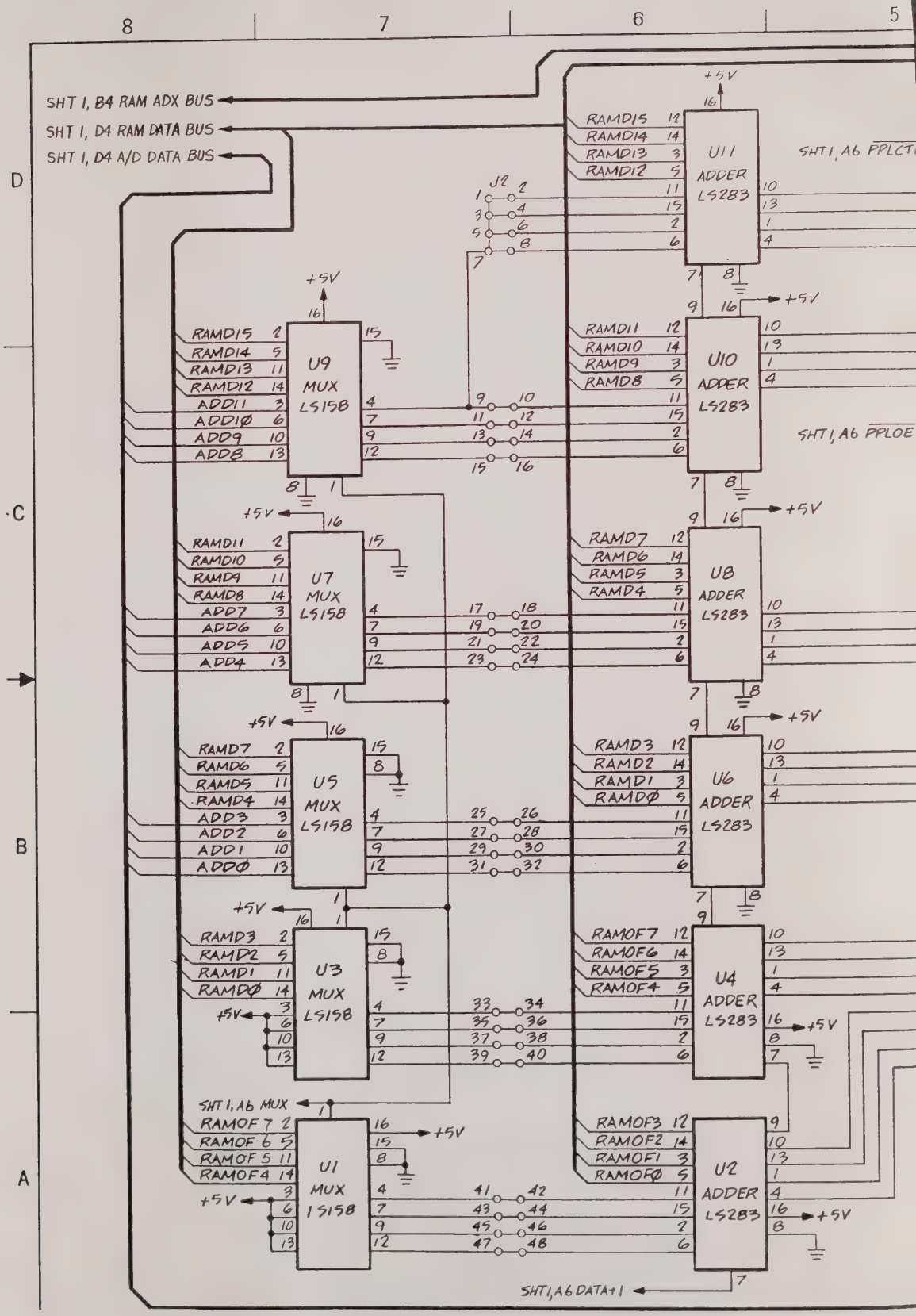


Figure 7-7. Accumulator CCA A6, A7 (P/N 787193-1), Schematic Diagram 768865-1/A (Sheet 1 of 2)


8
7
6
5
D
C
B
A
SHT 1, B4 RAM ADX BUS
SHT 1, D4 RAM DATA BUS
SHT 1, D4 A/D DATA BUS
+5V
U9 MUX LS158
U7 MUX LS158
U5 MUX LS158
U3 MUX LS158
U1 MUX LS158
U11 ADDER LS283
U10 ADDER LS283
U8 ADDER LS283
U6 ADDER LS283
U4 ADDER LS283
U2 ADDER LS283
J2
RAMDI5
RAMDI4
RAMDI3
RAMDI2
RAMDI1
RAMDIØ
RAMD9
RAMD8
RAMD7
RAMD6
RAMD5
RAMD4
RAMD3
RAMD2
RAMD1
RAMDØ
ADDI1
ADDIØ
ADD9
ADD8
ADD7
ADD6
ADD5
ADD4
ADD3
ADD2
ADD1
ADDØ
RAMOF7
RAMOF6
RAMOF5
RAMOF4
RAMOF3
RAMOF2
RAMOF1
RAMOFØ
SHT 1, A6 MUX
SHT 1, A6 PPLCT
SHT 1, A6 PPLOE
SHT 1, A6 DATA+1

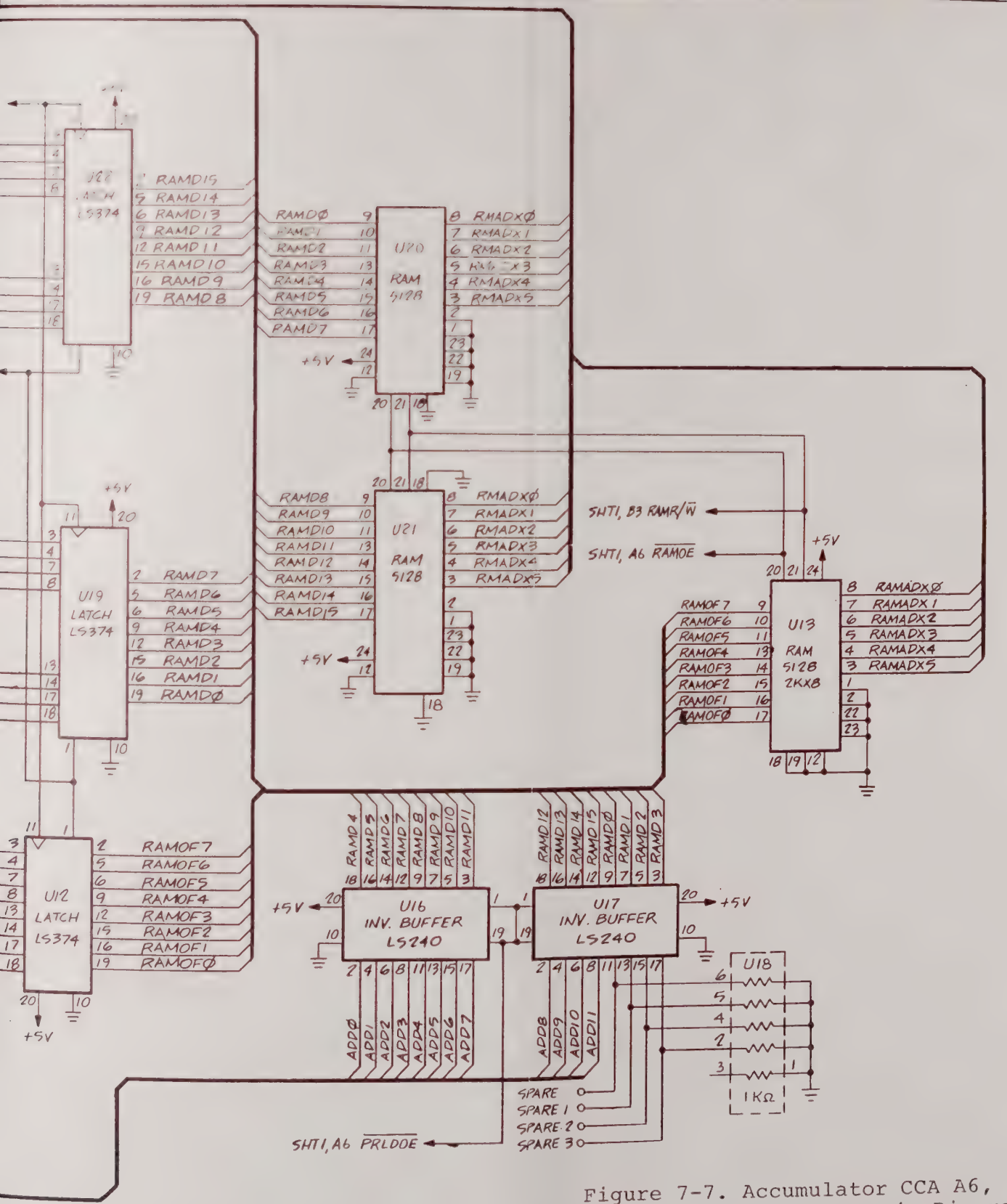
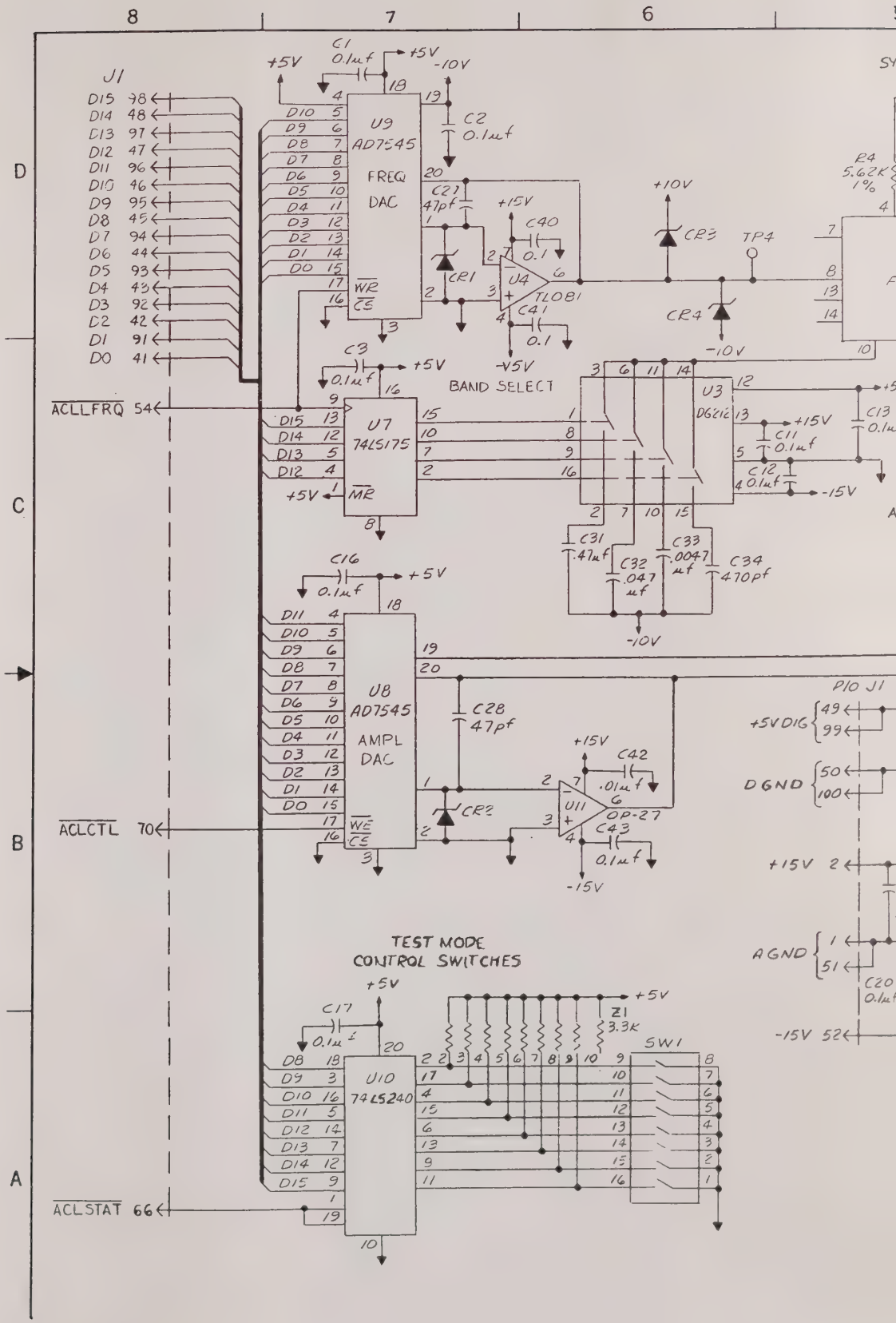


Figure 7-7. Accumulator CCA A6, A7 (P/N 787193-1), Schematic Diagram 768865-1/A (Sheet 2 of 2)


8
7
6
D
C
B
A
J1
D15 98
D14 48
D13 97
D12 47
D11 96
D10 46
D9 95
D8 45
D7 94
D6 44
D5 93
D4 43
D3 92
D2 42
D1 91
D0 41
ACLLFRQ 54
ACLCTL 70
ACLSTAT 66
C1 0.1µf
+5V
-10V
U9 AD7545 FREQ DAC
C2 0.1µf
C27 47pf
+15V
C40 0.1
CR1
U4 TL081
C41 0.1
-15V
+10V
CR3
TP4
CR4
-10V
R4 5.62K 1%
C3 0.1µf
BAND SELECT
U7 74LS175
MR
U3 DG212
C11 0.1µf
C12 0.1µf
C13 0.1µ
C31 .47µf
C32 .047 µf
C33 .0047 µf
C34 470pf
C16 0.1µf
U8 AD7545 AMPL DAC
C28 47pf
CR2
U11 OP-27
C42 .01µf
C43 0.1µf
P/O J1
+5VDIG 49 99
DGND 50 100
+15V 2
AGND 1 51
-15V 52
C20 0.1µ
TEST MODE CONTROL SWITCHES
C17 0.1µf
U10 74LS240
Z1 3.3K
SW1

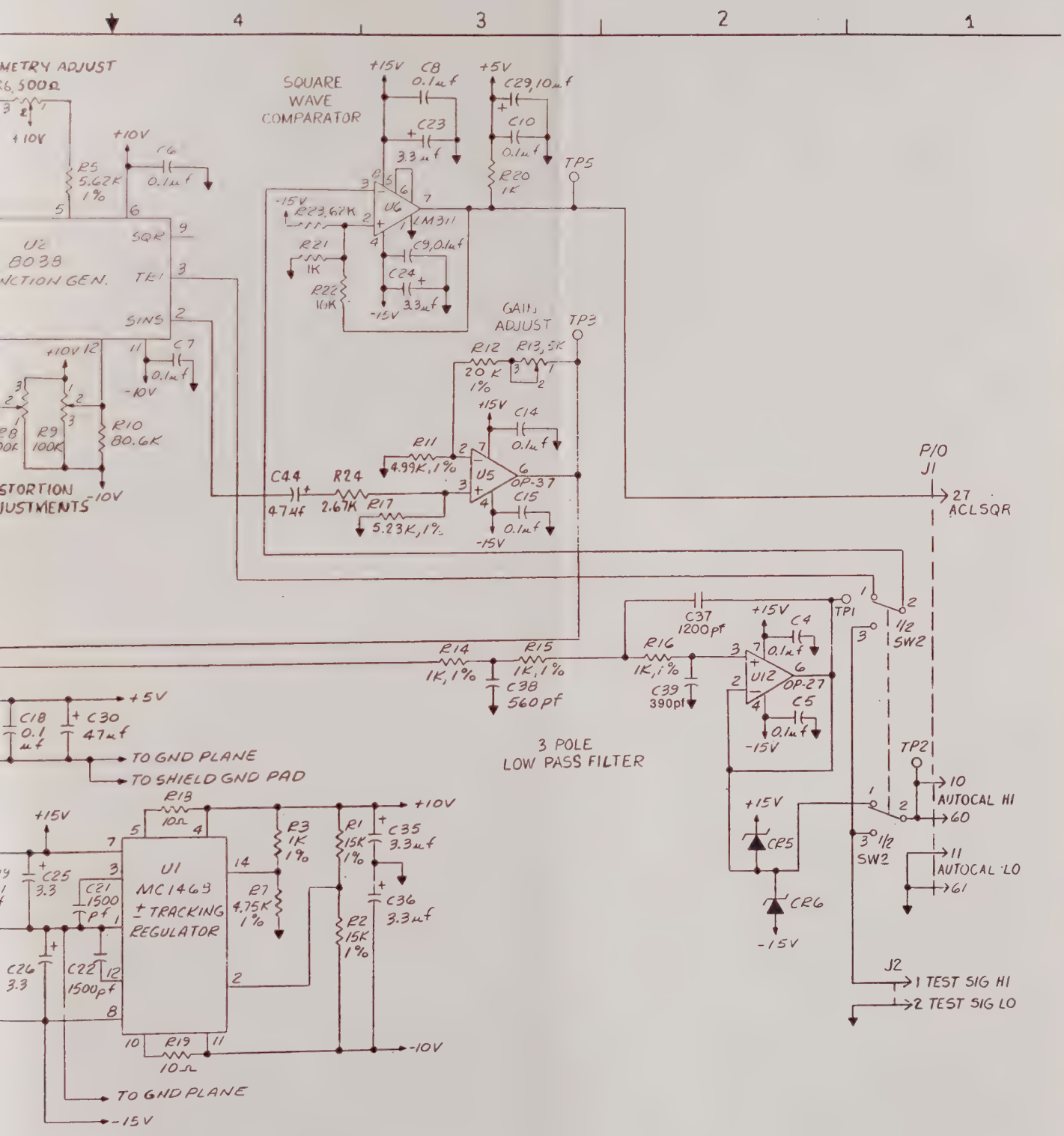
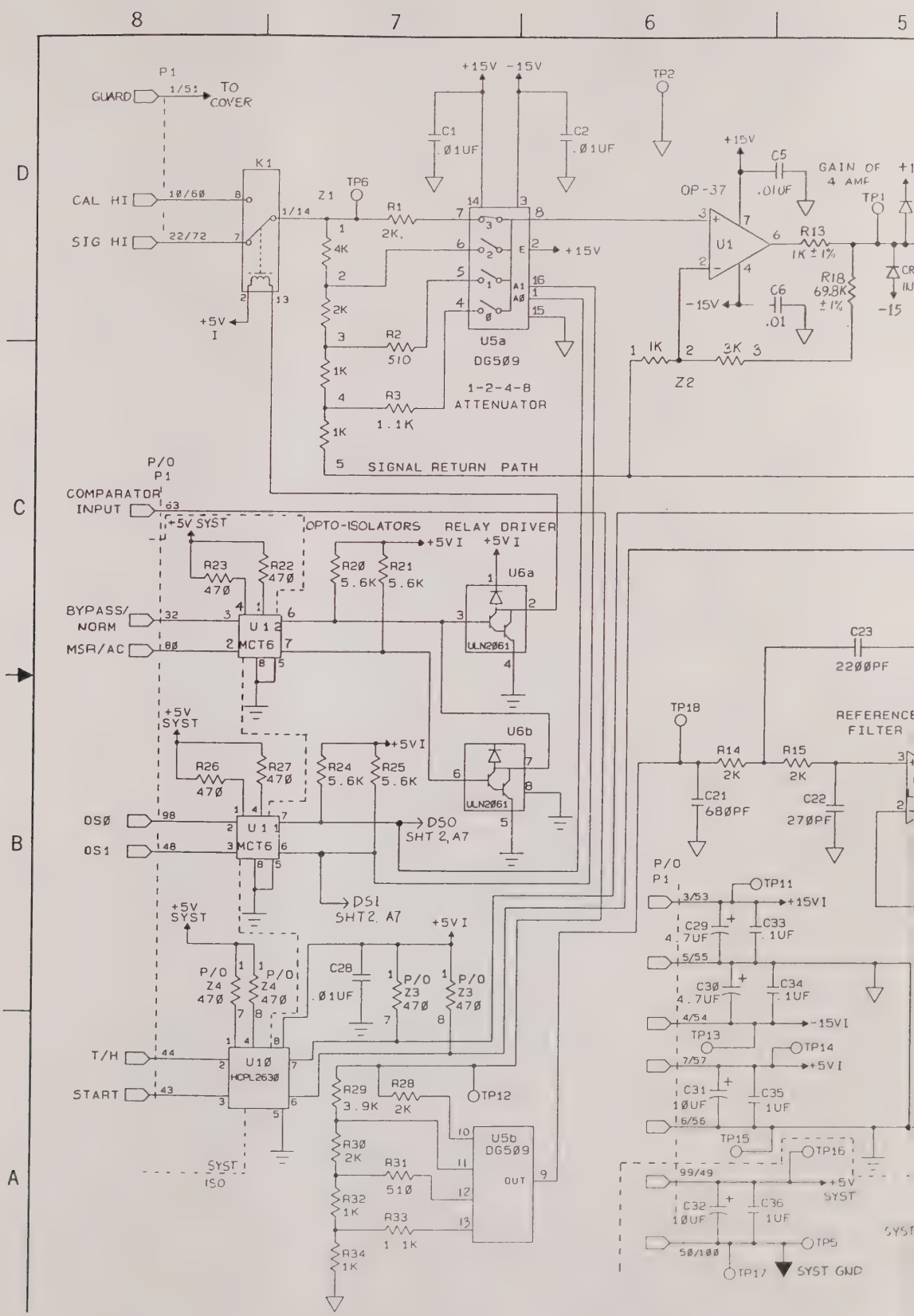


Figure 7-8. Auto Calibration CCA A8
(P/N 787274-2),
Schematic Diagram 768877-2/B


8
7
6
5
D
C
B
A
P1
GUARD
1/51
TO COVER
CAL HI
10/60
SIG HI
22/72
K1
1/14
+5V I
Z1
TP6
R1 2K
4K
2K
1K
1K
R2 510
R3 1.1K
5 SIGNAL RETURN PATH
+15V -15V
C1 .01UF
C2 .01UF
U5a DG509
1-2-4-8 ATTENUATOR
+15V
TP2
OP-37
U1
C5 .01UF
GAIN OF 4 AMP
TP1
R13 1K ±1%
R18 69.8K ±1%
C6 .01
-15V
1K
3K
Z2
P/O P1
COMPARATOR INPUT
63
+5V SYST
OPTO-ISOLATORS
RELAY DRIVER
+5VI
R23 470
R22 470
R20 5.6K
R21 5.6K
U6a
ULN2061
BYPASS/ NORM
32
MSR/AC
80
U12 MCT6
R26 470
R27 470
R24 5.6K
R25 5.6K
U6b
OS0
98
OS1
48
U11 MCT6
DS0 SHT 2, A7
DS1 SHT2, A7
P/O Z4 470
P/O Z4 470
C28 .01UF
P/O Z3 470
P/O Z3 470
T/H
44
START
43
U10 HCPL2630
SYST ISO
R29 3.9K
R28 2K
TP12
R30 2K
R31 510
R32 1K
R33 1 1K
R34 1K
U5b DG509
OUT
C23 2200PF
TP18
REFERENCE FILTER
R14 2K
R15 2K
C21 680PF
C22 270PF
TP11
3/53
+15VI
C29 4.7UF
C33 .1UF
5/55
C30 4.7UF
C34 .1UF
4/54
-15VI
TP13
TP14
7/57
+5VI
C31 10UF
C35 1UF
6/56
TP15
TP16
99/49
+5V SYST
C32 10UF
C36 1UF
50/100
TP5
TP17
SYST GND

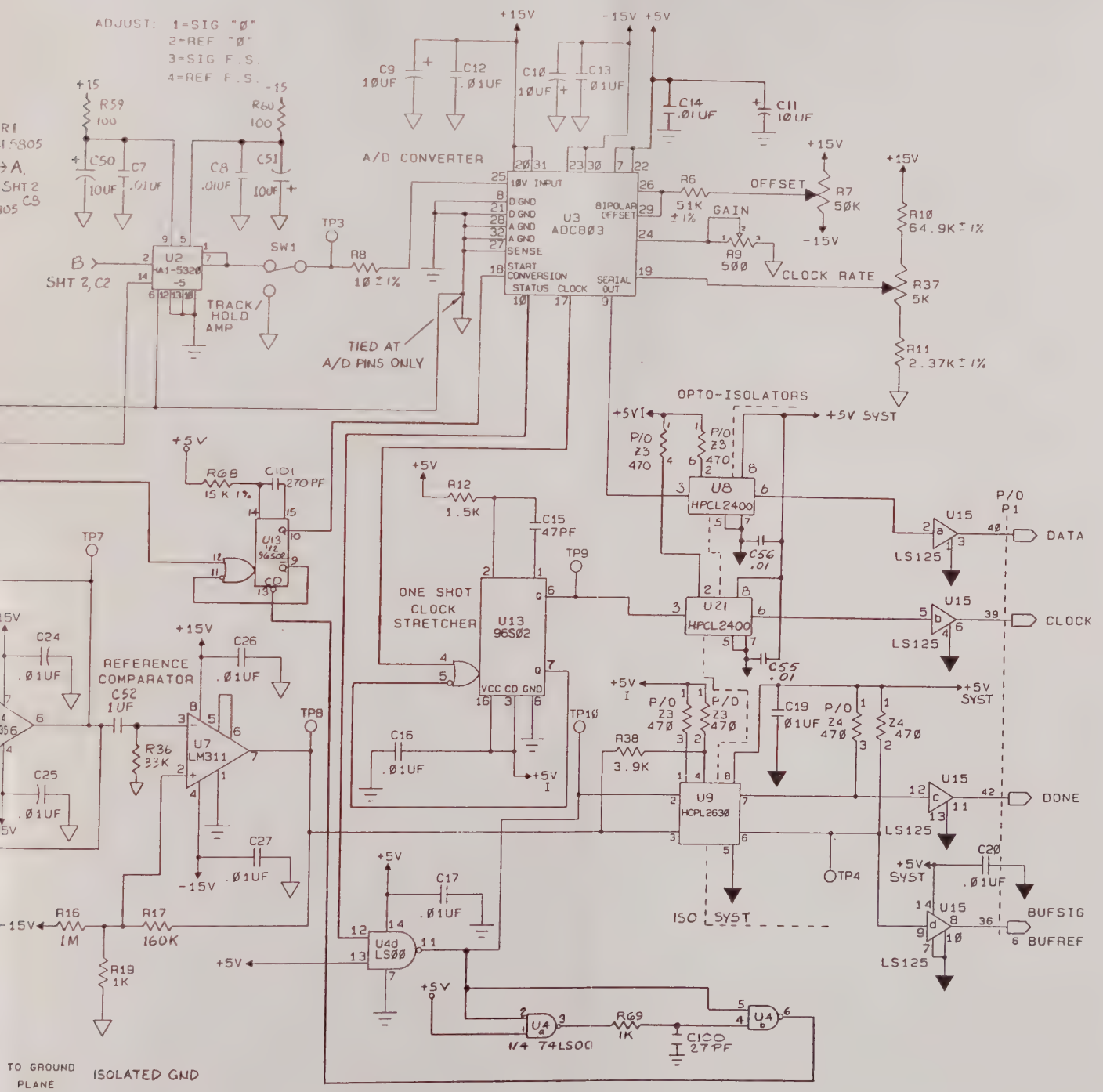
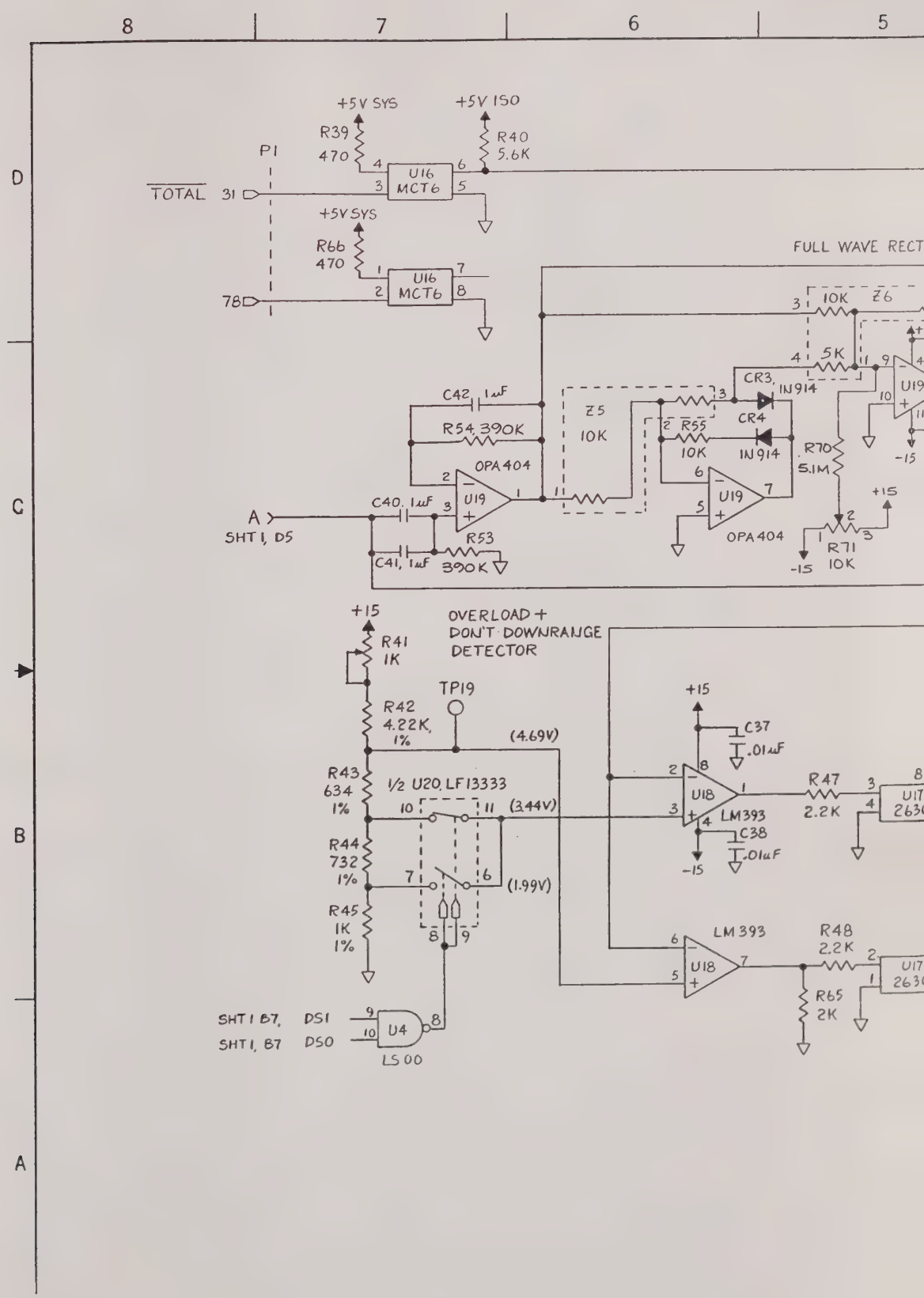
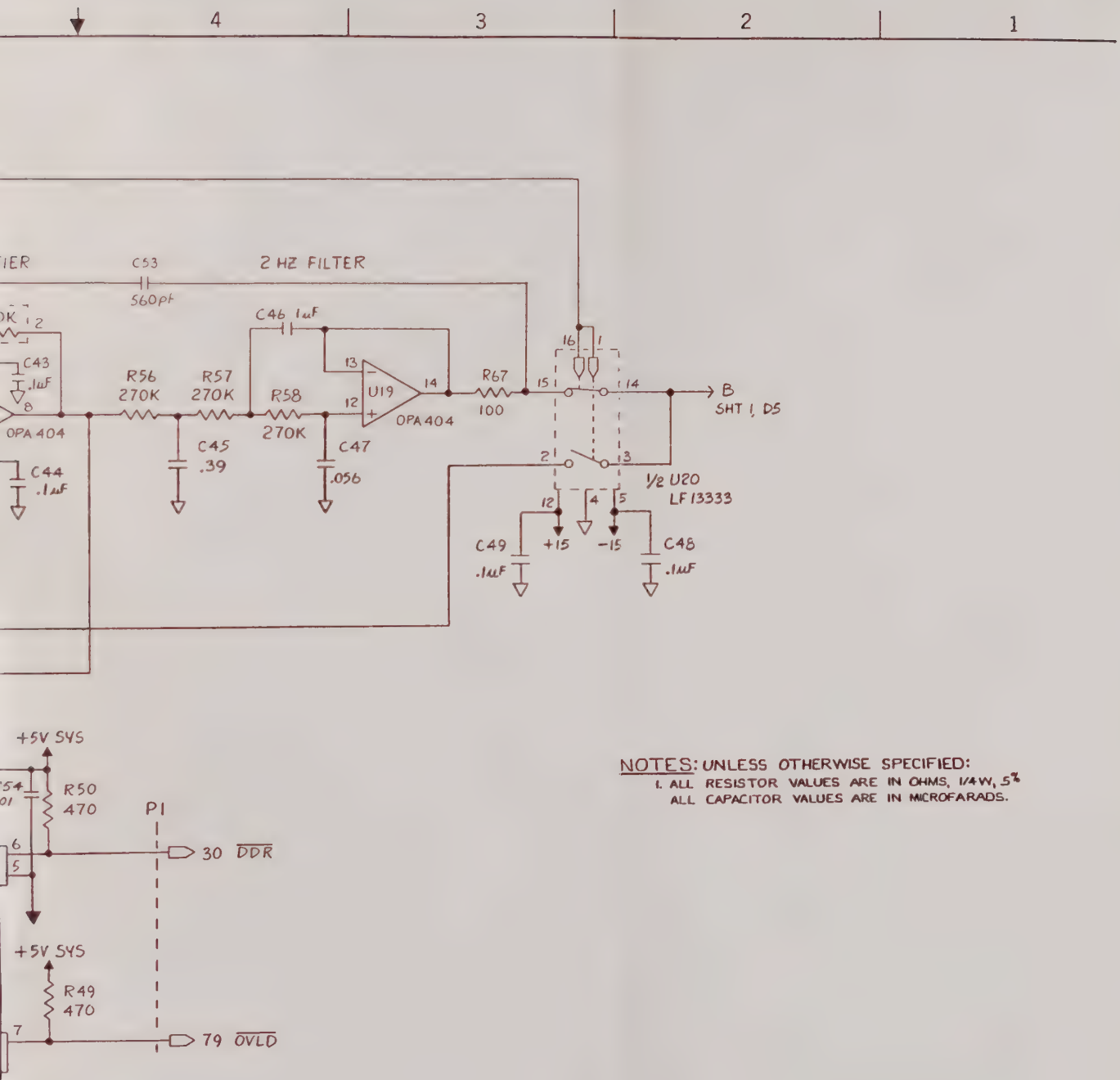


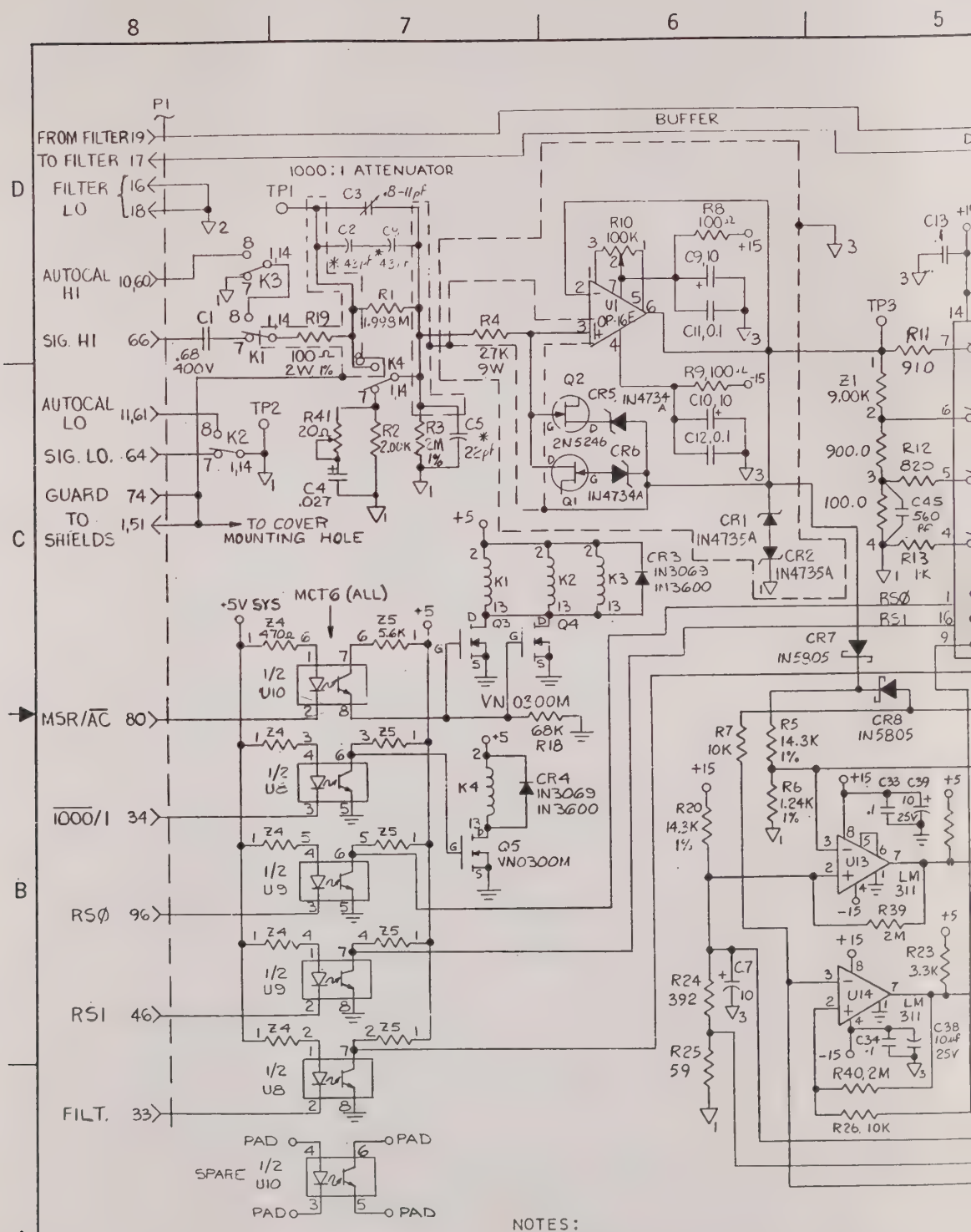
Figure 7-9. A/D Converter CCA A9, A12 (P/N 787664), Schematic Diagram 768987/E (Sheet 1 of 2)


8
7
6
5
D
C
B
A
+5V SYS
+5V ISO
R39
470
R40
5.6K
P1
TOTAL
31
U16
MCT6
+5V SYS
R66
470
78
U16
MCT6
FULL WAVE RECT
10K
Z6
5K
CR3,
IN914
C42, 1uF
Z5
10K
R54, 390K
CR4
R55
10K
IN914
OPA404
R70
5.1M
U19
A
SHT 1, D5
C40, 1uF
R53
C41, 1uF
390K
OPA404
+15
-15
R71
10K
+15
OVERLOAD +
DON'T DOWNRANGE
DETECTOR
R41
1K
TP19
R42
4.22K,
1%
(4.69V)
R43
634
1%
1/2 U20, LF13333
(3.44V)
R44
732
1%
(1.99V)
R45
1K
1%
U18
LM393
C37
.01uF
C38
.01uF
R47
2.2K
R48
2.2K
R65
2K
SHT 1 B7, DS1
SHT 1, B7 DS0
U4
LS00



NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS.

Figure 7-9. A/D Converter CCA A9, A12 (P/N 787664), Schematic Diagram 768987/E (Sheet 2 of 2)



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, 1/4 W, ±5% AND CAPACITANCE VALUES ARE IN MICROFARADS.

*CURVED END OF C2, C5, & C8 IS CONNECTED TO OUTSIDE FOIL

NOTE: C46 IS A "SELECT-AT-TEST" COMPONENT.

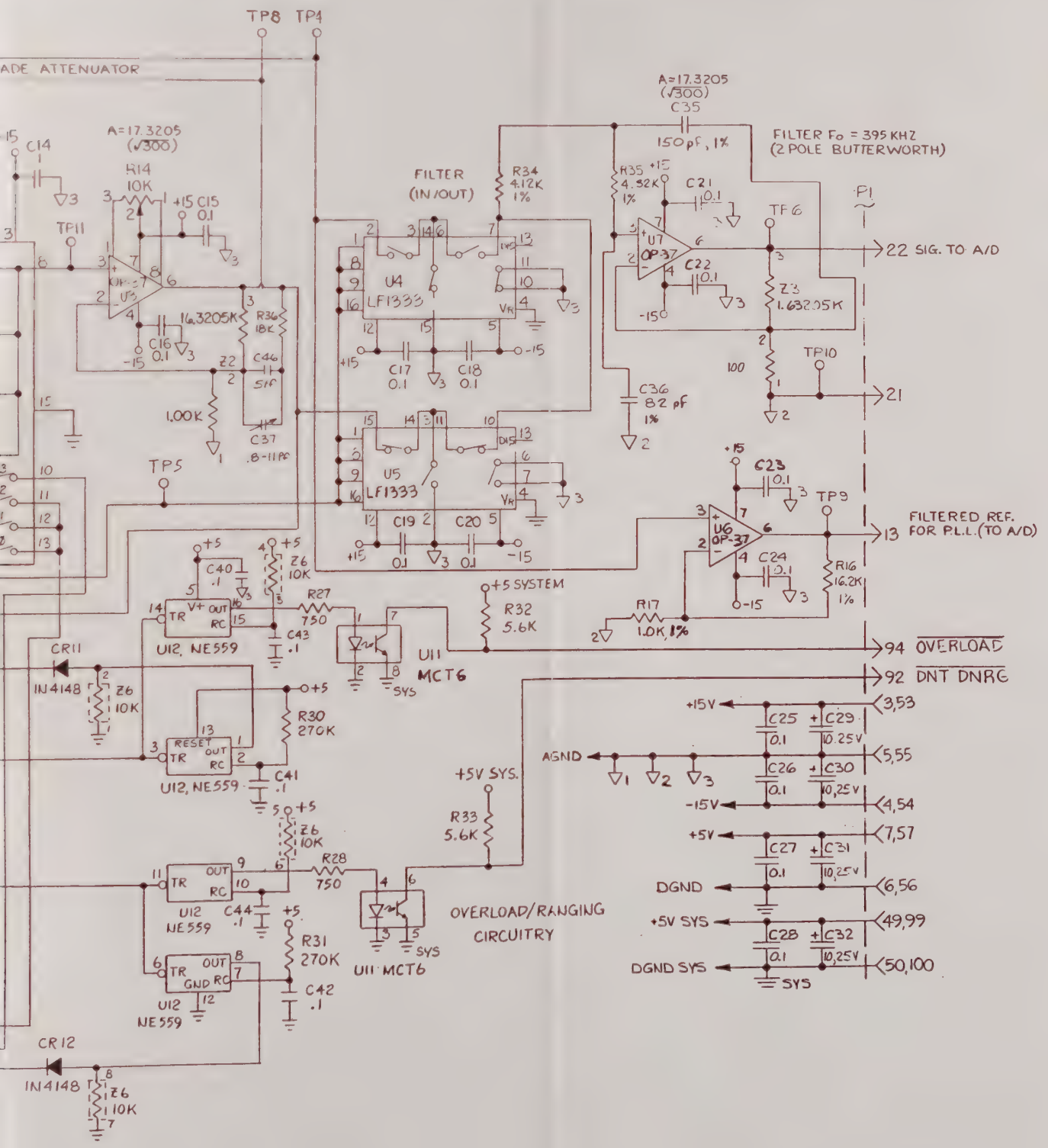
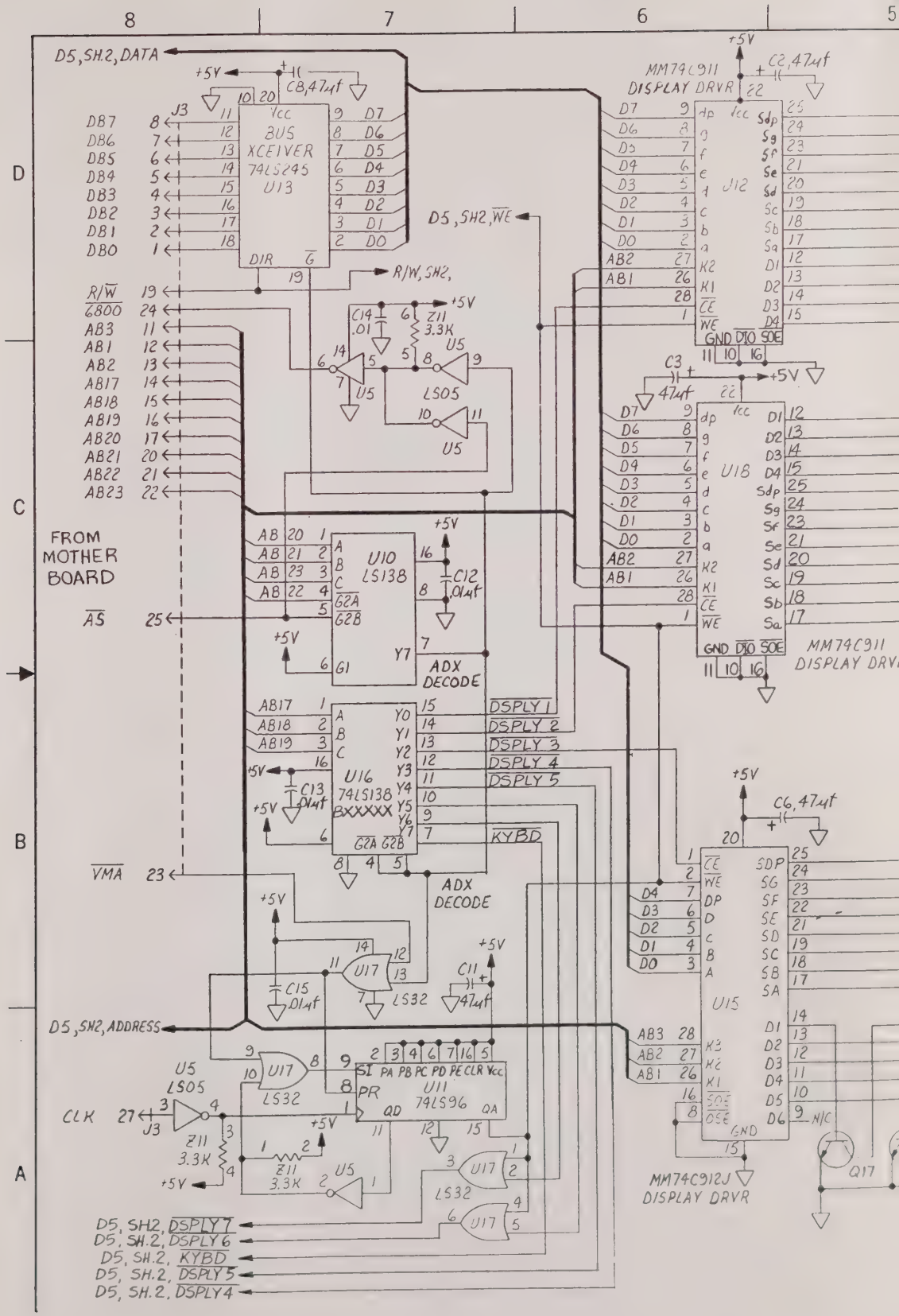


Figure 7-10. Front End CCA
A11, A14 (P/N 787505-1),
Schematic Diagram 768930-1/E


8
7
6
5
D
C
B
A
D5,SH2,DATA
+5V
C8,47uf
J3
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
BUS XCEIVER 74LS245 U13
Vcc
DIR
G
D7
D6
D5
D4
D3
D2
D1
D0
R/W, SH2,
R/W
6800
AB3
AB1
AB2
AB17
AB18
AB19
AB20
AB21
AB22
AB23
C14 .01
Z11 3.3K
U5
LS05
FROM MOTHER BOARD
AS
U10 LS138
C12 .01uf
ADX DECODE
U16 74LS138 BXXXXX
C13 .01uf
DSPLY 1
DSPLY 2
DSPLY 3
DSPLY 4
DSPLY 5
KYBD
VMA
U17 LS32
C15 .01uf
C11 47uf
D5,SH2,ADDRESS
U11 74LS96
CLK
D5,SH2,DSPLY7
D5,SH2,DSPLY6
D5,SH2,KYBD
D5,SH2,DSPLY5
D5,SH2,DSPLY4
D5,SH2,WE
MM74C911 DISPLAY DRVR
C2,47uf
U12
C3 47uf
U18
C6,47uf
U15
MM74C912J DISPLAY DRVR
Q17

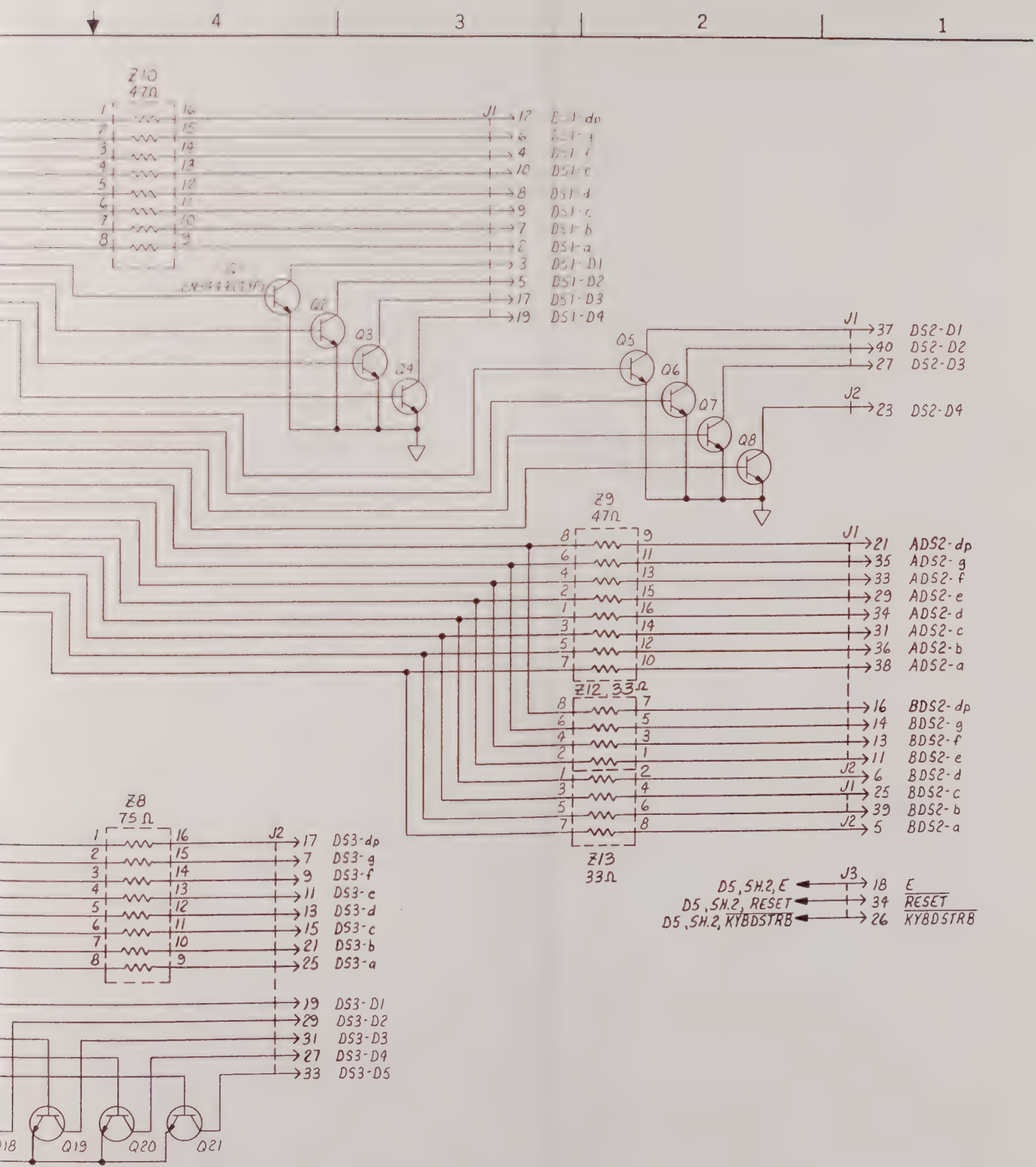
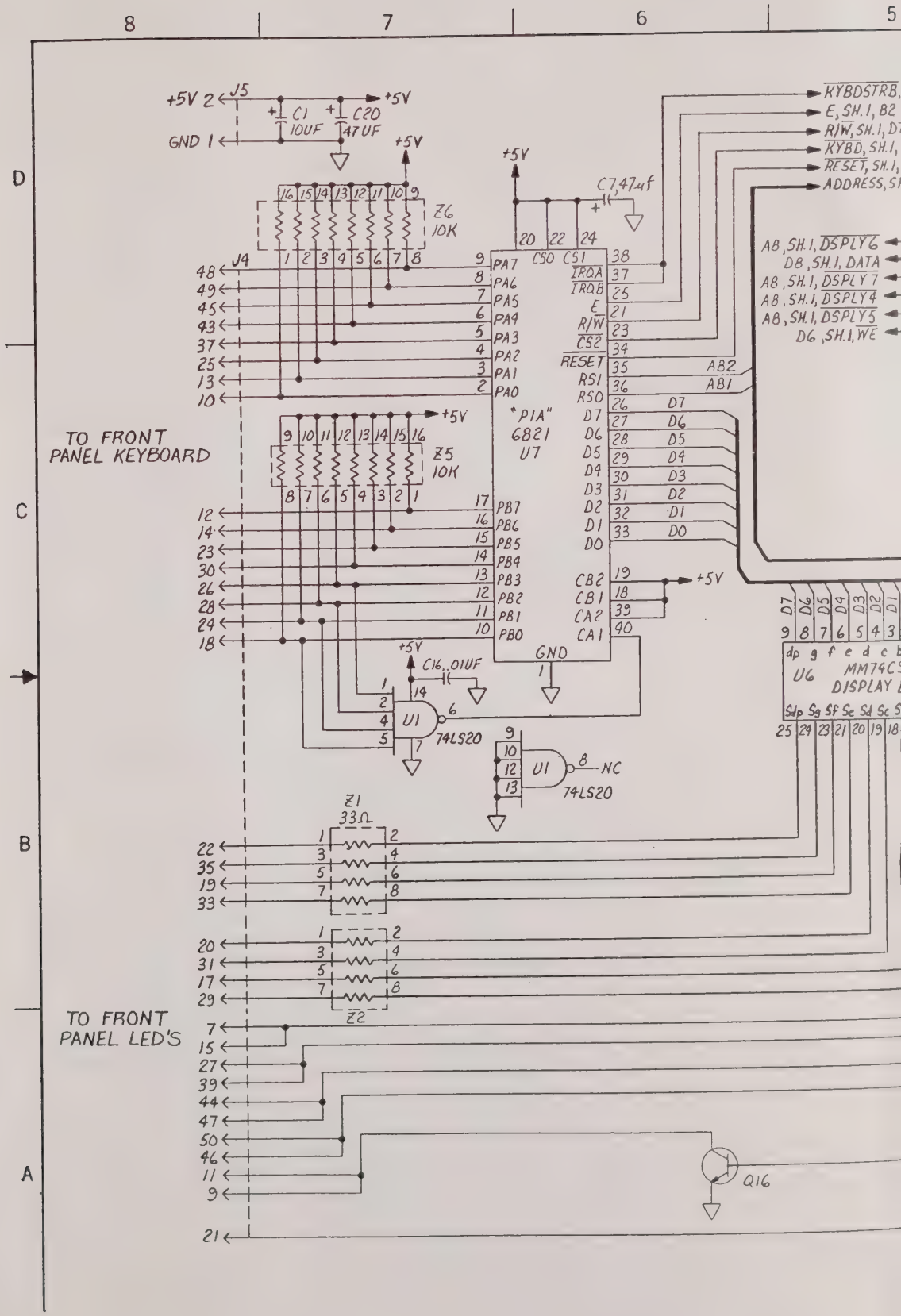


Figure 7-11. Display Driver CCA A15A2 (P/N 787179), Schematic Diagram 768862/D (Sheet 1 of 2)


8
7
6
5
D
C
B
A
+5V 2
J5
GND 1
C1
10UF
C20
47UF
+5V
Z6
10K
J4
TO FRONT
PANEL KEYBOARD
"PIA"
6821
U7
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
CS0
CS1
IRQA
IRQB
E
R/W
CS2
RESET
RS1
RS0
D7
D6
D5
D4
D3
D2
D1
D0
CB2
CB1
CA2
CA1
GND
Z5
10K
C7,47uf
C16,.01UF
U1
74LS20
NC
Z1
33Ω
Z2
TO FRONT
PANEL LED'S
Q16
KYBDSTRB
E, SH.1, B2
R/W, SH.1, D7
KYBD, SH.1,
RESET, SH.1,
ADDRESS, SH
AB, SH.1, DSPLY6
DB, SH.1, DATA
AB, SH.1, DSPLY7
AB, SH.1, DSPLY4
AB, SH.1, DSPLY5
DG, SH.1, WE
AB2
AB1
U6
MM74C
DISPLAY

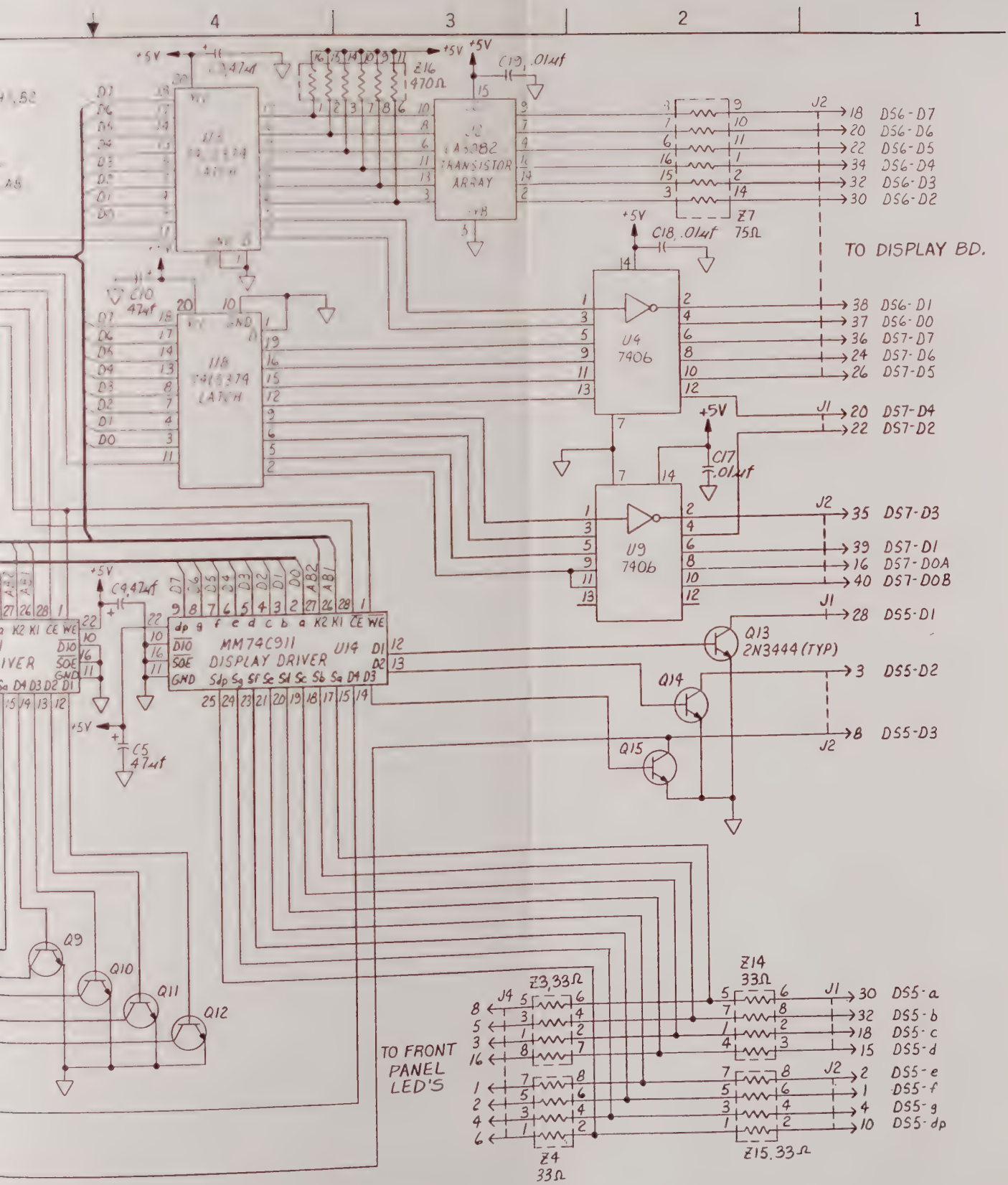
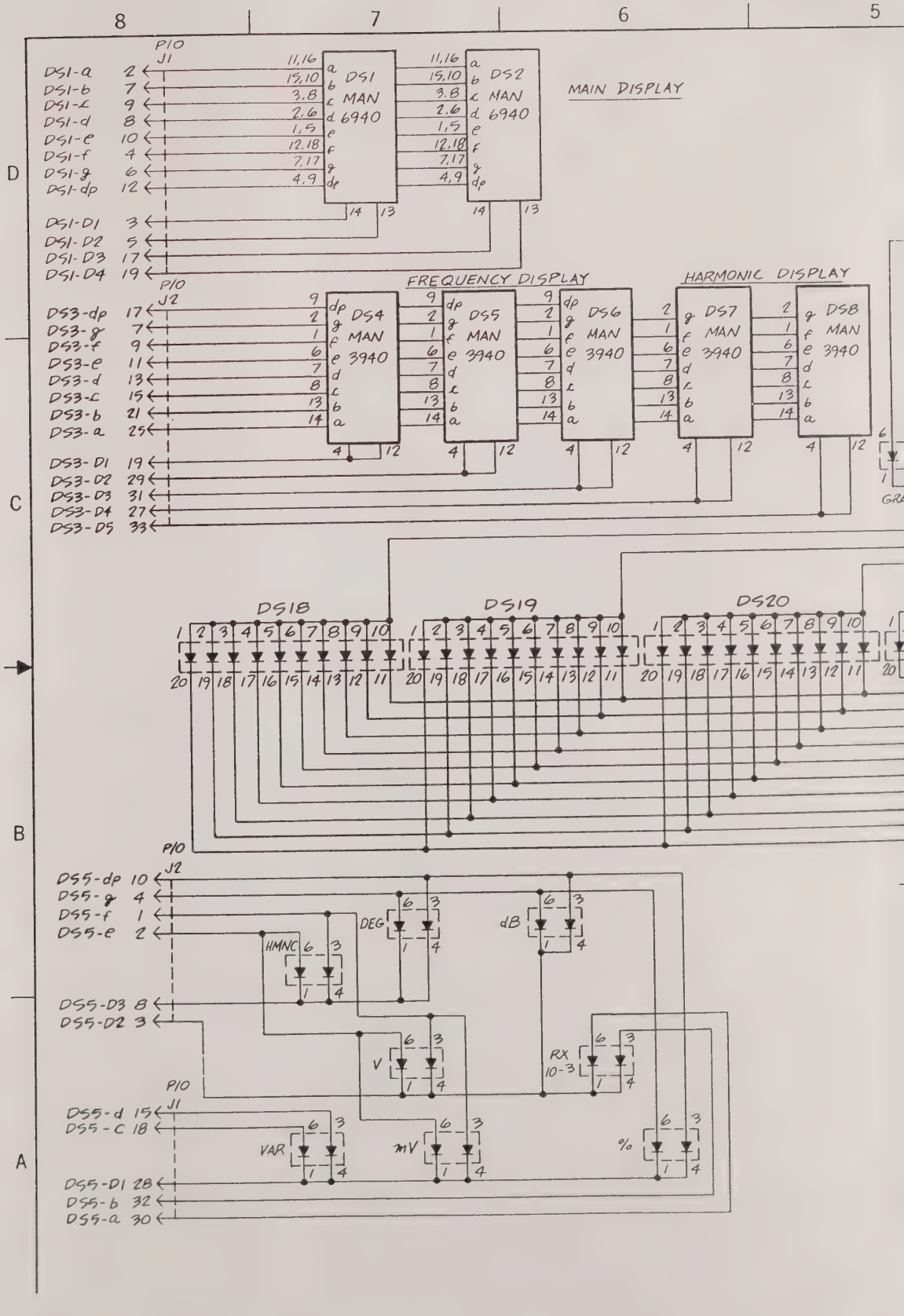


Figure 7-11. Display Driver CCA A15A2 (P/N 787179), Schematic Diagram 768862/D (Sheet 2 of 2)


8
7
6
5
D
C
B
A
MAIN DISPLAY
FREQUENCY DISPLAY
HARMONIC DISPLAY
P10
J1
J2
DS1
DS2
DS4
DS5
DS6
DS7
DS8
MAN 6940
MAN 3940
DS1-a
DS1-b
DS1-c
DS1-d
DS1-e
DS1-f
DS1-g
DS1-dp
DS1-D1
DS1-D2
DS1-D3
DS1-D4
DS3-dp
DS3-g
DS3-f
DS3-e
DS3-d
DS3-c
DS3-b
DS3-a
DS3-D1
DS3-D2
DS3-D3
DS3-D4
DS3-D5
DS18
DS19
DS20
DS5-dp
DS5-g
DS5-f
DS5-e
DS5-D3
DS5-D2
DS5-d
DS5-c
DS5-D1
DS5-b
DS5-a
HMNC
DEG
dB
V
RX
10-3
VAR
mV
%

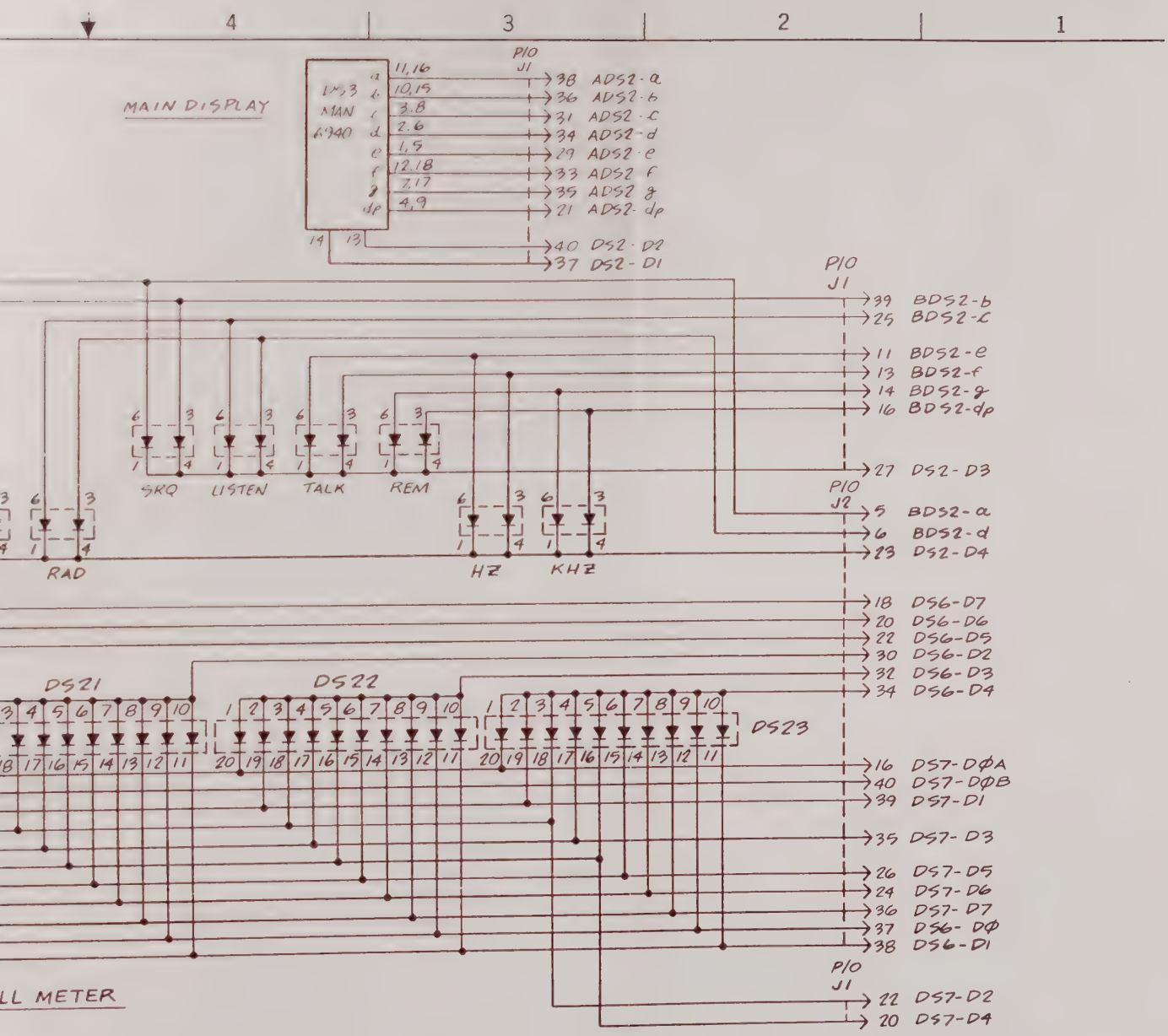
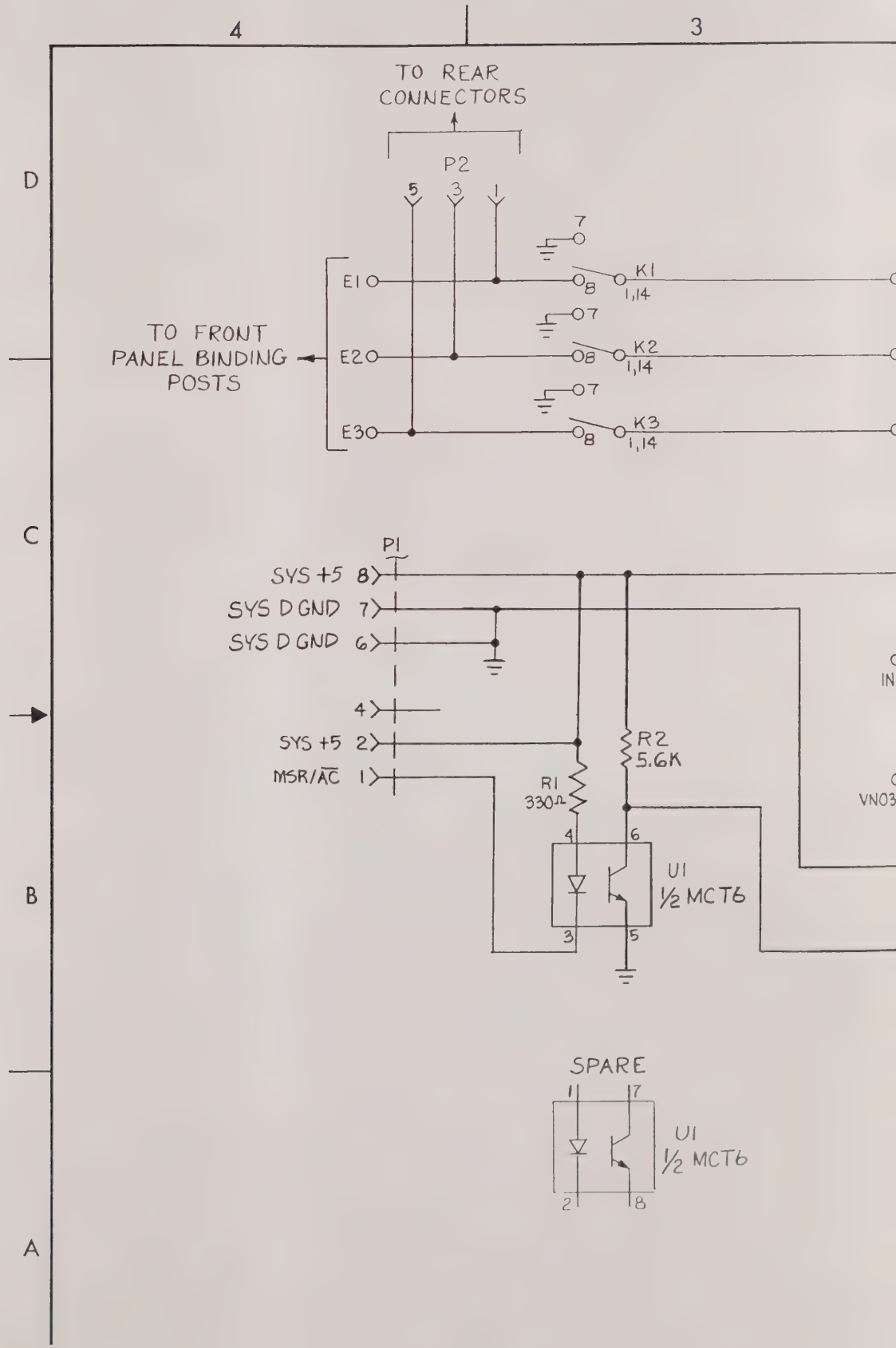


Figure 7-12. Display CCA A15A3 (P/N 787178), Schematic Diagram 768864/D


4
3
D
C
B
A
TO REAR CONNECTORS
P2
5
3
1
7
E1
K1
1,14
8
TO FRONT PANEL BINDING POSTS
E2
K2
E3
K3
P1
SYS +5 8
SYS D GND 7
SYS D GND 6
4
SYS +5 2
MSR/AC 1
R1
330Ω
R2
5.6K
4
6
3
5
U1
½ MCT6
SPARE
1
7
2
8
U1
½ MCT6

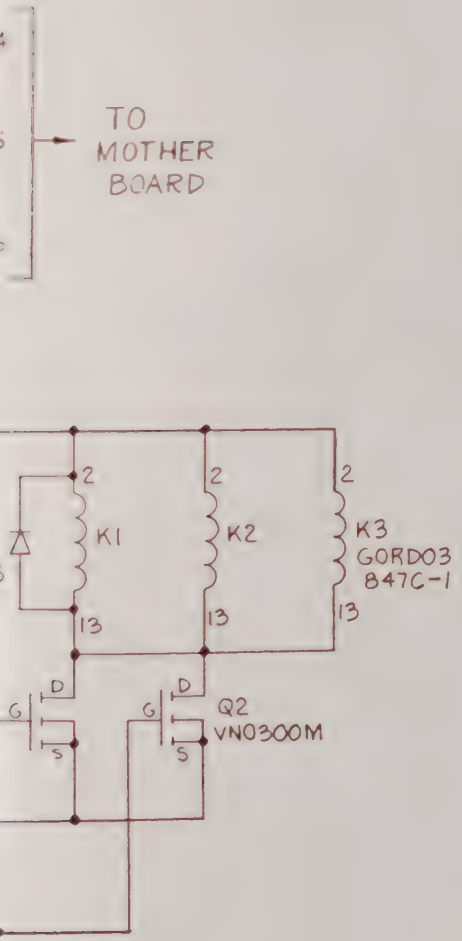
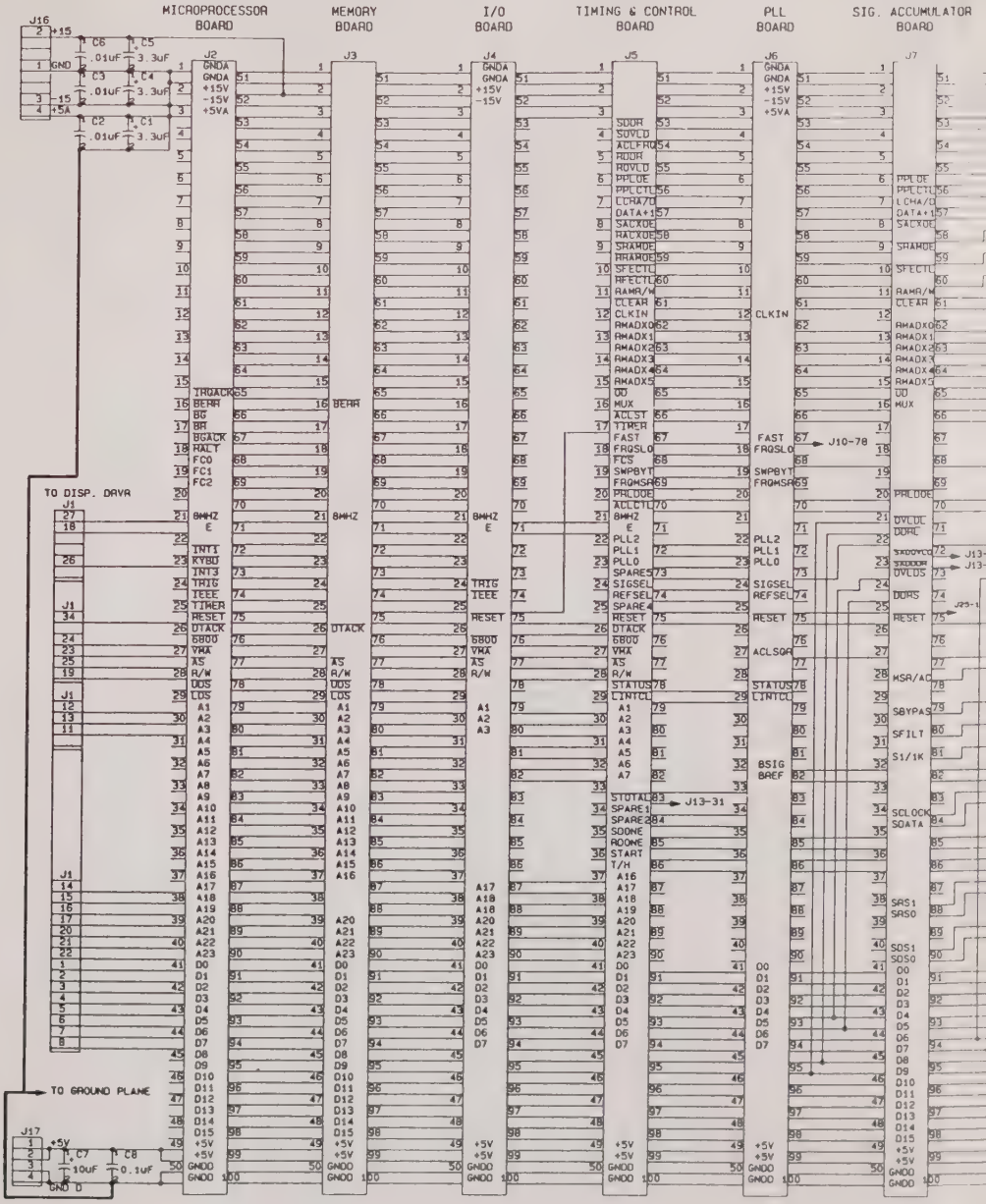


Figure 7-13. Isolation CCA A15A4, A15A5 (P/N 787448-1,-2), Schematic Diagram 768910/D



NOTE: FOR CONNECTORS J2 THROUGH J15, CONNECTION IS MADE ONLY AT POINTS WHERE SIGNAL NAMES APPEAR

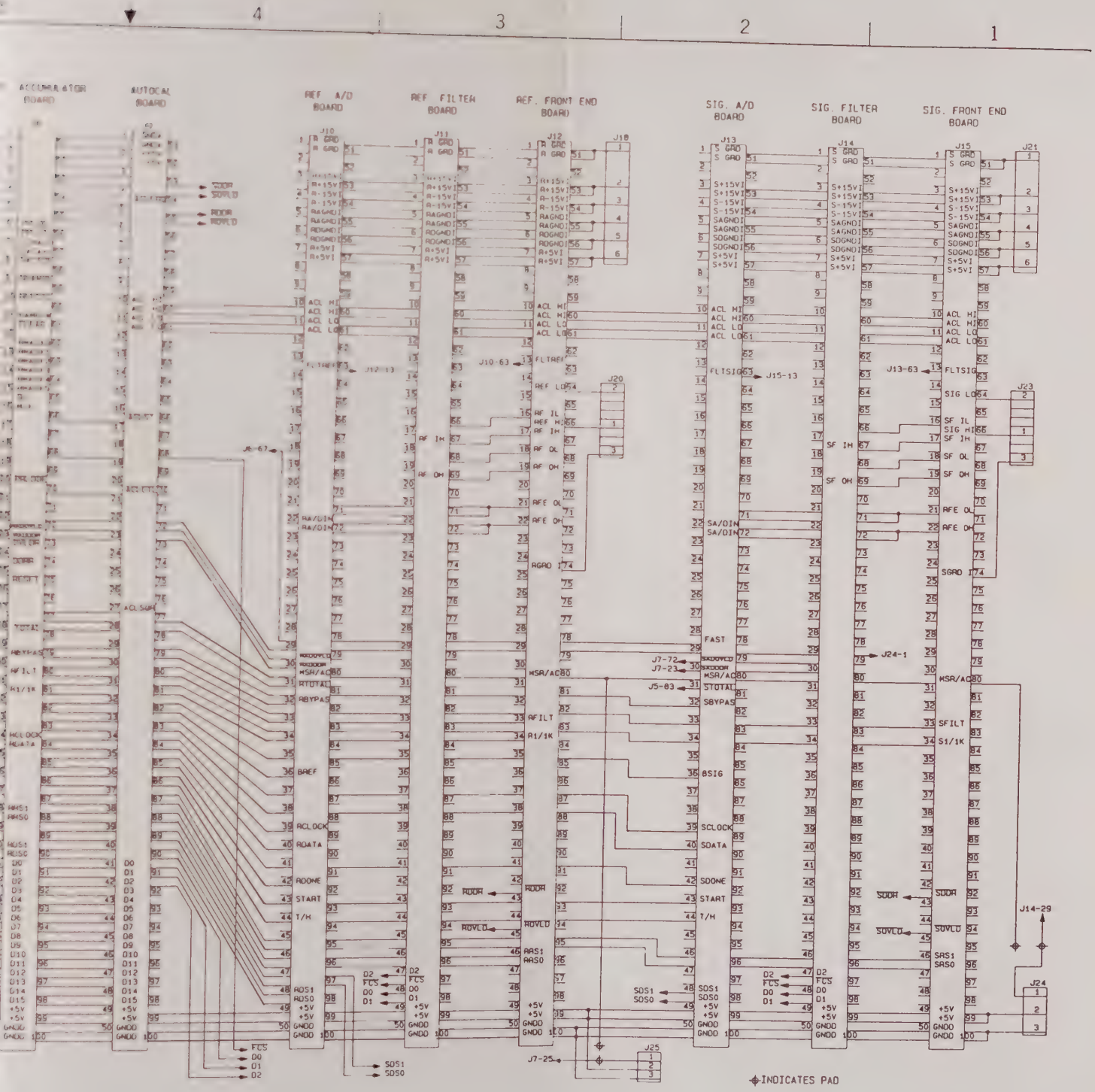


Figure 7-14. Mother Board A16A1 (P/N 787177), Schematic Diagram 768866/J

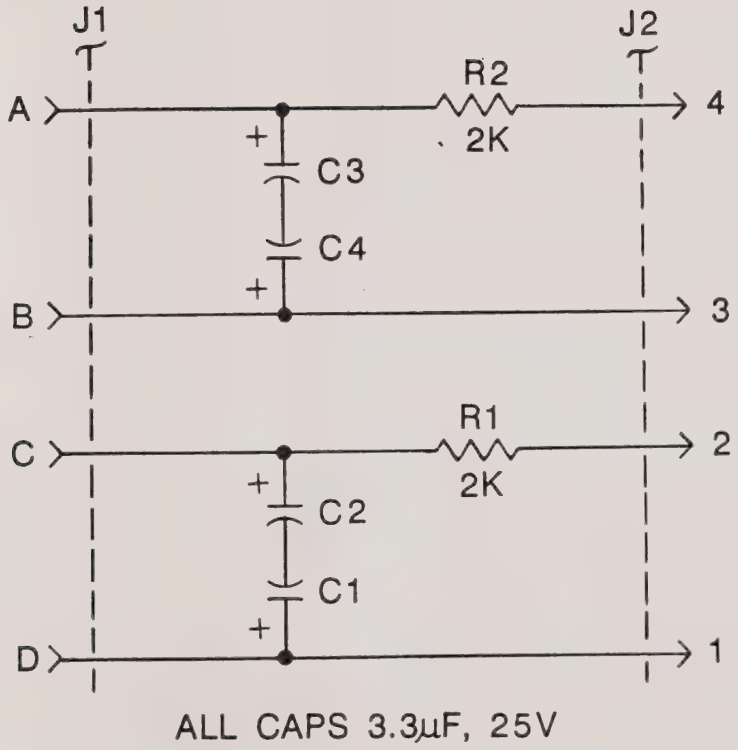
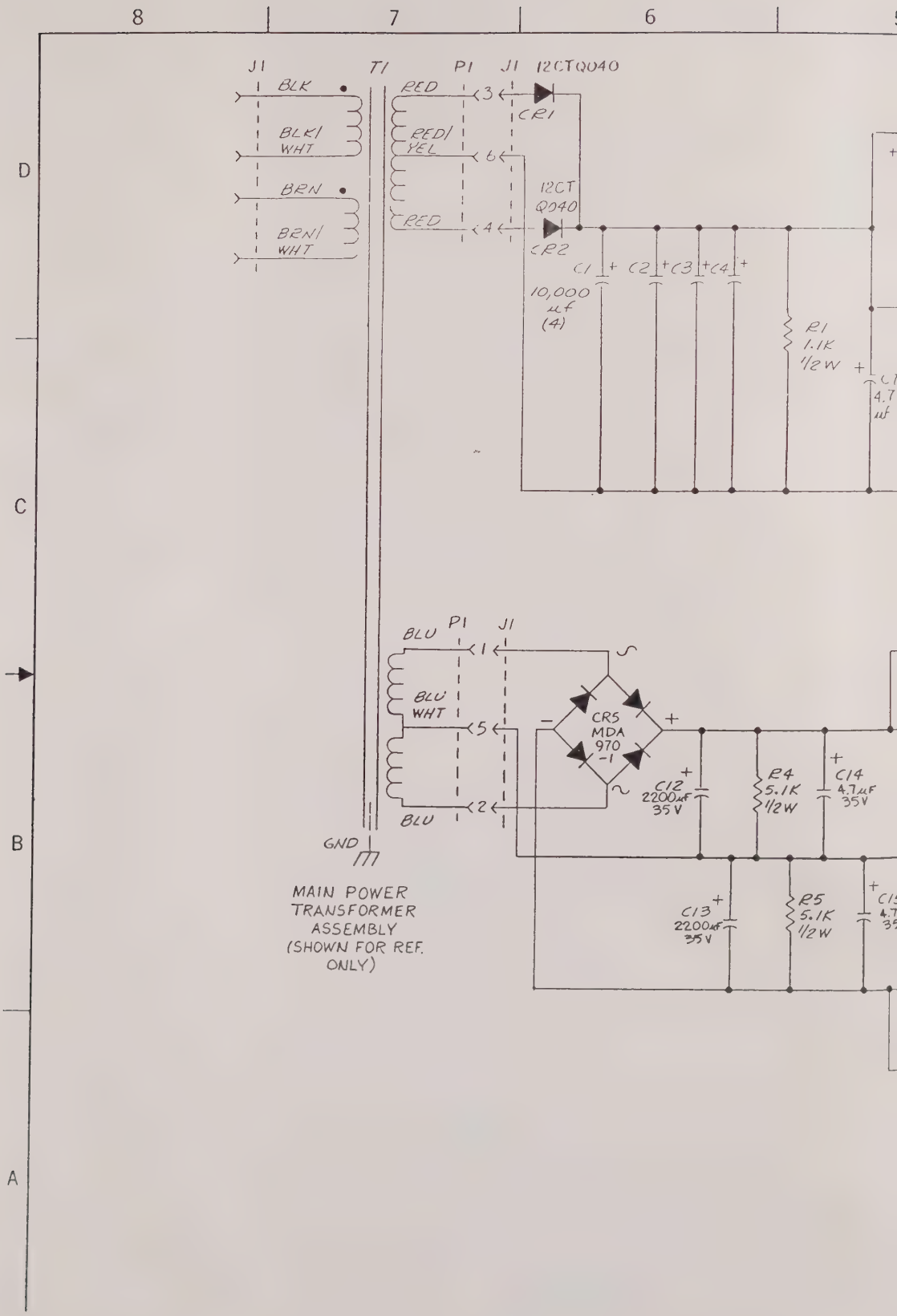


Figure 7-15. Recorder Filter Assembly
A17A1 (P/N 787667),
Schematic Diagram 768983/B


8
7
6
D
C
B
A
J1
T1
P1
J1
12CTQ040
BLK
BLK/
WHT
BRN
BRN/
WHT
RED
RED/
YEL
RED
3
6
4
CR1
12CT
Q040
CR2
C1
C2
C3
C4
10,000
µf
(4)
R1
1.1K
1/2W
4.7
µf
BLU
P1
J1
BLU
WHT
BLU
1
5
2
CR5
MDA
970
-1
C12
2200µF
35V
R4
5.1K
1/2W
C14
4.7µF
35V
C13
2200µF
35V
R5
5.1K
1/2W
GND
MAIN POWER
TRANSFORMER
ASSEMBLY
(SHOWN FOR REF.
ONLY)

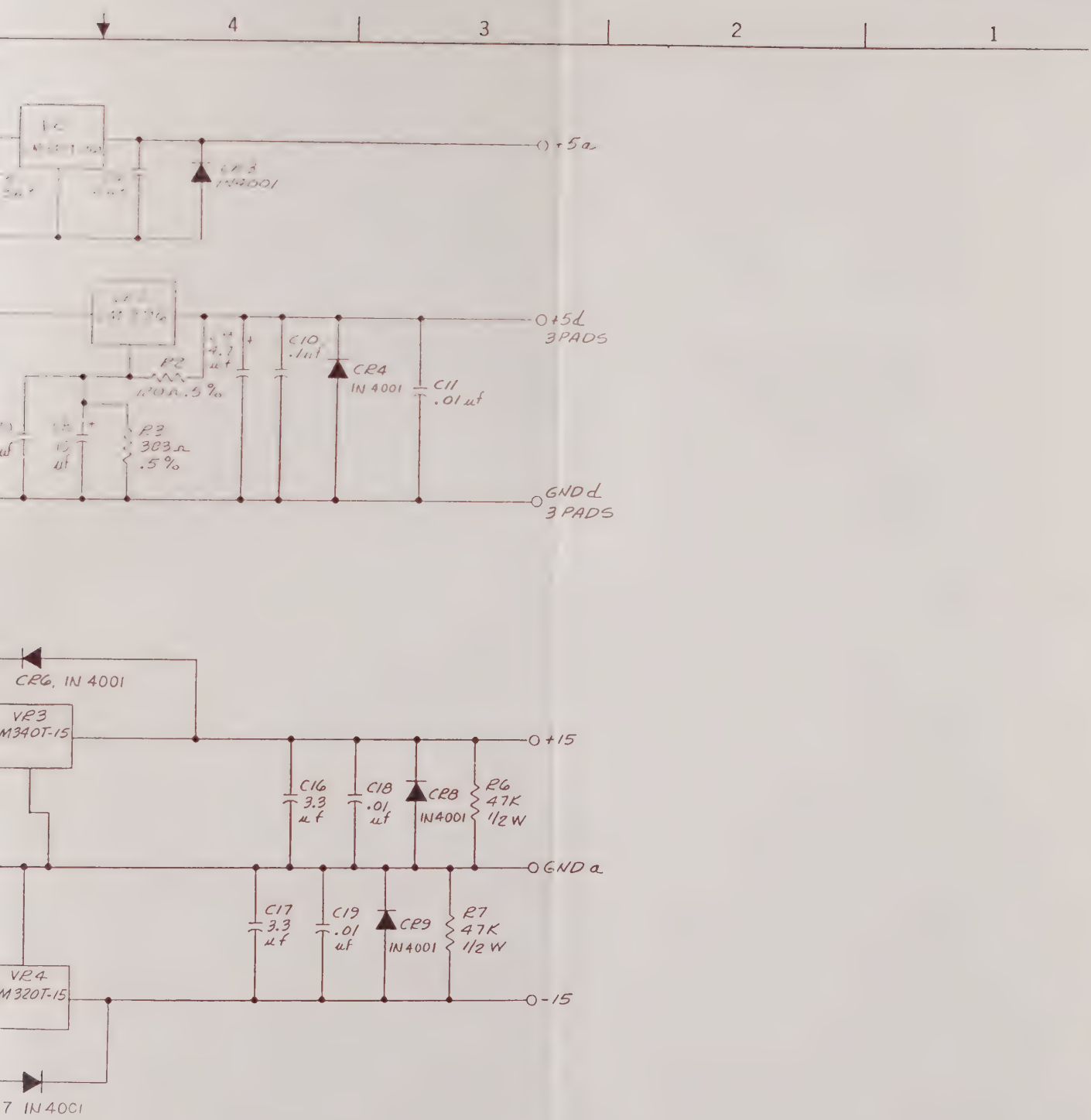
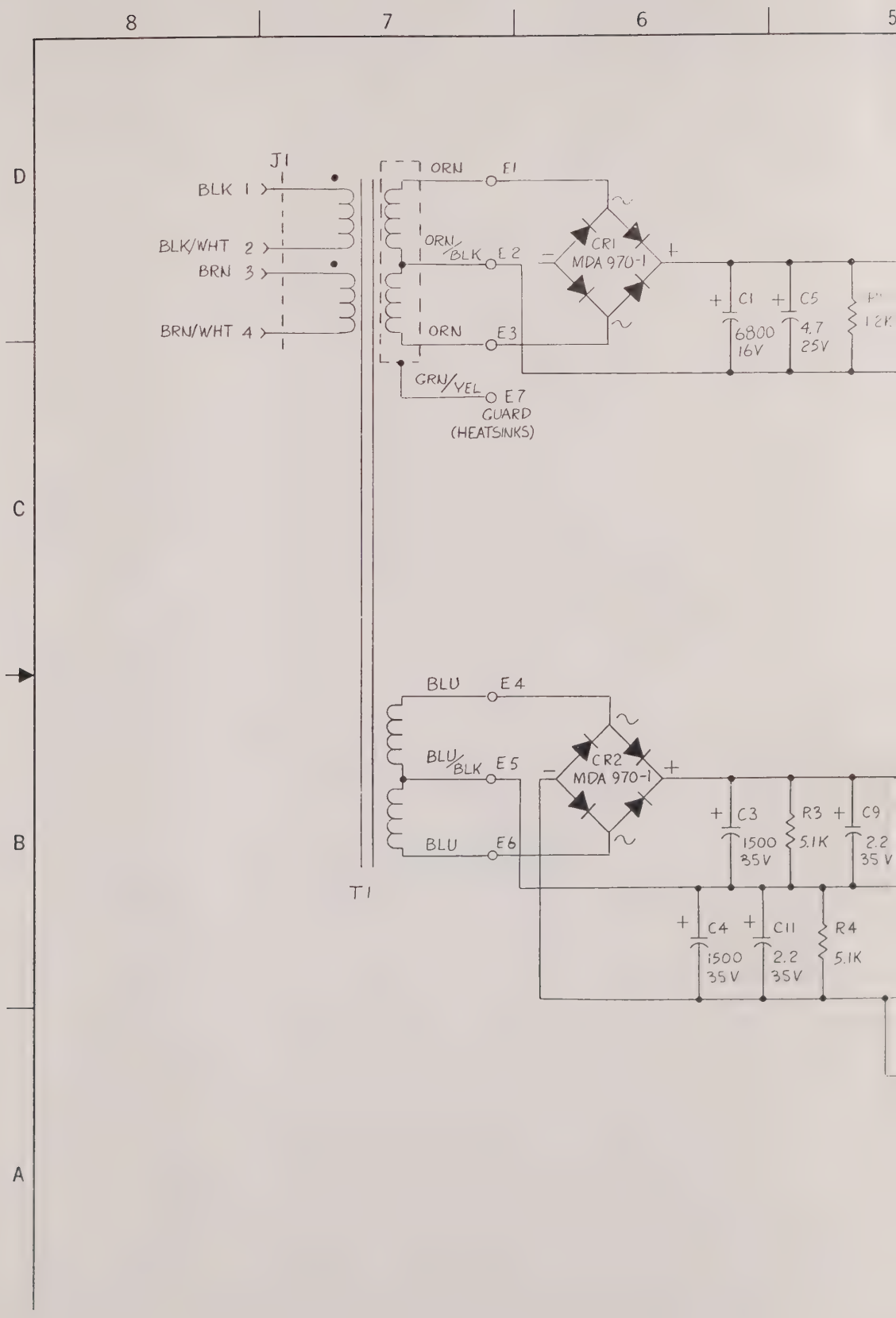
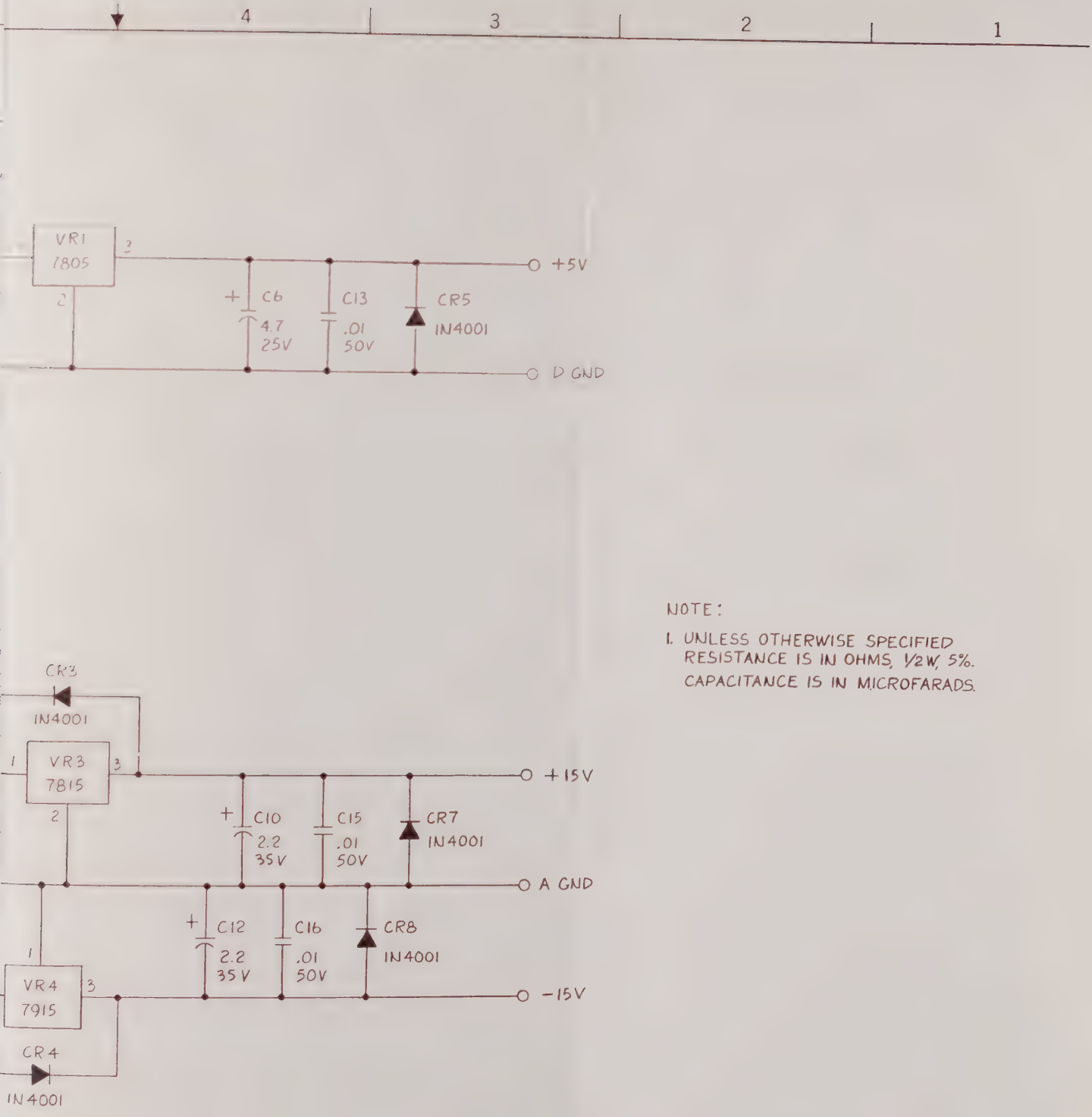


Figure 7-16. Main Power Supply CCA A17PS1 (P/N 787181), Schematic Diagram 768863/H

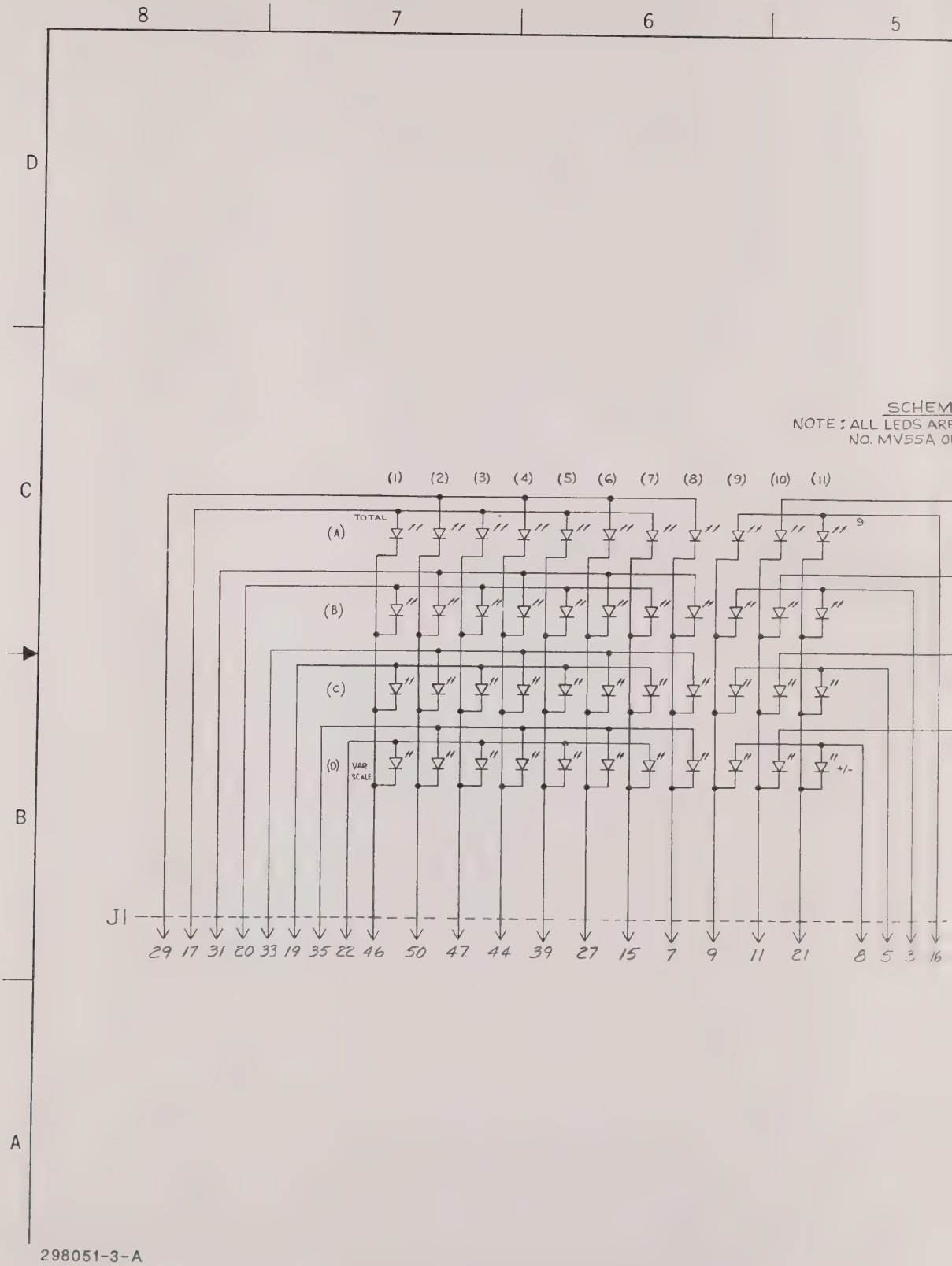

8
7
6
5
D
C
B
A
J1
BLK 1
BLK/WHT 2
BRN 3
BRN/WHT 4
ORN
F1
ORN/BLK
E2
ORN
E3
GRN/YEL
E7
GUARD
(HEATSINKS)
CR1
MDA 970-1
C1
6800
16V
C5
4.7
25V
12K
BLU
E4
BLU/BLK
E5
BLU
E6
CR2
MDA 970-1
C3
1500
35V
R3
5.1K
C9
2.2
35V
C4
1500
35V
C11
2.2
35V
R4
5.1K
T1



NOTE:

1. UNLESS OTHERWISE SPECIFIED RESISTANCE IS IN OHMS, 1/2W, 5%. CAPACITANCE IS IN MICROFARADS.

Figure 7-17. Isolated Power Supply A17PS2A1, A17PS3A1 (P/N 787313-1), Schematic Diagram 768876-1/A


8
7
6
5
D
C
B
A
SCHEM
NOTE : ALL LEDS ARE
NO. MV55A 0
(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11)
TOTAL
(A)
9
(B)
(C)
(D)
VAR SCALE
+/-
J1
29 17 31 20 33 19 35 22 46 50 47 44 39 27 15 7 9 11 21 8 5 3 16

298051-3-A

IIC
-ENERAL INSTRUMENT
APPROVED EQUIVALENT.

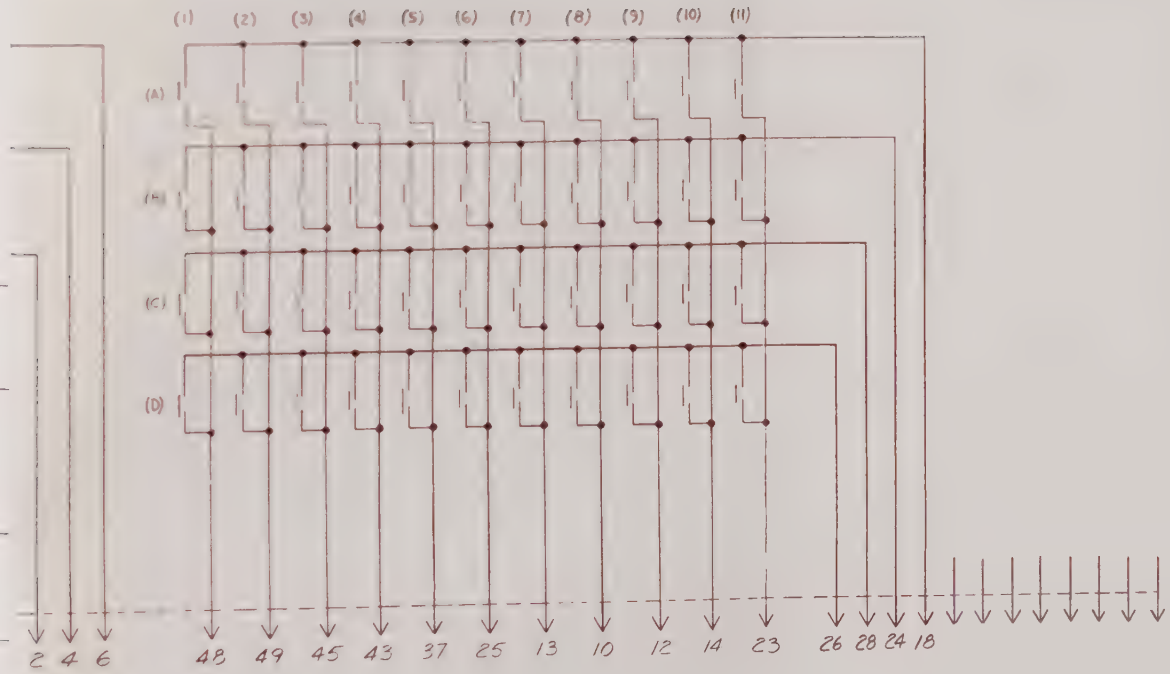


Figure 7-18. Membrane Panel (Keyboard) A15A1 (P/N 298051-3), Schematic Diagram

MODEL 2250

SECTION 8

UPDATE INFORMATION

. INTRODUCTION.

NAI continues to improve the performance of the DAV, corrections and modifica-
ns to the manual may be required. This section contains Product Revision Sheet
S) data which updates the unit to the most current configuration available.

MODEL 2250 (MM-I-5027A) PRODUCT REVISION SHEET #28255 SEPTEMBER 22, 1989

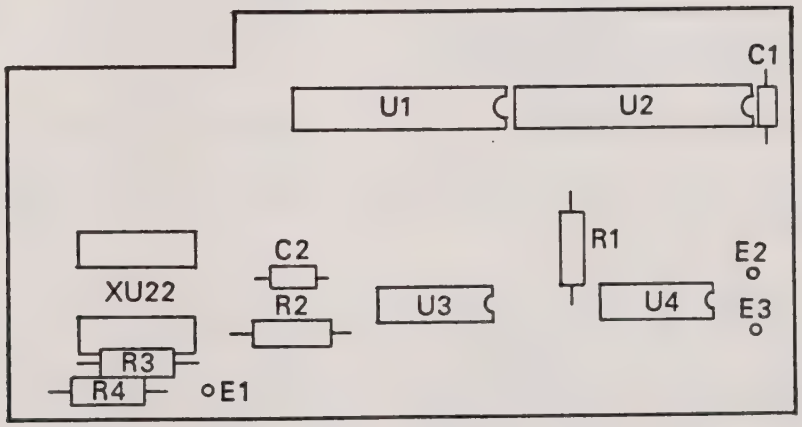
A. ASSEMBLIES AND REVISION LEVELS AFFECTED:

Memory CCA A2 - NAI P/N 787171-1, -2, -3, -4 Revision B and higher
Memory CCA Reset Adapter - NAI P/N 789092 Revision B

B. CHANGES:

1. In SECTION 6 - PARTS LIST Table 6-6 delete components R1, R2, R3, C28 and U22.

2. Add Figure 6-4A Memory CCA Reset Adapter as shown:

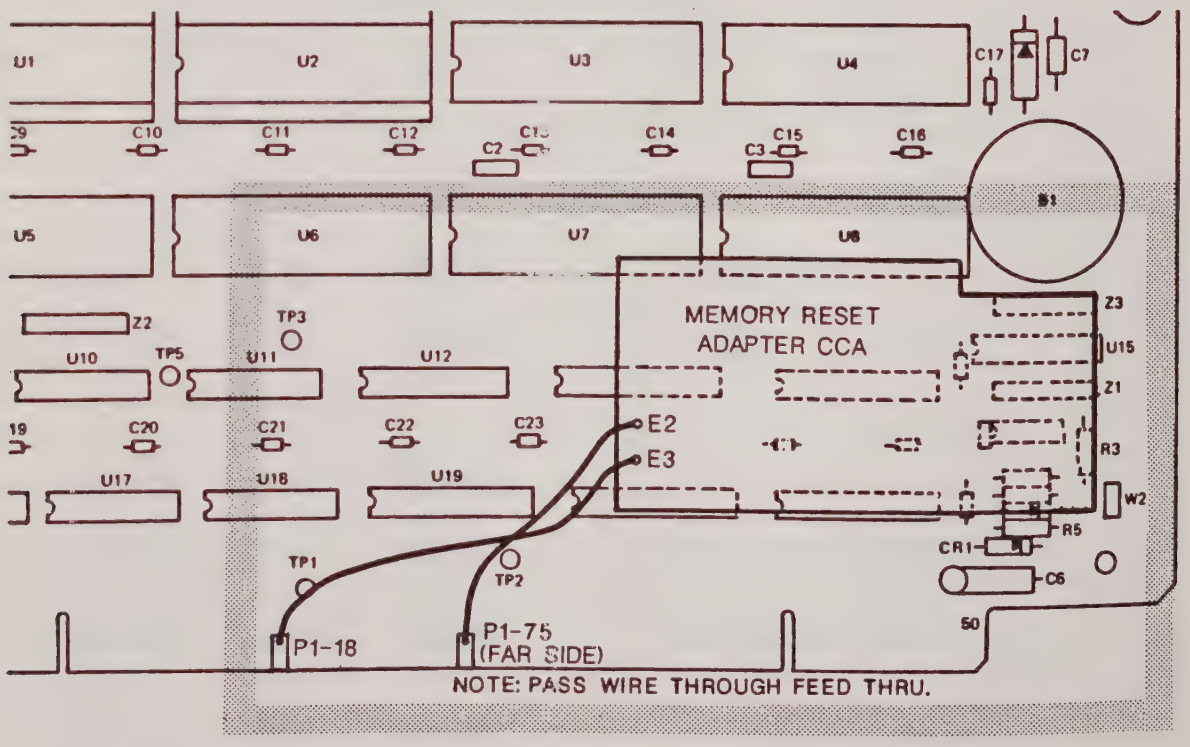


3. Add replacement parts Table 6-6A as follows:

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C1	Capacitor, Ceramic, 0.01 uf, 25 V, ±10%	885363	96733	W211BX103-K
C2	Same as C1			
E1	Post	880007	00779	87022-9
R1	Resistor, Composition, 4.7 M, 1/4 W, ±5%	807098	01121	CB4755
R2	Resistor, Composition, 470 k, 1/4 W, ±5%	806093	01121	CB4745
R3	Resistor, Metal Film, 10 k, 1/8 W, ±1%	880044	16299	NA55-10K

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
R4	Resistor, Metal Film, 6.34 k, 1/10 W, ±1%	807575	81349	RN55D6341F
U1	IC, CMOS, Hex Inverter, High Speed	888814	04713	MC74HC04N
U2	IC, CMOS, Retriggerable, Resettable Monostable Multi-vibrator	808819	04713	MC14538BCP
U3	IC, CMOS, Operational Amplifier	887250	32293	ICL7611DCPA
U4	IC, Interface, Dual-in-Line Peripheral Positive NAND Driver	883056	01295	SN75462P
XU22	Strip, 32 position	888815	51306	BBS-132-T-A

4. Install Memory CCA Reset Adapter and connect two wire jumpers to Memory CCA A2 as shown:



5. Add figure 7-3A as shown in this document.

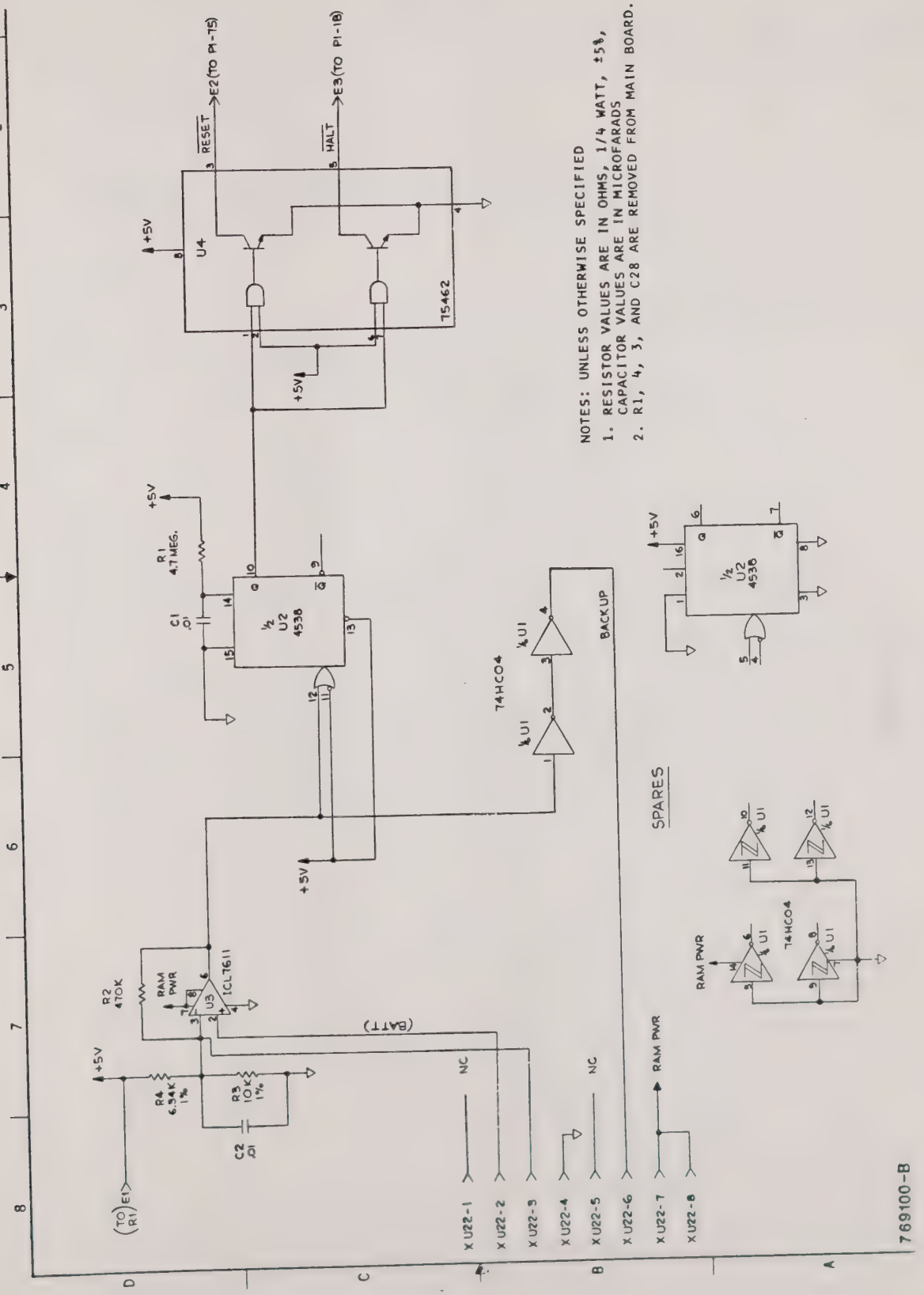


Figure 7-3A. Memory CCA Reset Adapter, Schematic Diagram

MODEL 2250 (MM-I-5027A) PRODUCT REVISION SHEET #28266/67 AUGUST 18, 1989

A. ASSEMBLIES AND REVISION LEVELS AFFECTED:

1. Top Assembly NAI P/N 402250 Revision E and higher.
2. Memory CCA NAI P/N 787171-3 Revision B and lower.
3. Memory CCA NAI P/N 787171-4 Revision A and higher.

B. CHANGES:

1. In SECTION 1 - GENERAL INFORMATION add the following to Table 1-2. F2 Unit Version/Check Sum Numbers:

Model Version	Check Sum Number
1.5	0EB6
2.0	FB2E
2.1	FB46

2. In SECTION 6 - PARTS LIST change the following:

   a. In Table 6-1. Digital Analyzing Voltmeter Model 2250, P/N 402250 - FX Common Parts add the following footnote to A2 Memory CCA:

   *Model 2250 Versions 1.4 - 1.5 use Memory CCA NAI P/N 787171-3 Revision B and lower.

3. In Table 6-6. Replacement Parts List: Memory Circuit Card Assembly A2 - 787171-4 Revision A and higher, add the following footnote:

   *In 2250 Model Versions 2.0 and higher PROMs U1 and U2 are NAI P/N 888672.

A. ASSEMBLIES AND REVISION LEVELS AFFECTED:

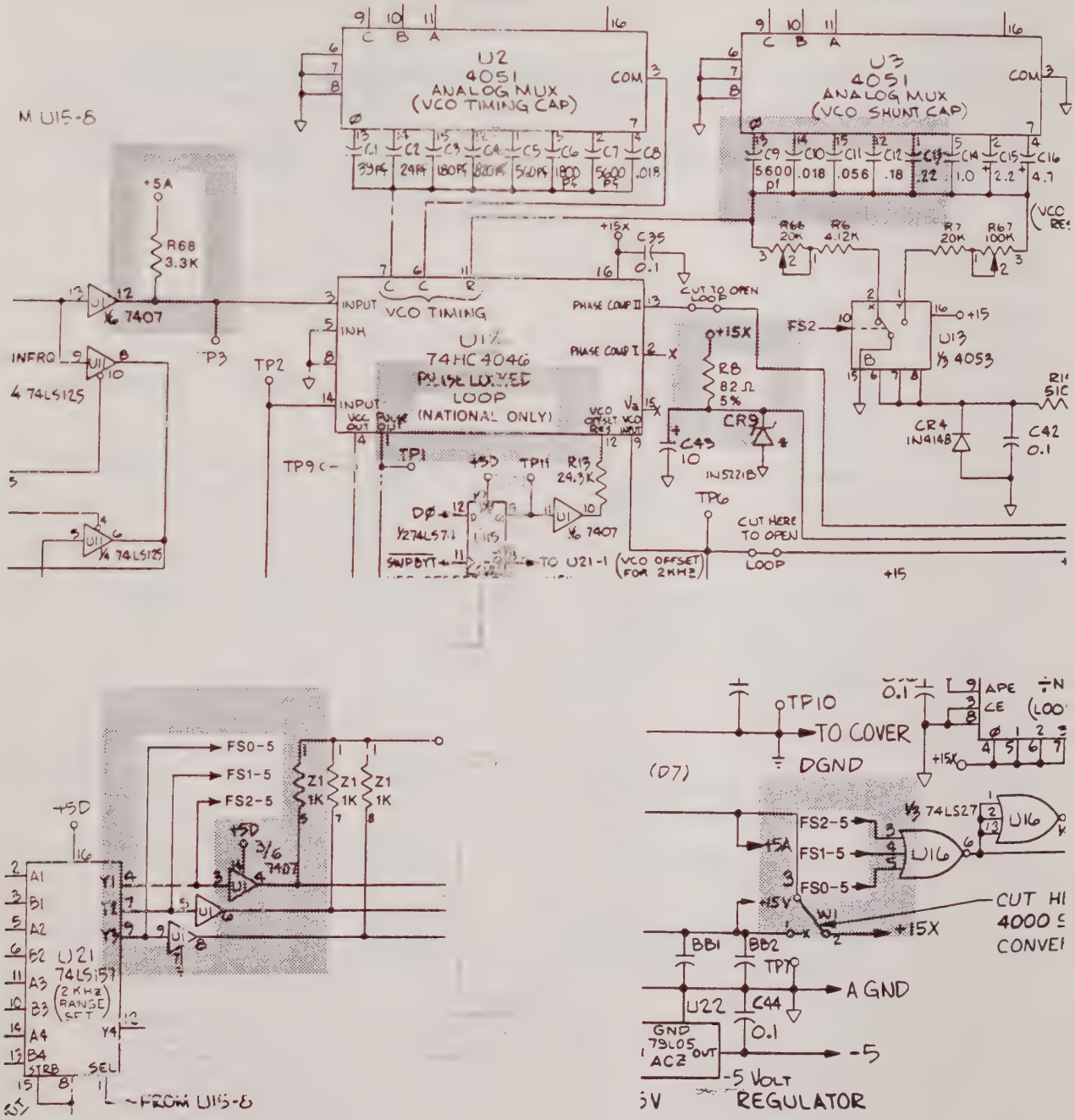
Phase-Locked Loop CCA A5 NAI P/N 787192-1 Revision Level D and higher.

B. CHANGES:

1. In SECTION 6 - PARTS LIST, Table 6-9. Replacement Parts List: Phase-Locked Loop CCA A5 - 787192-1 Revision D, make the following changes:

REF DES	DESCRIPTION	NAI P/N	FSCM	MFR P/N
C9	Same as C7			
C10	Same as C8			
C11	Capacitor, Ceramic, 0.056 uf, 100 V, ±10%	805454	81349	CK06BX563K
C12	Capacitor, Ceramic, 0.18 uf, 100 V, ±10%	886402	51406	CK06BX184K
C17	Capacitor, Ceramic, 0.015 uf, 100 V, ±10%	806367	81349	CK06BX153K
C18	Same as C11			
C22	Capacitor, Ceramic, 0.47 uf, 50 V, ±10%	886398	54407	CP487
CR6	Same as CR2			
CR8	Same as CR2			
R8	Resistor, Composition, 82 ohm, 1/8 W, ±5%	888711	01121	RCR056820JS
R64	Resistor, Composition, 5.1 k, 1/8 W, ±5%	880576	01121	BB5125
R68	Resistor, Composition, 3.3 k, 1/8 W, ±5%	805103	81349	RC05GF332J

2. In SECTION 7 - SCHEMATIC DIAGRAMS change Figure 7-6. Phase-Locked Loop CCA A5 (P/N 787192-1), Schematic Diagram 768878-1/D (Sheet 1 of 2) as shown:



MODEL 2250 (MM-I-5027A) PRODUCT REVISION SHEET #27731 JANUARY 10, 1989

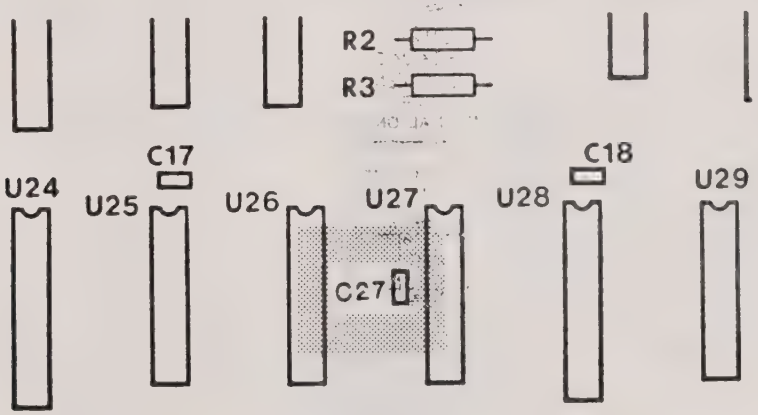
A. ASSEMBLIES AND REVISION LEVELS AFFECTED:

Timing and Control CCA A4 - NAI P/N 787173-1 Revision D and higher.

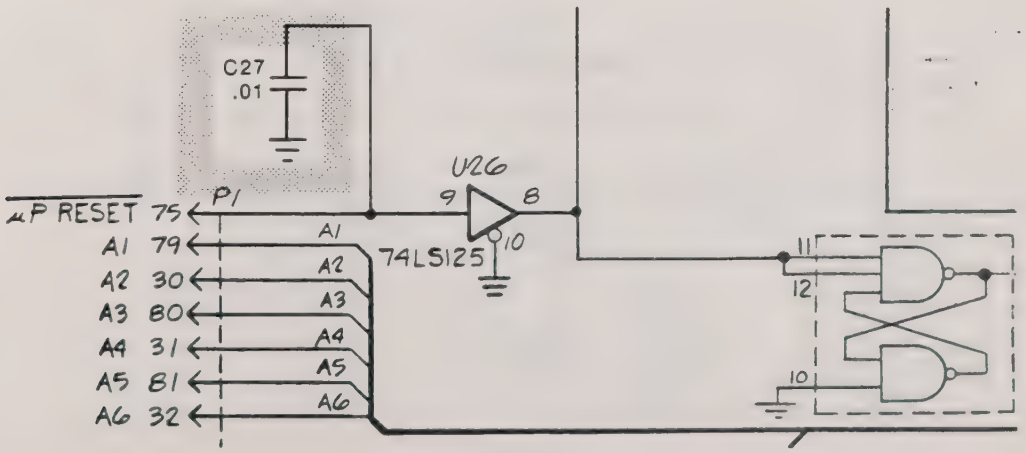
B. CHANGES:

1. In Table 6-8. Replacement Parts List: Timing and Control Circuit Card Assembly A4 - 787173-1 Revision D add Capacitor C27 NAI P/N 886061.

2. Change Figure 6-6. Timing and Control CCA A4 (P/N 787173-2 Revision D), Parts Location Diagram as shown:



3. Change Figure 7-5. Timing and Control CCA A4 (P/N 787173-1), Schematic Diagram 768879-1/C (Sheet 2 of 3) as shown:



MODEL 2250 (MM-I-5027A) PRODUCT REVISION SHEET #27730 JANUARY 3, 1989

A. ASSEMBLIES AND REVISION LEVELS AFFECTED:

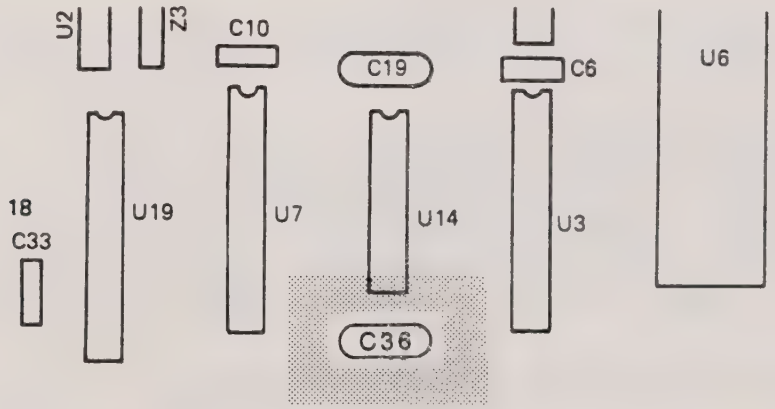
I/O CCA A3 - NAI P/N 787172-2 Revision B and higher.

B. CHANGES:

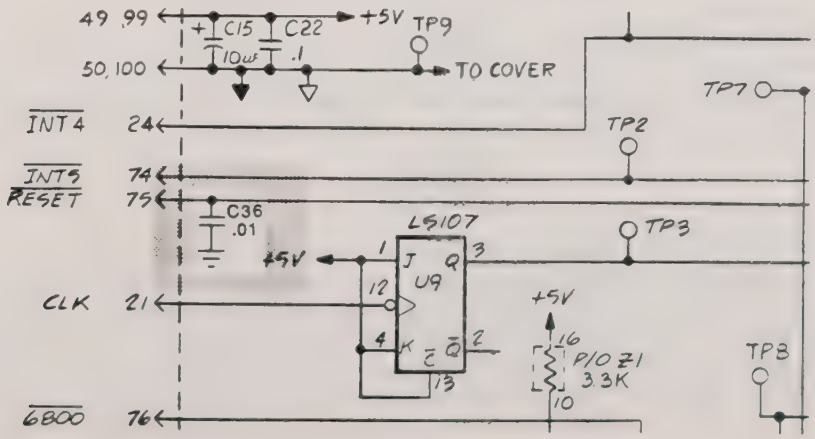
1. In Table 6-7. Replacement Parts List: I/O Circuit Card Assembly A3 - 787172-2 Revision B change the following:

   (a) Change capacitors C1, C3, C11, C13, C14, and C19 from NAI P/N 886061 to NAI P/N 886812.
   (b) Add capacitor C36 NAI P/N 886812.
   (c) Change I/O CCA revision level from B to D.

2. Change Figure 6-5. I/O CCA A3 (P/N 787172-2 Revision B), Parts Location diagram as shown:



3. Change Figure 7-4. I/O CCA A3 (P/N 787172-2), Schematic Diagram 768882-2/C (Sheet 1 of 2) as shown:



DAMAGE IN SHIP

...rectionally test the product(s) in accordance ...
...as it is received. If the product is damaged ...
...e, a claim should be filed immediately with ...
...y, with the purchaser's insurance company.

...ntity, await receipt of shipping instructions ...
...the day, unless indicated. Use original ...
...-plate blocking and bracing material to the ...
other sturdy, strong containers may be used ...
a sealed plastic ... and surrounded with ...
...g material to cushion firmly, preventing ...

LIMITED WARRANTY

A. The seller warrants products against defects in material and workmanship for twelve months from the date of original shipment. The seller's liability is limited to the repair or replacement of products which prove to be defective during the warranty period. There is no charge under the warranty except for transportation charges. The purchaser shall be responsible for products shipped until received by the seller.

B. The seller specifically excludes from the warranty 1) calibration, 2) fuses, 3) source inspection, 4) test data, 5) normal mechanical wear, e.g.: end-of-life on assemblies such as switches, printheads, recording heads, etc. is dependent upon number of operations or hours of use, and end-of-life may occur within the warranty period.

C. The seller is not liable for consequential damages or for any injury or damage to persons or property resulting from the operation or application of products.

D. The warranty is voided if there is evidence that products have been operated beyond their design range, improperly installed, improperly maintained or physically mistreated.

E. The seller reserves the right to make changes and improvements to products without any liability for incorporating such changes or improvements in any products previously sold, or for any notification to the purchaser prior to shipment. In the event the purchaser should require subsequently manufactured lots to be identical to those covered by this quotation, the seller will, upon written request, provide a quotation upon a change control program.

F. No other warranty expressed or implied is offered by the seller other than the foregoing.

CLAIMS FOR DAMAGE IN SHIPMENT

The purchaser should inspect and functionally test the product(s) in accordance with the instruction manual as soon as it is received. If the product is damaged in any way, including concealed damage, a claim should be filed immediately with the carrier, or if insured separately, with the purchaser's insurance company.

SHIPPING

On products to be returned under warranty, await receipt of shipping instructions then forward the instrument prepaid to the destination indicated. The original shipping containers with their appropriate blocking and isolating material is the preferred method of packaging. Any other suitably strong container may be used providing the product is wrapped in a sealed plastic bag and surrounded with at least four inches of shock absorbing material to cushion firmly, preventing movement inside the container.

LIMITED WARRANTY

A. The seller warrants products against defects in material and workmanship for twelve months from the date of original shipment. The seller's liability is limited to the repair or replacement of products which prove to be defective during the warranty period. There is no charge under the warranty except for transportation charges. The purchaser shall be responsible for products shipped until received by the seller.

B. The seller specifically excludes from the warranty 1) calibration, 2) fuses, 3) source inspection, 4) test data, 5) normal mechanical wear, e.g.: end-of-life on assemblies such as switches, printheads, recording heads, etc. is dependent upon number of operations or hours of use, and end-of-life may occur within the warranty period.

C. The seller is not liable for consequential damages or for any injury or damage to persons or property resulting from the operation or application of products.

D. The warranty is voided if there is evidence that products have been operated beyond their design range, improperly installed, improperly maintained or physically mistreated.

E. The seller reserves the right to make changes and improvements to products without any liability for incorporating such changes or improvements in any products previously sold, or for any notification to the purchaser prior to shipment. In the event the purchaser should require subsequently manufactured lots to be identical to those covered by this quotation, the seller will, upon written request, provide a quotation upon a change control program.

F. No other warranty expressed or implied is offered by the seller other than the foregoing.

CLAIMS FOR DAMAGE IN SHIPMENT

The purchaser should inspect and functionally test the product(s) in accordance with the instruction manual as soon as it is received. If the product is damaged in any way, including concealed damage, a claim should be filed immediately with the carrier, or if insured separately, with the purchaser's insurance company.

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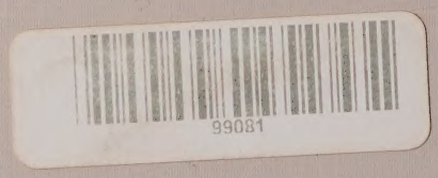

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